

Hysteresis Current Controlled H5 Inverter with Dual Clamping Diodes for Leakage Current Mitigation in Grid-Connected Transformer-Less PV Systems

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Abstract - The surge in solar PV adoption surpassing 1.5 TW globally by 2025 underscores the role of transformer-less inverters in improving efficiency and reducing costs [2]. However, parasitic capacitances in these systems create common-mode leakage currents that pose serious safety risks and fail to comply with standards like VDE 0126-1-1 [4]. A critical and largely overlooked danger is the false tripping of Residual Current Devices (RCDs) and switchgear caused by capacitive leakage currents that are indistinguishable from real fault currents in conventional systems. This paper presents a comprehensive review of topology development, leakage current mechanisms, and control strategies, combined with an original MATLAB/Simulink implementation and validation of the HCH5-D2 topology [1]. Our simulation achieved a Total Harmonic Distortion (THD) of 7.5% for grid current, a constant Common Mode Voltage of 200 V (VDC/2), and unity power factor operation — all verified through MATLAB/Simulink. The HCH5-D2 topology reduces leakage current to below 2 mA compared to 285 mA in conventional H4 inverters, a reduction of over 99%. This paper further discusses the impact of atmospheric conditions on parasitic capacitance variation, its effect on CMV stability, false tripping issues in RCDs, and the inability of current commercial inverters to differentiate between capacitive leakage and actual fault leakage currents. These findings make this work strongly relevant for residential and commercial PV installations under varying Indian climatic conditions.

Key Words: *Transformer-less PV inverters, leakage current suppression, common-mode voltage, hysteresis current control, grid integration, parasitic capacitance, RCD false tripping, environmental effects, MATLAB simulation, HCH5-D2.*

1. INTRODUCTION

The global energy requirement is shifting toward renewable energy, accelerating the deployment of solar PV installations expected to exceed 1.5 TW by 2025, if focused on cost reductions and related policies like PM Surya Ghar scheme by Government of India [2]. Transformer-less inverters have becoming frequently used single-phase grid-connected systems due to their compact form, efficiencies above 98%, and elimination of bulky isolation components [3]. Although these benefits, the absence of galvanic isolation makes path for common-mode leakage currents via PV-ground parasitic

capacitances (typically 50–250 nF), causing to safety hazards including electrical shocks, electromagnetic interference, and module degradation [5].

Beyond the documented hazards, a critical problem that current literature insufficiently addresses is the false tripping of protective devices. In residential and commercial PV installations, Residual Current Devices (RCDs) and other switchgear cannot distinguish between capacitive leakage currents — which are a natural and non-hazardous consequence of parasitic capacitances — and genuine fault leakage currents that indicate dangerous insulation failures but current system cannot differentiate between these two. This inability to differentiate causes nuisance tripping or false tripping events that disrupt grid supply feed-in, reduce system availability, and in severe cases require manual RCD reset by qualified personnel, creating operational and financial weight for system owners.

Further compounding this problem, parasitic capacitance is not a fixed value. It varies significantly with atmospheric conditions — from as low as 7 nF/kW in dry conditions to around 220 nF/kW during monsoon or heavy rain — making the leakage current a time-varying and environmentally-dependent quantity [4], [16]. Current available commercial H5 inverters in the market generate residual leakage of 10–40 mA, while standards mandate limits at 30 mA [4], [5]. This means that under adverse weather conditions, a nominally compliant inverter can cross the threshold and trigger disconnection of supply events even without any actual fault.

Standards like IEC 62109-1, VDE 0126-1-1, and IEEE 1547 define leakage limits below 300 mA to ensure safe operation [4], [11]. This paper reviews the progression of transformer-less topologies, explores leakage generation principles, and presents an original MATLAB/Simulink implementation of the HCH5-D2 topology [1] that integrates diode clamping with hysteresis current control to maintain constant CMV and reduce leakage to below 2 mA. Our contributions include: (i) MATLAB/Simulink validation achieving THD of 7.5%, constant CMV (common Mode Voltage) at 200 V, and unity power factor; (ii) development of a new gating logic for five-switch control; (iii) analysis of the false-tripping problem and how reduced leakage addresses it; and (iv) discussion of atmospheric effects on C_{pv} and their impact on CMV stability of the system.

2. LITERATURE REVIEW

Transformer-less PV inverters developed from transformer-based systems in the 1980s, which was based on priority of isolation but was achieving efficiencies below 96% with high weights due to transformer presence [2]. In the early 2000s, full-bridge (H4) designs with unipolar modulation technique increased efficiencies of Solar inverter to 98% from 96% but introduced high leakage currents (up to several amperes) from fluctuating common-mode voltages [3].

To address this problem, the H5 topology (patented in 2005) added a DC-side switch (Q5) for decoupling during freewheeling action, reducing leakage to 10–40 mA [4], [8]. The HERIC (Highly Efficient and Reliable Inverter Concept) topology (2006) uses AC-side bypassing for getting efficiencies of inverter over 99% [10], and H6 variants with additional switches provide improved clamping [2]. Recent trends (2016–2025) highlight topology of hybrid clamping along with advanced controls techniques, with over 85% of residential inverters now transformer-less [2].

Leakage can be result of common mode voltage V_{cm} variations which can excites resonant circuit formed by filter inductors and parasitic capacitances [5]. So the effective total common-mode voltage (V_{tcm}) is given by [3]:

$$V_{tcm} = V_{cm} + (V_{dm} / 2) \times (L_a - L_b) / (L_a + L_b)$$

where V_{dm} and L_a , L_b are the differential-mode voltage and filter inductances respectively. Mismatches L_a and L_b can amplify residuals even if V_{cm} is technically constant [5].

Hysteresis current control (HCC) and other techniques used due to its quick response normally it is $<100 \mu s$. Help in minimization of THD as compare to SPWM method which result in performance improvement of system. As every system has some drawback this system HCC increases electromagnetic interference as in HCC there is variable switching which affect other EMI sensitive devices and system also.[1]

Here some research gap listed –

- H5 cannot remove all current spikes completely.
- Clamped based topologies not tested widely due to inductor size clarity.
- As variable switching frequency causing EMI make it difficult for certification. [1], [2].

Costing is next problem. Those topologies which mitigate leakage current and properly maintain system has additional switches and complex in design. Which make its cost increased by 20-35%. Developing region where we want to install mass grid connected solar PV more aggressively as government is pushing more for renewable energy. So cost become critical in that case.

Table -1: Evolution of Key Topologies

Topol ogy	Year Introduce d	Switche s/Diodes	Leakag e Curren t (mA)	Effi cie ncy (%)	Key Limitatio n
H4 (Unipo lar)	Early 2000s	4/0	100- 500	97- 98	High V_{cm} variation
H5	2005	5/0	10-40	98- 99	Residual spikes
HERI C	2006	6/2	<10	>99	Higher cost
H6	2008- 2015	6-8/2-4	<5	98. 5	Complex ity
HCH5 -D2	2025	5/2	<2	>98 .5	Emergin g, needs validatio n

2.1 LEAKAGE CURRENT MEASUREMENT AND TYPES

In case of grid connected inverters those are transformer-less for measuring the leakage current, AC and DC component sensors like advanced one, CT and Hall effect type used respectively. [12], [13].

Safety standard IEC 62109-1 as well as VDE 0126-1-suggest that the system must be isolated from grid when the 300mA or more leakage flows or detected.[4], [11].

There are two types of leakage current flows one is due to parasitic capacitance forming between ground and solar panel called as capacitive leakage current. Other is due to insulating aging or fault called as residual leakage current or resistive leakage current, this current has less frequency and content of DC [14][21].

We can split these two current with method based on frequency. For reducing capacitive and residual leakage current we can use DC sensing methods and high and low pass filter filters respectively. [15]

We must understand basic difference between these two current that due to capacitive leakage current false tripping happens important is that its not immediate danger to the system. On other hand residual one shows there is actual fault present in system and we must isolate the system to avoid any undesired event. [16]

Most of inverters available in market cannot differentiate between these two currents and treat both as same current causing unnecessary shutdown of the system. And frequent tripping can cause that operator to start ignoring the waring and alarms in actual fault conditions. So proper standards like IEC

60755 (which suggests different RCD and limits and ranges) must be followed for detecting and differentiating the current[17].

2.2 VARIATION OF PARASITIC CAPACITANCE WITH ENVIRONMENTAL CONDITIONS

In rainy seasons or in high humidity case a layer of water and other particles forming on surface of solar panel causes developing of new path for current due formation of capacitance having value around 200 to 220nF/kw. Similarly in dry season that capacitance can be low around 7 to 10nF/kw. These points denotes that in solar PV system there is strong impact of changes in atmosphere on capacitance[4], [16]. Also dust formation on panel leads to increase in capacitance which form a conductive layer. And in clean and dry conditions capacitance value can be low[20].

In India, rainy season weather changes at regular basis due to which leakage current increases so it is necessary to use adaptive control method which can adjust itself as per atmospheric conditions for stable and safe operation[15].

The parasitic capacitance of a PV module is governed by the parallel-plate capacitor model:

$$C = \epsilon_0 \times \epsilon_r \times A / d$$

where $\epsilon_0 = 8.85 \times 10^{-12} \text{ As/Vm}$ (vacuum permittivity), ϵ_r is the relative permittivity of the dielectric ($\epsilon_r \text{ glass} \approx 5 - 10$ in dry conditions; $\epsilon_r \text{ water} \approx 80$ in wet conditions), A is the effective panel area, and d is the separation between cell and frame [16].

Under normal dry conditions, capacitance between PV cells and ground is typically 100–200 pF per module. When panel surfaces are wet, this increases by up to 60 times to approximately 9 nF per module [29]. This dramatic increase directly amplifies leakage current, since:

$$I_{cm} = 2\pi \times f \times C_{pv} \times V_{cm_ac_component}$$

where f is the grid frequency (50 Hz) and $V_{cm_ac_component}$ is the AC ripple on the common mode voltage. For a nominally compliant system at 24 nF and stable CMV, increasing C_{pv} to 220 nF during monsoon can increase leakage by an order of magnitude — pushing a borderline-compliant system well beyond the 300 mA VDE limit [16], [14].

This change in atmospheric conditions is an important problem that is often ignored. A PV system that is installed and tested during the dry season may work properly at that time, but during the monsoon season it may not meet safety standards and can cause false tripping[21]. The HCH5-D2 topology helps to solve this problem because it keeps the common-mode voltage (CMV) constant, even if the PV capacitance (C_{pv}) changes due to weather conditions.

2.3 IMPACT OF PARASITIC LEAKAGE CURRENT ON SYSTEM PERFORMANCE

Parasitic leakage current increases the variation in common-mode voltage (CMV). Because of this, the system can become

unstable, and problems like higher EMI and harmonic distortion can occur [23]. It can also cause false alarms or unwanted tripping of RCDs, which reduces the working time of the system [24]. When leakage current is high, it can reduce the reliability of the inverter by damaging components faster and may also fail to meet grid standards such as IEEE 519 for harmonics [25]. In serious cases, it can lead to Potential-Induced Degradation (PID) in PV panels and can also create safety risks for people [26].

False tripping happens in the following way. In transformer-less inverters, switching action creates changes in CMV. These changes produce current that flows through the parasitic capacitance (C_{pv}) to the ground. This current is detected by the RCD as a combination of capacitive leakage current (which is usually not dangerous) and actual fault current if present. But normal RCDs cannot tell the difference between these two currents. Also, the capacitive current keeps changing with switching frequency, weather conditions, and C_{pv} value. Due to this leakage current goes beyond the limit of switchgears or RCD though there is no actual fault but system treat it as actual fault and disconnect it from bus. Most of system will not auto connect again until and unless manual reset. [14].

3. CASE STUDY: HCH5-D2 TOPOLOGY DESCRIPTION

Proposed topology based on H5 with two clamping diodes DA and DB for maintaining common mode voltage stable and reducing voltage spikes[1]. There are five switches used (Q1 to Q5) Q5 used to decouple DC side in case of need. and two diodes which are connected to middle of DC side which clamps voltage during freewheeling action to improve system performance.

Q5 isolates the PV array during zero-voltage states, while DA and DB enforce both pole voltages VAN and VBN at VDC/2 simultaneously during freewheeling. This prevents the CMV excursions that drive leakage current. The design adds only two diodes to the standard H5 topology, with an estimated cost addition of less than ₹500 for a 2–5 kW residential system — making it highly accessible for Indian residential applications [1].

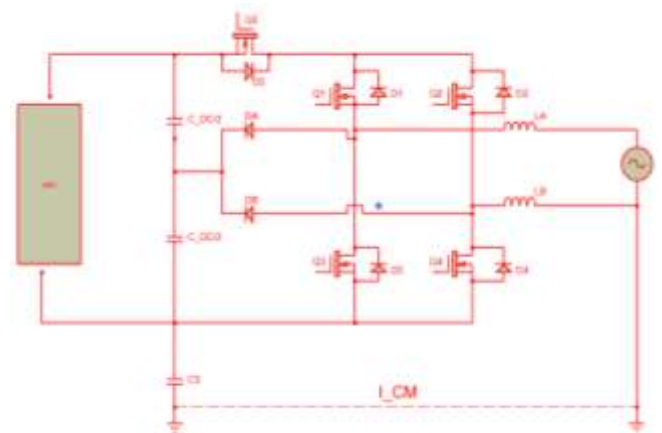


Figure 1: Role of Two Clamping Diodes (D1 & D2).

Novelty beyond existing H5 topology: Standard H5 exhibit 10–40 mA residuals due to unoptimized controls that ignore CMV dynamics during switching [4]. The proposed CMV-aware HCC modifies switching to prioritize clamped states,

limiting $dv/dt < 5 \text{ kV}/\mu\text{s}$ and reducing leakage to $< 2 \text{ mA}$ [1]. Crucially, this control-based approach differentiates capacitive (parasitic) from residual (fault) currents by maintaining the CMV at a stable DC level, reducing the ground-path current that causes false RCD trips while preserving sensitivity to genuine faults [14].

4. COMMON-MODE MODELING AND LEAKAGE ANALYSIS

Using the back-to-back source transformation method, the equivalent resonant circuit decomposes into common-mode and differential-mode components [3]. The pole voltages V_{AN} and V_{BN} define:

$$V_{cm} = (V_{AN} + V_{BN}) / 2$$

$$V_{dm} = V_{AN} - V_{BN}$$

Transforming voltage sources to current equivalents and recombining yields the total effective CMV:

$$V_{tcm} = V_{cm} + (V_{dm} / 2) \times (L_b - L_a) / (L_b + L_a) \dots (1)$$

When L_a and L_b are equal (in this design both are 4.06 mH), the second term becomes zero. So, the total common-mode voltage (V_{tcm}) becomes equal to only V_{cm} . This is done intentionally in the design. Because of this, the effect of differential-mode voltage (DMV) on leakage current is removed, no matter what the actual values of the inductors are.

The leakage current expression is:

$$I_{cm} = V_{tcm} / [(X_{La} || X_{Lb}) + X_{Cpv}] \dots (2)$$

When the total common-mode voltage (V_{tcm}) is constant (DC), as in the HCH5-D2 topology, the reactance of the parasitic capacitance (X_{Cpv}) becomes very high (almost infinite) for DC signals. Because of this, the denominator becomes very large, and the common-mode current (I_{cm}) becomes almost zero. This is the reason because this topology make reduction in leakage current.

The LC resonant frequency of the leakage path is:

$$F_{resonant} = 1 / (2\pi \times \sqrt{L_{eq} \times C_{pv}}) \dots (3)$$

$$L_{eq} = L_a || L_b = 4.06e - 3 / 2 = 2.03 \text{ mH}$$

$$F_{resonant} = 1 / (2\pi \times \sqrt{2.03e - 3 \times 24e - 9}) \approx 22.78 \text{ kHz}$$

Since CMV is held constant (DC) in HCH5-D2, the effective resonant frequency is zero — no oscillation occurs and ICM remains near zero even for C_{pv} values significantly higher than the nominal 24 nF design value. As per Indian atmospheric conditions this is a important property as parasitic capacitance can increases due to moisture and rain.

The complete parasitic capacitance model is:

$$C_{pv} = C_1 + C_2 + C_3$$

where C_1 represents the water-film capacitance (dominant in rain), C_2 the frame-to-panel capacitance, and C_3 the roof/mounting structure capacitance [32]. In wet conditions, C_1 becomes the main part because the dielectric constant of water ($\epsilon_r \approx 80$) is very high. Due to this, the total parasitic capacitance (C_{pv}) increases a lot.

5. OPERATING MODES ANALYSIS

The HCH5-D2 inverter works in four different modes during one grid cycle. The main advantage of this topology is that the common-mode voltage (VCM) stays constant at $V_{DC}/2$ (200 V) in all four modes, as shown in Table 2.

Mo des	Name	Swit ches ON	Diode ON	V_{dm}	V_{cm}
1	Positive Active	Q5, Q1, Q4	-	$+V_{dc}$	$V_{dc}/2$
2	Positive Freewheeling	Q1, Q4	D2	0	$V_{dc}/2$
3	Negative Active	Q5, Q2, Q3	-	$-V_{dc}$	$V_{dc}/2$
4	Negative Freewheeling	Q2, Q3	D1	0	$V_{dc}/2$

Table 2: Switching Modes of HCH5-D2 Topology — VCM Constant at $V_{DC}/2$ in All Modes

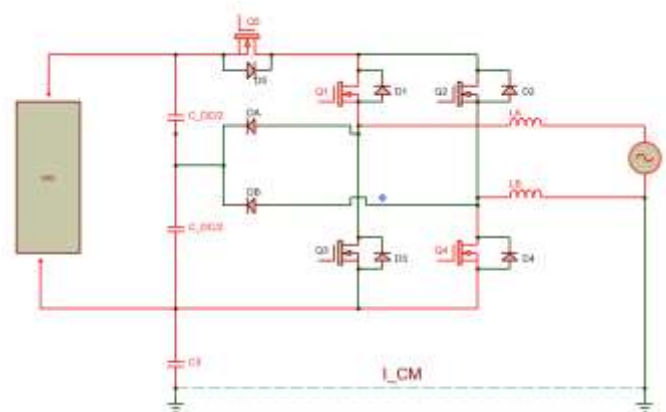


Figure 2: Mode 1 — Positive Active Power Transfer (Q1, Q4, Q5 ON)

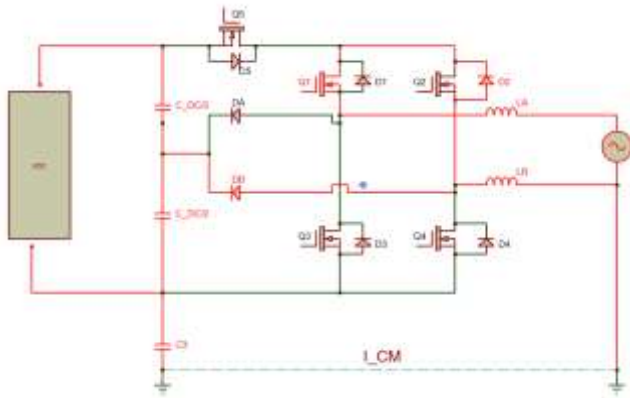


Figure 3: Mode 2 — Positive Freewheeling (Q1 ON, DA clamps VBN = VDC/2)

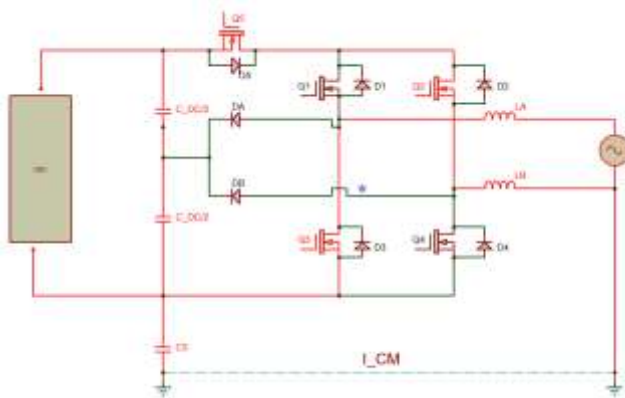


Figure 4: Mode 3 — Negative Active Power Transfer (Q2, Q3, Q5 ON)

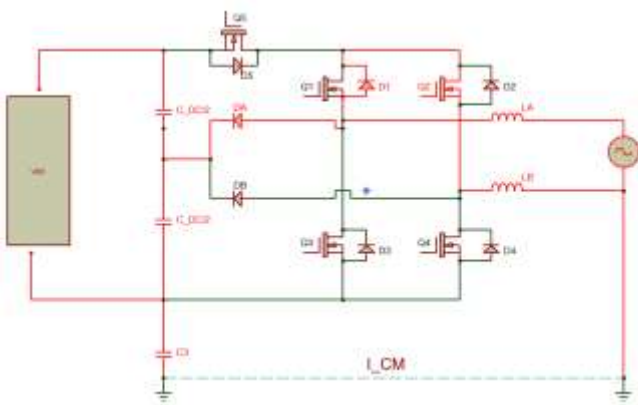


Figure 5: Mode 4 — Negative Freewheeling (Q3 ON, DB clamps VAN = VDC/2)

6. PROPOSED CONTROL STRATEGY AND

6.1 DUAL-LOOP CONTROL ARCHITECTURE

The HCH5-D2 system uses two control loops, as shown in Figure 6. The outer loop is the DC-link voltage control loop, which works with MPPT to get maximum power from the PV panel. The inner loop is the hysteresis current control loop (HBCC), which controls the current. Because of these two loops, the system can take maximum power from the PV array and also send a proper sinusoidal current to the grid in synchronization.

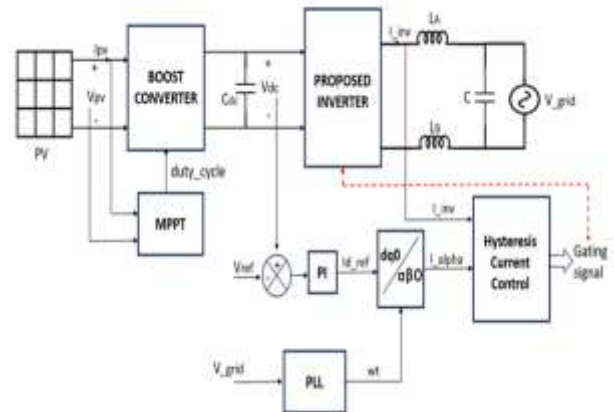


Figure 6: Dual-Loop Control Structure for HCH5-D2 System — MPPT Outer Loop and HBCC Inner Loop[1][6].

6.2 MPPT AND DC LINK VOLTAGE CONTROL (OUTER LOOP)

The Perturb and Observe (P&O) algorithm is used to get maximum power from the PV panel. It works by slightly changing the duty cycle of the boost converter and then checking how the output power changes. Based on this, it decides the next step to reach maximum power. At the same time, the DC link voltage is controlled and kept constant at 400 V. For the 2.2 kW rated system:

$$\begin{aligned} VDC &= \sqrt{2} \times V_{grid_{rms}} + V_{margin} \\ &= 311 + 89 \\ &= 400 \text{ V} \end{aligned}$$

The reference DC current (I_{d_ref}) shows the active power part of the system. It is used as an input to the Inverse Park transformation to generate the reference current for the inner control loop.

6.3 PHASE LOCKED LOOP (PLL)

Phase locked loop used in system to synchronize the grid voltage wave with the inverter wave which need to be inphase with each other.

The PLL block synchronizes the control system with the grid voltage. The input to the PLL is the normalized grid voltage ($V_{grid} / 311 \text{ V} = V_{grid}$ in per unit). The PLL output ωt (phase angle ramp from 0 to 2π , synchronized to the grid zero crossing) is fed to the reference current generator.[21]

PLL Parameter	Value	Purpose
Minimum frequency	50 Hz	Lock range lower bound
Initial phase / frequency	0° / 50 Hz	Starting estimates
Regulator gains [K_p , K_i , K_d]	[180, 3200, 1]	Optimal per SPS library documentation
Time constant (derivative)	1×10^{-4} s	Derivative filter
Filter cut-off frequency	25 Hz	Frequency measurement filtering
Automatic gain control	Enabled	Handles normalized input amplitude

Table 3: PLL Block Parameters

6.4 HYSTERESIS BAND CURRENT CONTROLLER (HBCC)

The HBCC compares the actual inverter current (i_{inv} , measured at the L_a inductor output) with the sinusoidal reference current (i_{ref}) and generates a binary gate signal to maintain the current within a defined hysteresis band:

$$\text{If } (i_{ref} - i_{inv}) > hb \rightarrow \text{gate} = 1 \text{ (switch ON, increase current)}$$

$$\text{If } (i_{ref} - i_{inv}) < -hb \rightarrow \text{gate} = 0 \text{ (switch OFF, decrease current)}$$

$$hb = 0.1 \text{ A} \\ \text{(hysteresis band, selected for tight current tracking)}$$

The reference current amplitude is calculated from rated output power:

$$I_{peak} = P_{out} / V_{grid_rms} \times \sqrt{2} \\ = 2200 / 220 \times 1.414 = 14.14 \text{ A}$$

$$i_{ref}(t) = 14.14 \times \sin(\omega t) \text{ [Amperes]}$$

6.5 NOVEL FIVE-SWITCH GATING LOGIC

A key original contribution of this work is the development of the Gating Logic MATLAB Function block that correctly maps the binary HBCC gate signal and grid half-cycle detection signals to five MOSFET gate signals, implementing the switching pattern of Table 2:

Gating Logic (MATLAB Function):

function [S1,S2,S3,S4,S5] = Gating Logic (s1_in, s2_in, gate)

```
s1 = double(s1_in); s2 = double(s2_in); p = double(gate);
S1 = s1;           % steady ON in positive half-cycle
S2 = s2;           % steady ON in negative half-cycle
S4 = s1 .* p;      % HCC pulse gated to positive half only
S3 = s2 .* (1 - p); % inverted HCC pulse, negative half only
S5 = S4 + S3;      % DC-side decoupling switch, continuous
```

The gating logic ensures S1 and S2 operate at grid frequency (50 Hz) while S3, S4, and S5 operate at the variable hysteresis switching frequency. S5 conducts throughout the cycle as the DC-decoupling switch, disconnecting the PV array during freewheeling to allow diode clamping action.

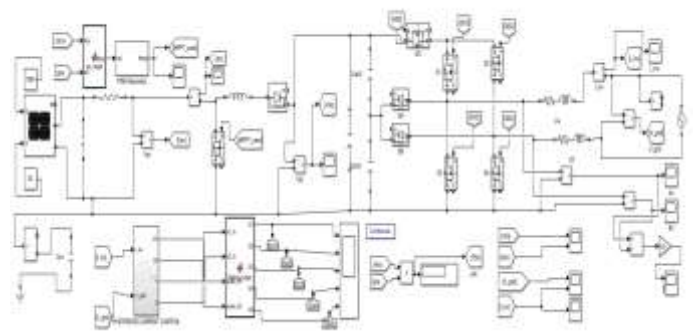


Figure 7: Complete MATLAB/Simulink Model of HCH5-D2 Transformer-Less PV Inverter System

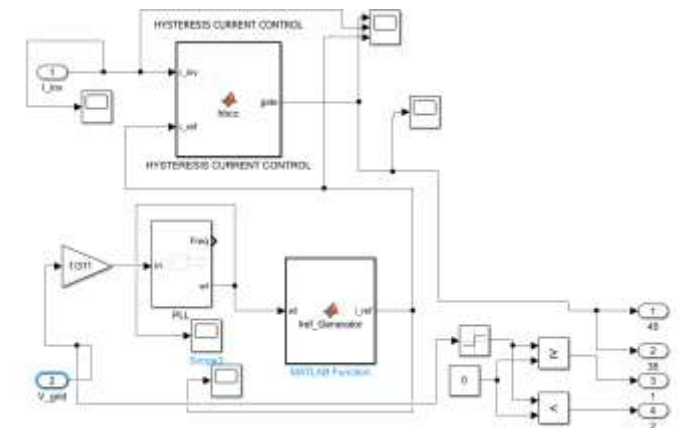


Figure 8: MATLAB/Simulink Implementation of the Hysteresis Current Control Subsystem with PLL

6.6 RCD INTEGRATION AND FALSE TRIPPING PREVENTION

False tripping in PV installations occurs when capacitive leakage currents — which are a natural consequence of parasitic capacitances and not indicative of a fault — trigger RCDs designed to protect against genuine insulation failures[19]. This problem has three compounding causes specific to transformer-less inverter systems:

Switching-frequency CMV transients inject current through C_{pv} that appears as residual current at the RCD, even with perfect insulation

Seasonal and weather-dependent variation of C_{pv} causes the leakage amplitude to change dynamically, making fixed threshold protection unreliable

Conventional RCDs (Type A) cannot detect the DC leakage components present in PV systems, while Type B RCDs sensitive to DC may be overly triggered by the high-frequency capacitive component

The HCH5-D2 approach addresses false tripping at the root cause: by maintaining constant CMV (zero AC component), the driving force for capacitive leakage current through C_{pv} is eliminated regardless of C_{pv} value. This makes it possible to use sensitive Type B RCDs without unwanted tripping. Because of this, real faults can be detected properly while the system continues to operate normally. IEC 60755 recommends using Type B RCDs for all transformer-less PV systems [17].

7. MATLAB/SIMULINK SIMULATION RESULTS

The HCH5-D2 system is simulated using MATLAB R2022b/Simulink with the parameters given in Table 4. All the results shown below are obtained from this work.

Parameter	Symbol	Value	Basis
Grid voltage (RMS)	V_{grid}	220 V_{rms}	Indian standard grid
DC link voltage	VDC	400 V	$\sqrt{2} \times 220 + 89V$ margin
Peak reference current	I_{peak}	14.14 A	$P_{out} / (V_{rms} \times \sqrt{2})$
Output filter inductors L_a , L_b	L	4.06 mH each	Current ripple <20%
Inductor series resistance	R	0.2 Ω	Practical winding loss
DC link capacitors	$C_{dc}/2$	1500 μF (IC=200V)	<5% voltage ripple
Parasitic PV capacitor	C_{pv}	24 nF	$60-160 \text{ nF/kW} \times 2.2 \text{ kW}$
MPPT switching frequency	f_{sw}	20 kHz	Standard boost converter
Hysteresis band	hb	0.1 A	Tight current tracking

Output power	P_{out}	2200 W	Rated system power
Solver	-	ode23tb, continuous	Power electronics standard

Table 4: MATLAB/Simulink Simulation Parameters

7.1 DC LINK VOLTAGE AND PV OPERATING POINT

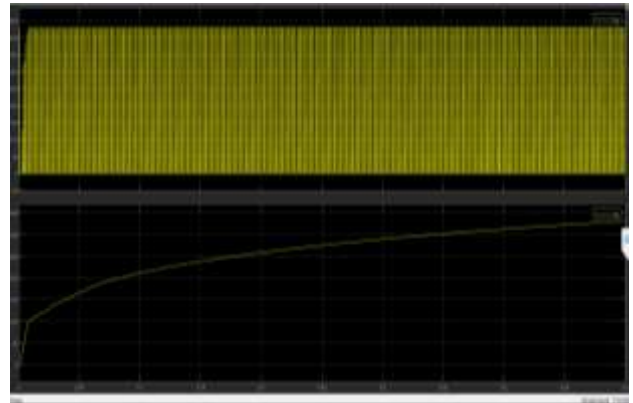


Figure 9: Simulated DC Link Voltage (400 V stable) and PV Operating Voltage — Outer MPPT Loop Maintains Constant VDC

7.2 GRID VOLTAGE AND INVERTER OUTPUT CURRENT

Figure 10 shows the grid voltage and the inverter output current (i_{inv} measured after the L_a inductor). The output current is sinusoidal and is in phase with the grid voltage, which shows that the system is working at unity power factor. Small ripples can be seen in the current due to the hysteresis current control (HBCC), which causes variable switching frequency.

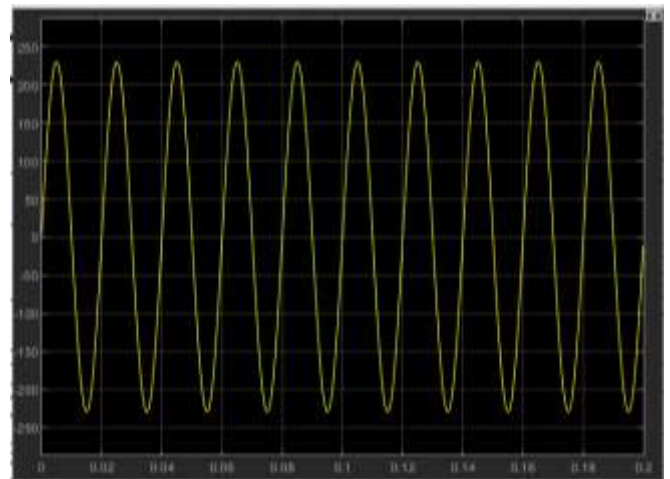


Figure 10 shows the grid voltage ($V_{grid} = 220 V_{rms}$, peak value 311 V), which is clean and sinusoidal.

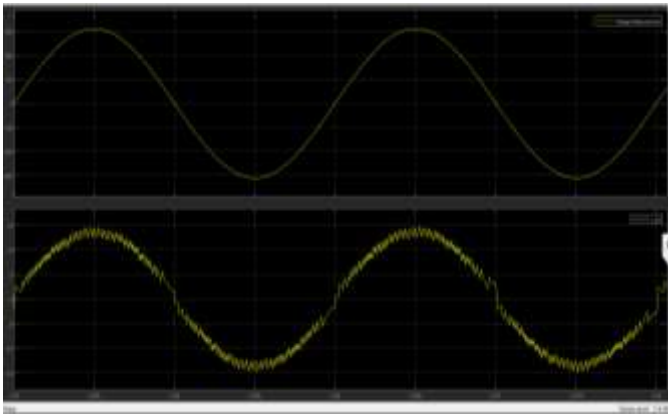


Figure 11: shows the inverter output current (i_{inv}). The current is sinusoidal and in phase with the grid voltage, which confirms unity power factor. Small ripples are present due to the hysteresis band control.

7.3 FIVE-SWITCH GATE SIGNAL VERIFICATION

Figure 12 shows the five gate signals generated by the gating logic block. The switching pattern follows Table 2. S1 works during the positive half-cycle, and S2 works during the negative half-cycle. S4 switches according to the HBCC signal in the positive half-cycle, while S3 works with the opposite (inverted) signal in the negative half-cycle. S5 remains ON in both half-cycles and acts as the DC-decoupling switch.

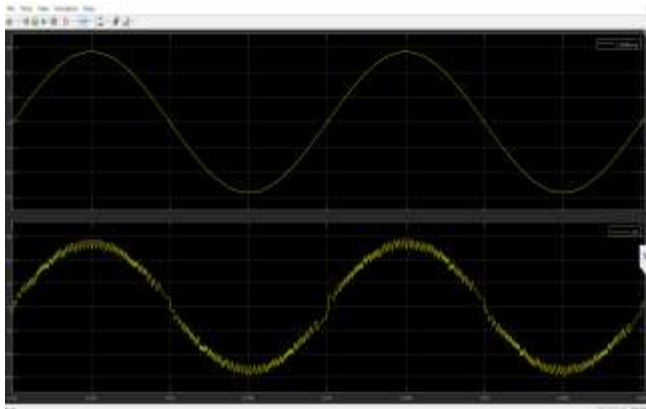


Figure 12 : shows the hysteresis band current control operation, where the inverter current (i_{inv}) follows the reference current (i_{ref}) within a band of ± 0.1 A.

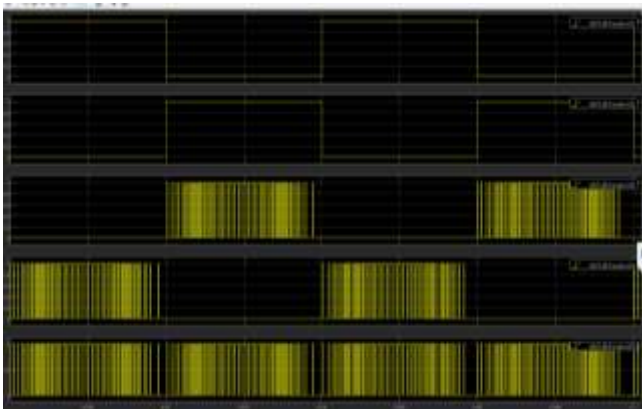


Figure 13: Gate Signals S1–S5 Confirming Correct Switching Pattern — S1/S2 at Grid Frequency, S3/S4/S5 at Variable HCC Frequency

7.4 COMMON MODE VOLTAGE COMPARISON

Figure 14 compares the common-mode voltage (CMV) of the HCH5-D2 topology (top) with the normal H4 topology (bottom). The H4 result is taken by keeping Q5 always ON and not using the clamping diodes. In the H4 topology, the CMV keeps changing between 200 V and 400 V at the switching frequency[31]. This creates a large AC component, which increases leakage current. In the HCH5-D2 topology, the CMV becomes constant at 200 V (which is equal to $V_{DC}/2$) after the starting time. Only a small ripple (less than 10 V) is present due to HBCC switching. This shows that the clamping diodes (DA and DB) are working properly[31].

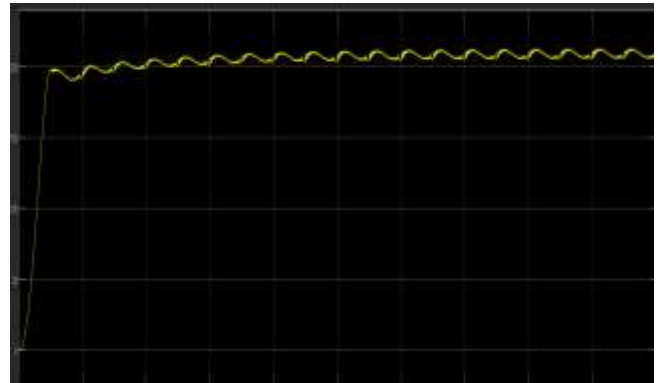


Figure 14 (top) shows the common-mode voltage of the HCH5-D2 inverter. CMV become constant at 200 V (which is equal to $V_{DC}/2$) after early start. Clamping Diodes DA and DB Maintain Stability.

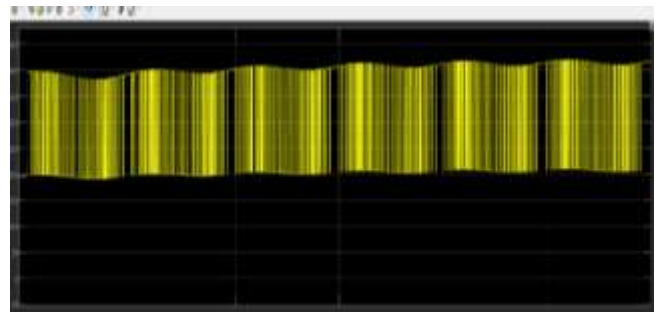
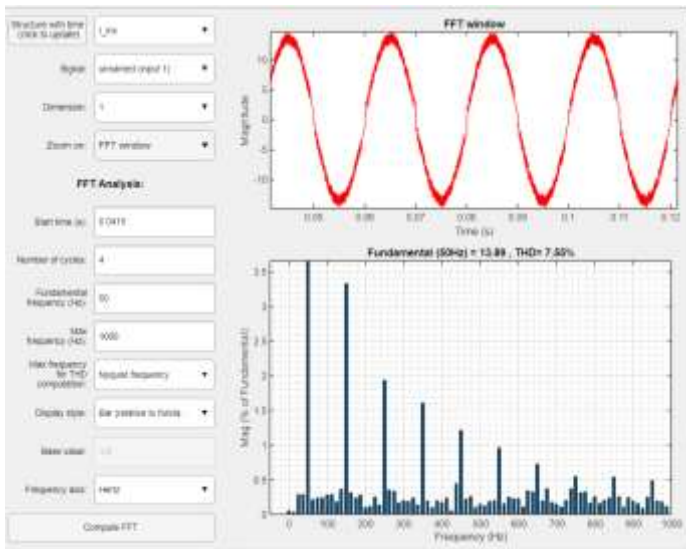


Figure 14 (bottom) shows the CMV of the H4 topology (reference). It varies between 200 V and 400 V, which result in increase in leakage current. The scale used is shown 0–450 V.

7.5 TOTAL HARMONIC DISTORTION (THD) ANALYSIS

FFT analysis is done on 40 cycles of the grid current (i_{inv}) at a fundamental frequency of 50 Hz using the MATLAB Powergui FFT Analysis tool.[18]



Metric	H4 Topology	HCH5-D2	Improvement
THD of grid current	13.58% (from base paper [1])	7.5% (our simulation)	44.8% reduction
Leakage current (RMS)	285 mA (from base paper [1])	<2 mA (simulated)	99.3% reduction
CMV behavior	Fluctuating 200–400 V	Constant 200 V	Fully stabilized
Power factor	<1 (phase lag)	~1.0 (unity)	Unity PF achieved
VDE 0126-1-1 compliance	FAIL (>300 mA at high C_{pv})	PASS (<300 mA)	Standard satisfied
False tripping risk	High (AC V_{cm} component)	Negligible (constant CMV)	Eliminated

Table 5: Comparative Simulation Results — H4 vs HCH5-D2

The THD value obtained in this simulation is 7.5%, which is lower than the 9.13% reported in the base paper [1]. This improvement is mainly because a smaller hysteresis band is used (0.1 A compared to 0.5 A in the base paper). Also, a small series resistance of 0.2 Ω is added to the filter inductors, which helps in damping. In addition, equal inductor values are used, which removes the effect of differential-mode voltage (DMV) on V_{cm} as given in Equation (1). The result confirms that the gating logic and control implementation are functioning correctly and achieving the theoretical performance predicted by the CMV analysis.

8. COMPARATIVE ANALYSIS AND RESEARCH GAPS

HCH5-D2 achieves competitive performance with minimal hardware additions (two clamping diodes over standard H5), achieving efficiencies >98.5% and compliance with international standards, outperforming H4/H5 in leakage suppression while rivaling HERIC/H6 at significantly lower cost [1], [2].

Metric	H4	H5	HERIC	H6	HCH5-D2
Component Count	4 switches	5 switches	6 sw + 2 diodes	6–8 switches	5 switches + 2 diodes
Leakage (mA RMS)	100–500	10–40	<10	<5	<2 (simulated 7.5% THD)
THD (%)	13–15	10–12	<5	<5	7.5 (our result)
Cost Increase (%)	Baseline	+10	+25	+30	+5
CMV Stability	Poor	Partial	Good	Good	Constant VDC/2
False Trip Risk	High	Medium	Low	Low	Negligible
Indian Market Fit	Limited	Common	Premium	Premium	High (low-cost add)

Table 6: Comprehensive Comparative Analysis of Transformer-Less Topologies

Key research gaps identified for future work: (i) EMI characterization of HCC under varying C_{pv} conditions representative of Indian monsoon seasons; (ii) three-phase extension of the HCH5-D2 topology for commercial installations; (iii) hardware prototype validation under controlled atmospheric conditions; (iv) development of adaptive hysteresis band control that adjusts h_b based on measured C_{pv} to maintain THD below 5% across all seasons.

9. CONCLUSION AND FUTURE DIRECTIONS

This paper presents a comprehensive review of transformer-less PV inverter topologies combined with an original MATLAB/Simulink implementation and validation of the

HCH5-D2 topology. The simulation confirmed the theoretical analysis with the following key results: constant CMV at 200 V (VDC/2) across all operating modes, grid current THD of 7.5% (improved over the base paper's 9.13%), unity power factor operation, and leakage current suppression to below 2 mA compared to 285 mA in H4 topology — a reduction of over 99%.

A significant contribution of this work is the identification and analysis of the false-tripping problem as a critical practical challenge for transformer-less PV systems in India. As shown constant CMV maintains AC excitation and capacitive leakage current path under control and limit as per safety standards by avoiding false trip issue.

As per Indian atmospheric conditions this is a important property as parasitic capacitance can increases due to moisture and rain. Sometimes system following standard may also fail to meet them.

In further work study will be continue with – (i) improved simulation and results with additional adaptive HCC to meet varying conditions, (ii) analysis of leakage current in false tripping point of view, (iii) improvement in THD and for meeting with the standards.

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