Implementation MAC Unit using Vedic Multiplier and Reversible Gates

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Abstract: *The design of Multiplier-Accumulator (MAC) unit can be implemented by using the Vedic multiplier and the reversible logic gates. The designing of Vedicmultiplier is designed by using four multiplier blocks and carry save adder. Theperformance of the MAC operation depends on the multiplier unit and the adder units. Here the designing of an adder can be implemented by using the reversible gates. In this project we use DKG reversible gate to increase the life time of the design. It can acts as full adder and full subtractor. Nowadays reversible gates are mostly used because it acts as heat controllers by this we can easily increase the life time of design. Here, we proposed 64-bit MAC using Vedic multiplier and the DKG adder. For better understanding we comparethis proposed 64bit MAC is with the basic MAC. Finally, it has been proved that the proposed MAC 10ns(time delay)isspeeder than basic MAC. The overall Simulation is carried out with Xilinx ISE 14.7.*

1. INTRODUCTION:

In the accumulate adder the previous MAC output and the present output will added and it consists of Multiplier unit, one adder unit and both will get be combined by an accumulate unit. The major applications of Multiply-Accumulate (MAC) unit are microprocessors, logic units and digital signal processors, since it determines the speed of the overall system [13]. The efficient designs by MAC unit are Nonlinear Computation like Discrete Cosine or wavelet Transform (DCT), FFT/IFFT. Since, they are basically executed by insistent application of multiplication and addition, the entire speed and performance can be compute by the speed of the addition and multiplication taking place in the system. Generally the delay, mainly critical delay, happens due to the long multiplication process and the propagation delay is observed because of parallel adders in the addition stage The main idea of this paper is comparison of area, speed and other parameters of Conventional MAC unit with the Vedic MAC design.

2. LITERATURE SURVEYMAC Unit

A multiplying function can be carried out in three ways: partial product Generation (PPG), partial product addition (PPA), and final conventional addition. The two bottle necks that should be considered are increasing the speed of MAC are partial product reduction and accumulator block. The 32 bit Mac design by using Vedic multiplier and reversible logic gate can be done in two parts. First, multiplier unit, where a conventional multiplier is replaced by Vedic multiplier using Urdhava Triyagbhayam sutra. Multiplication is the fundamental operation of MAC unit [1]. Power consumption, dissipation, area, speed and latency are the major issues in the multiplier unit. So, to avoid them, we go for fast multipliers in various applications of DSP, networking, etc. There are two major criterion that improve the speed of the MAC units are reducing the partial products and because of that accumulator burden is getting reduced. The basic operational blocks in digital system in which the multiplier determines the critical path and the delay. The (log2N + 1) partial products are produced by 2N1 cross products of different widths for N*N. The partial products are generated by Urdhava sutra is by Criss Cross Method. The maximum number of bits in partial products will lead to Critical path.

The second part of MAC is Reversible logic gate. In modern VLSI, fast switching of signals leads to more power dissipation. Loss of every bit of information in the computations that are not reversible is kT*log2 joules of heat energy are generated, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. In recent years, reversible logic functions has emerged and played a vital role in several fields such as Optical, Nano, Cryptography, etc

3. DESIGN OF MAC ARCHITECTURE

The design of MAC architecture consists of 3 subdesigns.

- Design of 32×32 bit Vedic multiplier.
- Design of adder using DKG gate reversiblelogic.
- Design of accumulator which integrates bothmultiplier and adder stages.

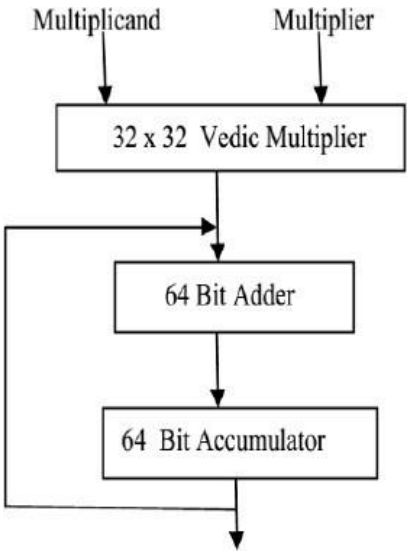


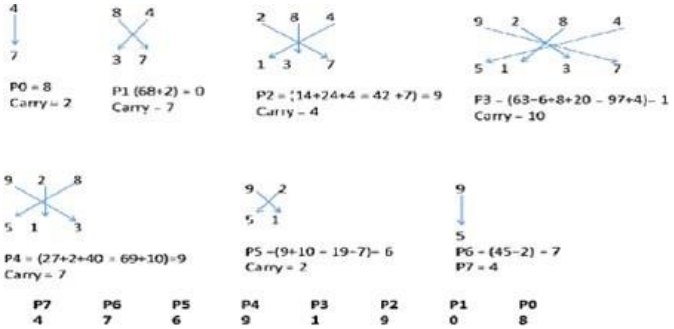
Fig: Modified MAC Architecture

32 x 32 bit Vedic Multiplier:

Vedic mathematics is an ancient system of mathematics, which was formulated by Sri Jagadguru Swami Bharati KrishnaTirthaji (1884 - 1960). After a research of eight years, he developed sixteen mathematical formulae from AtharvanaVeda[11]. The sutras (aphorisms) covered each and every topic of Mathematics such as Arithmetic, Algebra, Geometry, Trigonometry, differential, integral, etc., The word "Vedic" is derived from the word "Veda" which means the power house of all knowledge and divine [2, 3]. The proposed Vedic multiplier is based on the "Urdhava Triyagbhayam" sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we will utilize similar techniques to solve the binary number system to make the new aphorism, which will be more compatible for the digital systems. Itis a general multiplication formula applicable to all cases of multiplication

URDHAVA TRIYAGBHAYAM SUTRA:

It literally means "Vertically and Crosswise". Shift operation is not necessary because the partial product calculation will perform it in a single step, which in turn saves time and Power. This is the main advantage of the Vedic multiplier. An example for the Urdhva Triyagbhayam sutra is as follows:9284 * 5137



4. IMPLEMENTATION OF VEDICMULTIPLIER USING MODEL ARCHITECTURE IN DESIGN:

The following fig. 2 shows the design of a 16×16 Vedic multiplier using an 8×8 Vedic multiplier and the design can be implemented using Verilog HDL. Using a 16×16 Vedic multiplier we can design 32 ×32 Vedic multiplier with carry save adder as shown in fig. We have modified the final adder stage with the Kogge stone adder which is more efficient than the Carry save adder which is shown in the fig. By using the Vedic multiplier we can achieve lesser partial products as the table shows that the multiplier and adder stages for Vedic multiplier for higher bit are lesser as compared to the conventional multiplier. The multiplier designhas been simulated and synthesizedusing Xilinx.

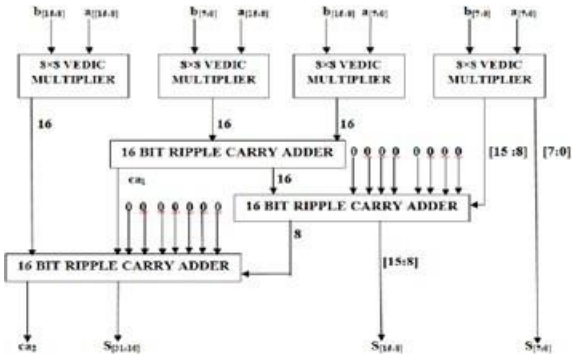


Fig : 16×16 Vedic multiplier using 8×8 Vedicmultiplier

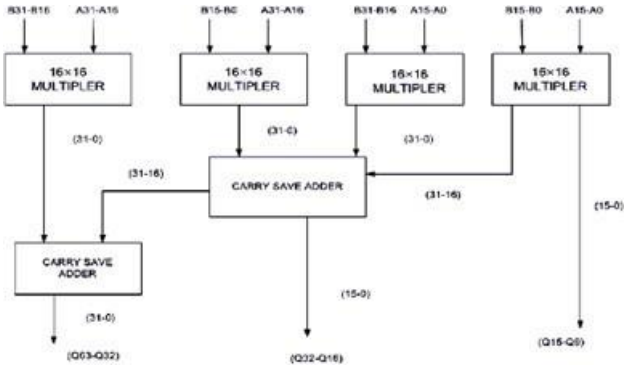


Fig : 32 × 32 Vedic Multiplier with Carry saveAdder

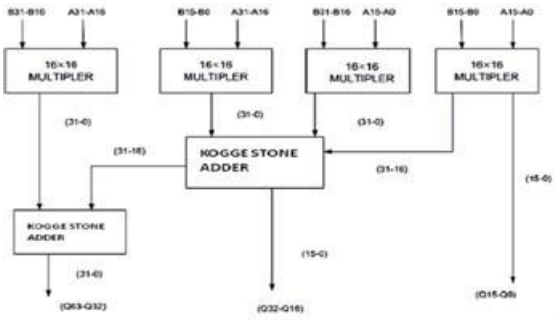


FIG: 32 × 32 VEDIC MULTIPLIER WITH KOGGE STONE ADDER

5. RESULTS:

RTL SCHEMATIC:

The RTL schematic is abbreviated as the register transfer level it denotes the blue print of the and is used to verify the designed architecture to the ideal architecture that we are in need of development. The hdl language is used to convert the description or summeryof the architecture to the working summery by use of thecoding language i.e verilog ,vhdl. The RTL schematic even specifies the internal connection blocks for better analyzing .The figure represented below shows the RTL schematic diagram of the designed architecture.

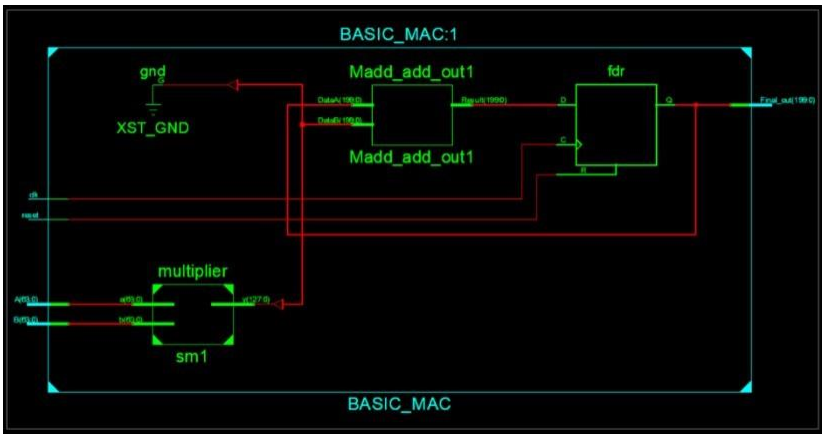


Fig: RTL Schematic of Basic MAC

TECHNOLOGY SCHEMATIC:

The technology schematic makes the representation of the architecture in the LUT format where the LUT is consider as the parameter of area that is used in VLSI to estimate the architecture design .the LUT is consider as an square unit the memoryallocation of the codeis represented in there LUT s in FPGA.

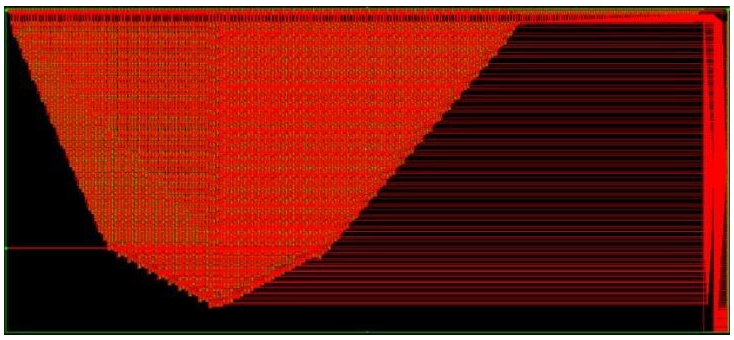


Fig :View Technology Schematic of Basic MAC

6. CONCLUSION

The results obtained by the design of Vedic multiplier with 32 bits and reversible logic are quite good. The work presented is based on 32 – bit MAC unit with Vedic Multipliers. We have designed MAC unit basic building blocks and its performance has been analyzed for all the blocks. Therefore, we can say that the Urdhava Triyag bhayam sutra with 32-bit Multiplier and reversible logic is the best in all aspects like speed, delay, area and complexity as compared to other architectures which are shown in table 2. Many researchers are reconfiguring the structure of MAC unit, which is the basic

block in different designs and aspects especially using reversible logic which evolves recent days. Spectrum Analysis and Correlation linear filtering which are the applications of transform algorithm further add to the field of communication, signaland image processing and instrumentation, and some other. Combining the Vedic and reversible logic will lead to new and efficient achievements in developing various fields of Mathematics, science as well engineering.

7. REFERENCES

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