International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 04 Issue: 04 | April -2020 ISSN: 2582-3930

IMPLEMENTATION OF 32-BIT CARRY LOOK AHEAD ADDER FOR FAST ADDITION

Mrs. D. Bhavani[1], N.Karthik[2], P. Blessy Mounika[3] , P. Padma Sriya , S. Sanath Kumar

[1]ECE, Asst. professor&SRKR Engineering College
[2]ECE, B. Tech Student&SRKR Engineering College
[3]ECE, B. Tech Student &SRKR Engineering College
ECE, B. Tech Students& SRKR Engineering College

ABSTRACT:

A carry-look ahead adder improves speed by decreasing the speed required to decide the carry bits. It can be contrasted with simpler, ripple carry adder for which the carry bit is calculated along the sum in it and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bit. The carry look ahead adder ascertains at least one carry bits before the whole, which decreases the hold up time to figure the after effect of the bigger bits.This adder model presents the design method and simulation strategy of a 32 bit Carry look ahead adder using VerilogHDL. The Simulation results are then introduced.

KEYWORDS:

Carry Look Ahead Adder, Verilog HDL, Carry generate, Carry propagation, FGPA, Computation time.

1. INTRODUCTION

Carry propagation delay is significant factor for structuring adders. The 32-bit adders are actualized using 16-bit adders. The 16-bit adders are implemented using 8-bit adders. The 8-bit adders are implemented using 4-bit adders. There are four type of adders. They are the Ripple carry adder, carry look ahead adder, Carry select adder and the Carry skip adder. Every adder has various systems to create output carry. Therefore every adder has distinctive carry propagation delay. The lower bits adder output carry is the input carry of upper bits adder. Therefore the lower bits adder ought to lessen the carry propagation delay.

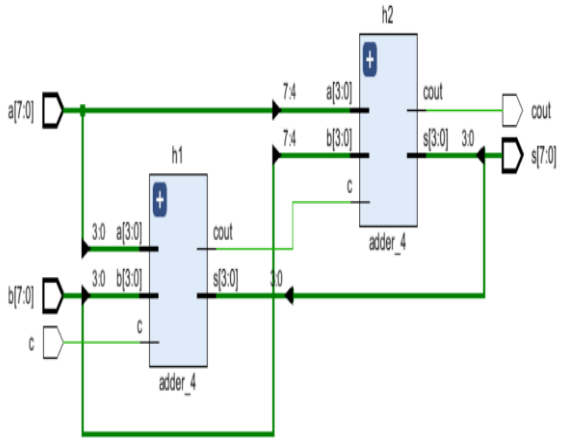

Fig.1 8 Bit Schematic Diagram

Fig.4 16 Bit Wave Form

Fig.2 8 Bit wave forms

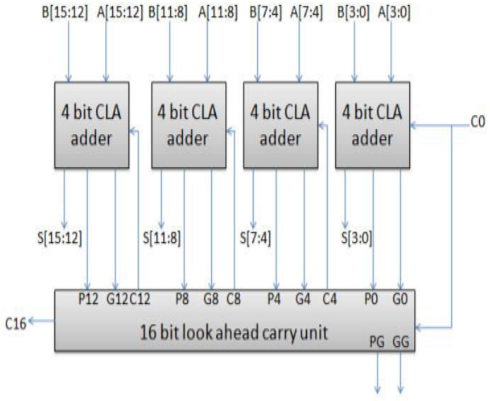

Fig.3 16 Bit CLA Adder

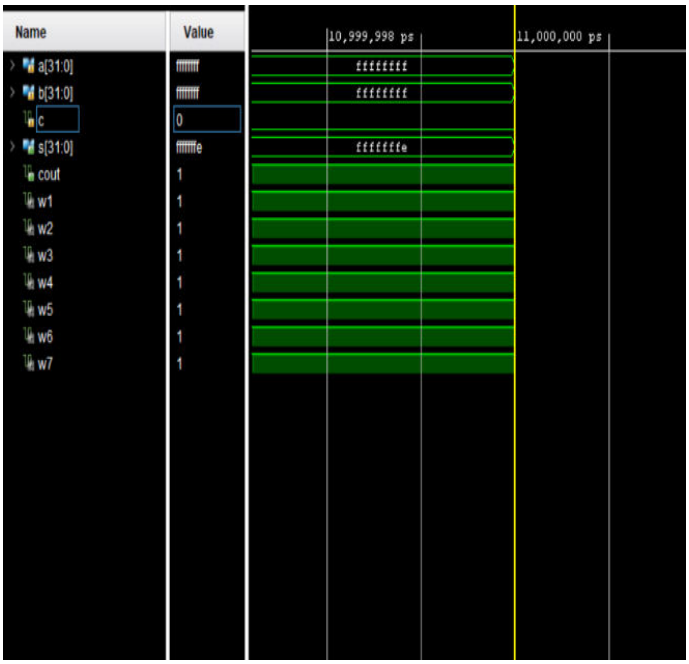

Fig.5 32 Bit Wave form

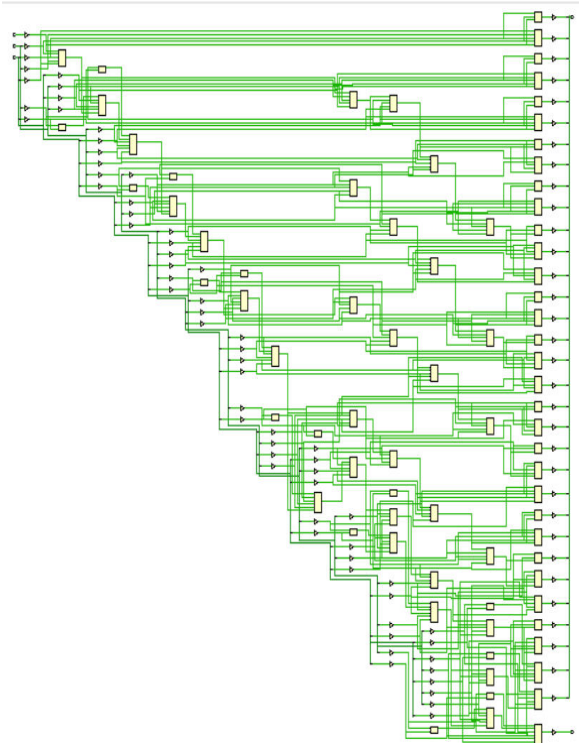

Fig.6 32 Bit Schematic

2. DELAY ESTIMATION IN BASIC ADDER UNITS:

Delay estimation is the fundamental operation in any digital system. The propagation time is more likewise because of huge time required for the carry bits. A carry look ahead adder improving the speed by lessening the time required to comprehend carry bits. It is mostly used in electronic devices. The performance of the CLA is measured. VLSI technology is used where we can design complex system like analog or digital circuit on a single chip. In devices for laptops and cellphones, power consumption has become a major concern in designing. Because of constrained force, the hardware included must be structured with the end goal that they expend less force since enormous force utilization requires costly cooling hardware. Expansion is the broadly utilized math activity and further more tedious. Expansion is the spread constraining element to processors. As far as we are concerned with high performance and the speed of the process, we have to increase the speed of the addition. In fast adder,the essential guideline of CLA adder is predominant, just the deferral of carry can be improved. Carry look ahead adder speed is normally controlled by the most minimal carry path delay. Its way is information subordinate.Basic carry look ahead principle is developed by Weinberger and Smith. In look ahead adder, the carry is generated in parallel by using look ahead carry circuit. Look ahead carry circuit contains two level AND-OR circuit. The basic logic gates used in this CLA adder are Exclusive OR gate, AND gate and OR gate.

3.TECHNOLOGIES USED:

The integration of FPGA and and all the small devices will be integrated by using Very Large Scale Integration(VLSI).

The code is written in Verilog HDL design pattern and synthesis is done in XILINX of version 2017.2.

Verilog HDL is used in programmable logic design and verification of digital circuits at the register transfer level of abstraction. A Verilog design consists of hierarchy of modules. Modules encapsulate design hierarchy and communicate with other modules through of set declared input, output, and bidirectional ports.

Xilinx ISE(Integrated Synthesis Environm-ent) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling

the developer to synthesize their structures, perform timing examination, look at RTL charts, mimic a plan's response to various boosts and arrange the objective gadget with the programmer . Xilinx ISE is a plan situation for FPGA items from Xilinx , and is firmly coupled to the engineering of such chips, and can't be utilized with FPGA items from different merchants.

4.CONCLUSION:

The 32-bit carry look ahead adder designed has less delay and less power consumption and memory consumption is very low.Thou-gh compared with other different logic design approaches carry look ahead adder employed the great importance to reduce carry propagation delay of the adder.

REFERENCES:

1.https://en.wikipedia.org/wiki/Application-specific_integrated_circuit

2.IEEE Standard Hardware Description Language Based on the Verilog Hardware Description LanguageIEEE Computer Society, IEEE, Network, NY, IEEE Standard 1364-1995

3.IEEE Standard Verilog Hardware Descr-iption Language, IEEE Computer Society , IEEE, New York , IEEE Standard 1364-2001

4.S.Brown and Z. Vramesic, "Fundamental of Digital Logic with Verilog Design", McGraw Hill, USA, ch.8,2003