International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 09 Issue: 04 | April - 2025 SJIF Rating: 8.586 ISSN: 2582-3930

Implementation of Dual-Use Power Lines to Improve Testability in CMOS Receiver Systems

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Abstract

Power Line Communication (PLC) integrates the power distribution network and data communication over the same infrastructure, enabling efficient transmission of data. In this system, the power pins and the power distribution networks of ICs are used for both power delivery and data communication.

To facilitate the necessary communication across various nodes in an integrated circuit (IC), receivers are installed at each node or testing point within the system.

However, a significant challenge arises as the existing PLC receivers consume excessive power, which impacts the overall system efficiency, especially in energy-sensitive applications. To address this issue, We introduces the design of a power-efficient CMOS-based PLC receiver, implemented using the Tanner Tool.

I. INTRODUCTION

The increasing complexity of modern communication systems has led to a growing need for efficient and reliable testing methodologies. In CMOS receiver systems, testability is a significant challenge due to the limited accessibility of internal nodes. Traditional testing approaches often require additional test circuitry, which can increase area overhead, power consumption, and design complexity.

To address these challenges, this paper proposes the implementation of dual-use power lines to improve testability in CMOS receiver systems. By leveraging the existing power distribution network, we can repurpose power lines as test access mechanisms, eliminating the need for dedicated test circuitry. This approach not only reduces area overhead and power consumption but also enhances test coverage and fault diagnosis capabilities

LITERATURE SURVEY :

To the best of our knowledge, we are the only group who reported the works on PLC in ICs in [1] and [21]–[29]. Our group proposed PLC in ICs to reduce the pin count, size, and hence the cost of a chip initially [21] and later to increase the channel capacity for the multiple parallel scan design in [1]. To follow up the proposal, we investigated several relevant topics for PLC in ICs, and reviewed them briefly as follows. We measured the propagation loss from a core power supply pin to an onchip node of a PDN of a cold Pentium 4 die (65 nm version) [24]. The largest passband was observed ~2 GHz over a 200-MHz band, and the path loss increases above 40 dB beyond 2.5 GHz. Other measurements were carried out on three different samples of cold 45-nm Core 2 Duo processors and two randomly picked locations on the PDNs [28]. The averaged transfer function shows narrow sporadic passbands, where about 5% ~ 7% of the input signal passes through the PDN. We observed that there is little correlation between the passbands of the 65 nm Pentium 4 and that for the 45-nm Core 2 Duo processors. We suggested the use of ultrawideband (UWB) and direct-sequence code division multiple access (DSCDMA) communication technologies to circumvent the blocking of data signals in low frequencies at packages and PDNs and increase the SNR [21], [22], [25]. Compared with the traditional narrow-band communication systems, UWB signaling has several advantages, such as high data rate, low average power, and simple RF circuitry [31]. Shannon's

theorem states that the channel capacity is given as $B \times \log2(1 + SNR)$, where B is the bandwidth [32]. As the bandwidth is much larger (on the order of several gigahertz) for UWB than a narrow-band signal, the SNR can be much smaller for UWB to achieve the same data rate. The DS-CDMA technology

Applications:

- Improved IC Testability: Makes it easier to test CMOS receiver circuits without adding extra testing circuitry.
- Low-Power, High-Reliability Systems: Useful in systems where power efficiency and fault detection are critical (e.g., aerospace, medical devices).
- Automotive Electronics: Advanced Driver-Assistance Systems (ADAS), infotainment, and control units, where reliability is a must.
- Medical Devices: Implantable or wearable devices where size and safety are crucial.
- Telecommunications: In CMOS-based RF receivers and signal processors for error detection and maintenance.
- Aerospace and Defense: Satellites, drones, and radar systems that require high-reliability and self-diagnostic capabilities.

Advantages of: Implementation of dual-use power Lines to improve testability in CMOS Receiver systems

1. Reduced Wire Count: Using power lines for communication reduces the number of wires required, saving space and weight.
2. Space Efficiency: Traditional testing setups often require additional space for test pads, dedicated test circuits, or separate test equipment. By using dual-use power lines, space is saved, as the power lines are already part of the system and can simultaneously handle testing. This is especially useful in systems where space is limited or in embedded systems with strict space constraints.
3. Reduction in Wiring Complexity : Traditional systems often require separate wiring for power delivery, data communication, and testing. Dual-use power lines consolidate these functions, reducing the complexity of the wiring in the system.

4.Reducing pin count.

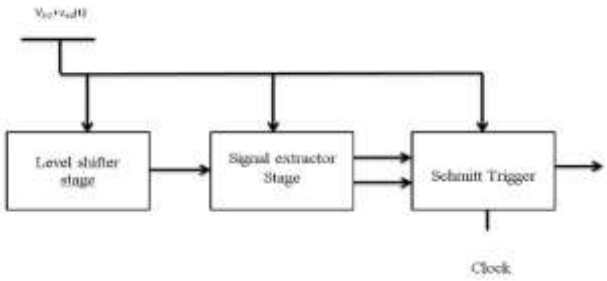
I. Proposed System:

- First block is a level shifter, which lowers the dc level of the signal superimposed on the supply voltage.

The level shifted signal is processed by the subsequent block,

- a signal extractor, which amplifies the signal and converts it to a differential signal. The input signal of the signal extractor is the data signal offset with 0.5 *V*DD, and the signal extractor amplifies the data signal while removing the dc offset voltage.
- The Schmitt Trigger translates the data in the form of analog differential signal into digital signals, and give A AND A'.

Block Diagram :



REQUIREMENTS/ SOFTWARE USED

- Tanner tool
- Windows OS 7/8/10/11
- RAM: minimum 4GB
- Hard disk: 128GB

II. ADVANTAGES

- Cost Efficiency
- Enhanced Signal Access
- Decrease Complexity circuit
- Avoiding of over heating
- Reduced Wire Count

I. CONCLUSION :

The proposed PLC receiver was designed and fabricated in CMOS 0.18 µm technology. In this paper, we presented the feasibility for dual use of power pins, data communications as well as its intended purpose of delivery of power, based on the ultra wideband communication technology and the direct-sequence code division multiple access scheme. Our simulation results indicate that the proposed approach is quite feasible and

can be applied to existing packages without or little modification. Further research including design of data recovery blocks and determination of various design parameters is necessary to deploy the proposed method to real world chips

RESULT :

1. Successful Enhancement of Testability

- The CMOS receiver circuit can now be more thoroughly tested at **both wafer-level and system-level** without adding extra hardware.
- Internal analog and digital nodes become **accessible** for stimulus and observation via shared power lines.

2. Reduction in Test Infrastructure Overhead

- **No additional test pads or routing** required.
- Reuse of power lines leads to **lower area overhead** and simplified physical design.
- **Fewer external test resources** are needed (less complex test benches or probe stations).

3. Improved Fault Coverage

- Detection of **hard-to-catch defects**, including:
  - Subtle process variations
  - Intermittent faults
  - Leakage paths
- Improves the **defect detection rate** in both pre-silicon simulation and post-silicon validation.

4. Better Debugging and Validation

- Faster and more accurate debugging process.
- Shorter time to isolate functional or performance issues.
- Helps in **early silicon bring-up** and debugging during chip prototyping.

5. Increased Production Yield and Reliability

- By detecting more faults early, **bad chips are screened out** before final packaging.
- This leads to:
  - Higher overall **yield**
  - Fewer **RMA (Return Merchandise Authorization)** issues in the field
  - Improved **customer trust and product quality**

6. Successful Demonstration/Validation

- A proof-of-concept or prototype implementation confirms:
  - Dual-use line integration works without impacting normal operation.
  - No significant power delivery or signal integrity issues are introduced.

II. REFRENCES :

[1] H.C. Ferreira, H.M. Grove, O. Hooijen, and A.J. Han Vinck, “Power line communications: An overview,” Proc. IEEE 4th AFRICON, vol. 2, Stellenbosch, South Africa, pp.558-63, September 2014.

[2] H. Meng et al., “Modeling of transfer characteristics for the broadband power line communication channel,” IEEE Trans. Power Delivery, vol. 19, no. 3, pp.1057-64, July 2017.

[3] Special issue on ultra-wideband radio in multiaccess wireless communications, IEEE Journal on Selected Areas in Communications, vol. 20, no.9, December 2002

[4] R.E. Ziemer, R.L. Peterson and D.E. Borth, Introduction to Spread Spectrum Communications, Prentice Hall, 2020.

[5] H.B. Bakoglu, Circuits, Interconnections, and Packaging for VLSI, Addison-Wesley Publisching Co., 2021.

[6] T. Sakurai, “Approximation of wiring delay in MOSFET LSI,” IEEE Journal of Solid-State Circuits, vol. sc-18, no.4, pp. 418-26, August 2018.

[7]http://www.amkor.com/Products/all_datasheets/flexbga.pdf, as of October 2020.

[8] M. Horowitz and R.W. Dutton, “Resistance extraction from mask layout data,” IEEE Trans. on CAD of Integrated Circuits and Systems, vol. 2, no. 3, pp. 145-50, July 2018.

[9] H. H. Chen and J. S. Nealy, “Interconnect and circuit modeling techniques for full-chip power supply noise analysis,” IEEE Trans. Comp., Pkg., Mfg. Tech. (CPMT) – Part B, vol. 21, no. 3, pp. 209- 215, Aug. 2016.