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Implementation Of Low Power and High Speed Dadda Multiplier Using XOR-XNOR Cell Based Hybrid Logic Full Adder Using Power Gating NMOS

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Abstract – In this paper**,** Digital multipliers are very important for the performance of VLSI systems. However, traditional designs like array multipliers suffer from high delay due to carry propagation and also consume more power. To overcome these problems, this paper presents the design of an optimized 8-bit Dadda multiplier that improves both speed and power efficiency. In this design, the conventional CMOS full adders are replaced with hybrid logic full adders based on XOR-XNOR cells. This change helps to reduce logic levels, internal capacitance, and switching activity, which directly improves the speed of operation. As a result, the generation of sum and carry becomes faster. To further reduce power consumption, an NMOS power gating technique is used. A sleep transistor is placed between the logic circuit and ground to reduce leakage current when the circuit is idle. This helps in minimizing static power dissipation. The proposed design is implemented and simulated using Cadence tools. The results are compared with a conventional Dadda multiplier, and significant improvements are observed. The propagation delay is reduced by 55.7%, from 740.0 ps to 327.3 ps, showing a clear increase in speed. Similarly, the total power consumption is reduced from 1.03 mW to 998.7 µW, improving overall efficiency. Although there is a small increase in area, with the transistor count increasing from 1744 MOS to 1752 MOS, the performance improvements in speed and power make it acceptable. Finally, the proposed multiplier offers a good balance between high speed, low power, and area, making it suitable for applications such as digital signal processing, image processing, and battery-operated embedded VLSI systems.

Key Words: NMOS Power Gating, Leakage Power, Propagation Delay, VLSI Arithmetic, Xor-Xnor cell

1. INTRODUCTION

Multipliers play a key role in determining the speed and energy efficiency of modern digital signal processing (DSP) and VLSI systems. Traditional array multipliers are simple in structure, but they suffer from large delays because partial products are added one after another. They also consume more dynamic power, which reduces overall efficiency. To overcome these problems, tree-based structures like the Dadda multiplier are used, as they reduce the number of computation stages and improve speed. However, when these structures are implemented using standard CMOS full adders, they still face issues such as higher logic complexity, more transistor usage, and increased leakage power, especially in deep submicron technologies. In this paper, an optimized 8-bit Dadda multiplier is proposed to reduce both delay and power consumption. The design replaces conventional full adders with hybrid logic full adders based on XOR-XNOR cells. This modification helps to shorten the critical path and reduce internal switching capacitance, which improves the overall speed of the circuit. In addition, an NMOS power gating technique is used to reduce static power consumption. A sleep transistor is introduced to control leakage current during idle conditions without affecting the performance during active operation.

2. LITERATURE SURVEY

Radhakrishnan minimized [1] short-circuit power for portable VLSI, laying the groundwork for low-power adders. Chang and Zhang reviewed 0.18-µm adders, [2] exposing standard CMOS limitations in deep-submicron tree multipliers. Valashani and Mirzakuchaki built a compact XOR-XNOR cell [3] that cuts internal capacitance and delay. Naseri and Timarchi combined [4] new XOR/XNOR gates to reduce static/dynamic power and suppress glitches. Tomar and Kandpal [5] designed an 18-transistor hybrid adder utilizing transmission gates to improve robustness. Chandrakasan and Sheng established [6] fundamental power-reduction theories via voltage and capacitance scaling. Zimmermann and Fichtner compared [7] CMOS with pass-transistor logic, noting pass-transistors offer speed but suffer voltage

degradation. Prem Kumar and Duraiswamy proved [8] genetic algorithms can automate and optimize transistor sizing for arithmetic circuits. Aguirre-Hernandez and Linares-Aranda [9] simplified logic expressions in CMOS adders to lower the power-delay product. Foroutan and Taheri engineered low-power [10] cells by merging GDI structures with hybrid CMOS logic. Vesterbacka implemented [11] a 14-transistor full adder capable of maintaining full voltage-swing nodes. Tung and Shieh tailored a [12] high-speed, low-power full adder specifically for portable electronics. Singh and Parveen Kumar analyzed delay in 32-bit array multipliers using carry-save [13] and carry-lookahead adders.

3. EXISTING METHODOLOGY

The conventional array multiplier is commonly used as a basic reference design. It works using a simple shift-and-add method to generate and add partial products step by step. Although its regular structure makes it easy to design and implement, it is not suitable for high-performance systems. This is because it suffers from large carry propagation delays, uses more chip area, and consumes high dynamic power. Other options like sequential and serial multipliers reduce hardware complexity by processing bits one at a time. However, this makes them very slow, so they are not useful for high-speed applications. Improve speed, the Dadda multiplier uses a parallel tree-based reduction method. It reduces partial products in multiple stages using half adders and full adders, followed by a final addition stage. This approach improves speed compared to the array multiplier. The existing Dadda multiplier still has some limitations. It uses standard CMOS full adders, which increase power consumption (both dynamic and leakage). It also has longer logic paths, which increase propagation delay, and requires more silicon area. In summary, although the Dadda multiplier is faster than the array multiplier, its use of conventional full adders makes it less efficient in terms of power and area. Therefore, it is not the best choice for modern low-power and high-performance VLSI systems.

Limitations: Higher Power Consumption, Increased Propagation Delay, Higher Leakage Power, Increased Heat Generation, Larger Area Requirement

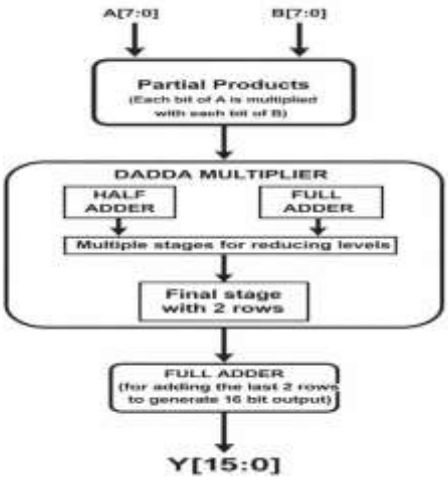

Fig. 1: Block Diagram of Dadda Multiplier

Fig. 4.1 represents an 8×8 Dadda Multiplier, where two 8-bit inputs A [7:0] and B [7:0] are multiplied to produce a 16-bit output Y [15:0]. First, the inputs A and B are given to the Partial Product Generation block. In this stage, each bit of A is multiplied with each bit of B using AND operations, generating multiple partial products arranged in columns. These partial products are then passed to the Dadda Multiplier block, where reduction takes place. Inside this block, Half Adders and Full Adders are used to reduce the number of bits in each column. This reduction is done in multiple stages, following the Dadda algorithm, to minimize the number of rows efficiently. After completing the reduction process, the partial products are reduced to two final rows, known as the final stage. Finally, these two rows are given to a Full Adder (final adder stage), which adds them together to produce the final 16-bit output Y [15:0].

4. PROPOSED METHODOLOGY

The proposed method focuses on designing an optimized 8-bit Dadda multiplier to reduce delay, area, and power consumption found in conventional array multipliers. This is achieved by using a parallel tree-based reduction structure combined with XOR-XNOR hybrid full adders and an NMOS power gating technique. The multiplication process starts with partial product generation. An array of AND gates is used to multiply two 8-bit inputs, producing a total of 64 partial products. These partial products are then processed in the Dadda reduction stage. Unlike array multipliers, which add rows one by one, or Wallace tree multipliers, which reduce all rows aggressively at every stage, the Dadda multiplier follows a controlled reduction approach. It reduces the number of bits in each column based on predefined limits such as 2, 3, 4, 6, and 9. This method ensures that only the minimum number of adders is used. As a result, hardware complexity, wiring, and delay are reduced

before the final addition stage, where a fast carry-propagate adder is used. A key improvement in this design is the replacement of conventional CMOS full adders with XOR-XNOR based hybrid full adders. Traditional full adders have longer logic paths and higher internal capacitance, which increases delay and power consumption. The XOR-XNOR design simplifies the internal structure, reduces unnecessary switching, and lowers capacitance. This helps to generate sum and carry outputs faster while also reducing dynamic power usage. To further improve power efficiency, an NMOS power gating technique is applied. A high-threshold NMOS sleep transistor is placed between the logic circuit and ground. During active operation, the transistor remains ON, allowing the circuit to function normally. During idle conditions, it is turned OFF, which cuts the leakage current and reduces static power consumption. The combined effect of these improvements results in significant performance enhancement. The propagation delay is reduced from 740.0 ps to 327.3 ps, and the total power consumption decreases from 1.03 mW to 998.7 µW. This is achieved with only a very small increase in area, where the transistor count increases by just 8 MOS transistors compared to the existing design. Overall, the proposed methodology provides a fast, power-efficient, and area-optimized solution, making it suitable for modern VLSI applications such as digital signal processing and embedded systems.

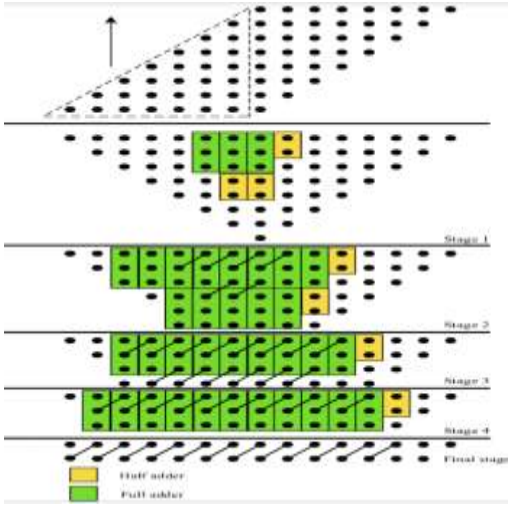

Fig. 2: Algorithm of Dadda Multiplier

Fig. 2 shows the algorithm of the Dadda multiplier mainly consists of three stages. In the first stage, partial products are generated using AND gates, where each bit of one input is multiplied with the corresponding bits of the other input. In the second stage, these partial products are reduced using compressors, half adders, and full adders in a structured manner. This reduction process converts multiple rows of partial products into fewer rows, which helps in minimizing delay. In the final stage, the reduced rows are added using a carry propagation adder to produce the final multiplication result. Overall, this algorithm reduces hardware area, improves speed, and lowers power consumption, making it suitable for high-performance VLSI applications.

5. RESULTS

Comparison between Existing and Proposed Dadda Multiplier

Table 1: Performance Comparison — Existing and Proposed

Parameter	Dadda Multiplier	Power Gating Dadda Multiplier
Power consumption	1.03 mW	998.7 µW
MOS Count	1744	1752
Delay	740.0 ps	327.3 ps

6. DISCUSSION

The simulation results show a clear difference between speed improvement and power reduction. The proposed XOR-XNOR based architecture is highly effective in improving speed. The propagation delay is reduced by 55.7%, decreasing from 740.0 ps to 327.3 ps, which confirms that the hybrid logic design successfully shortens the critical path. However, the improvement in power consumption is relatively small. The total power is reduced from 1.03 mW to 998.7 µW, which is approximately a 3% reduction. This indicates that the NMOS power gating technique provides only limited power savings and mainly compensates for the slight increase in hardware. The proposed design uses 1752 MOS transistors, compared to 1744 MOS in the conventional design, resulting in a very small increase in area. Despite this, the power consumption does not increase, which is a positive outcome. Overall, the proposed multiplier can be clearly described as a speed-optimized design. It achieves significant delay reduction with only a negligible increase in area, while maintaining nearly the same power consumption. This makes it a strong and practical solution for applications where high speed is more critical than minor power savings.

7. CONCLUSION

This work presents an optimized 8-bit Dadda multiplier designed to improve the performance of VLSI systems. By combining the Dadda partial product reduction method with XOR-XNOR based hybrid full adders and an NMOS power gating technique, the proposed design achieves significant improvements in speed with controlled power consumption. The simulation results show that the propagation delay is reduced from 740 ps to 327.3 ps, which is a major improvement in performance. The total power consumption is also slightly reduced from 1.03 mW to 998.7 µW, while maintaining a minimal increase in area from 1744 to 1752 MOS transistors. These improvements are mainly due to reduced switching activity, lower internal capacitance, and effective leakage control.

Overall, the proposed design can be considered a speed-optimized multiplier, as it provides a large reduction in delay with only a small impact on power and area. This makes it suitable for high-speed applications such as digital signal processing, image processing, and embedded VLSI systems. In future work, the design can be extended to higher bit-width multipliers, advanced technologies, and improved compression techniques to further enhance performance and scalability for modern low-power applications.

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