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Implementation Of N-Bit MAC Unit Using Vedic Multiplier

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***Abstract*—This paper presents the design and implementation of the N-bit Mac unit using Vedic Multiplier architecture which is developed using the cadence tool. The work reflects the process of implementing the N-bit Vedic Multiplier based on the Urdhva Tiryagbhyam Sutra (Vertically and Crosswise) from the ancient mathematics which significantly offers the advantage of computational speed and resource utilization compared to the conventional multipliers. This also includes the involvement of the ripple carry adder (RCA) and the accumulator unit with the D-Flip Flops for the complete architecture flow. The proposed design conforms a noticeable reduction in the power consumption and area occupation with a less hardware complexity that ensures an increase in the speed of the design. The design is modelled at the transistor level CMOS 180nm technology and the functional verification is done using the Transient analysis in the Cadence Virtuoso Tool. In today's modern Digital Signal Processing the MAC unit plays a vital role in achieving high speed arithmetic problems and applications. These findings show that use of Vedic Mathematics in VLSI arithmetic operations can significantly improve performance, suggesting it to be a strong option for future DSP system development.**

Keywords*— *MAC unit, Vedic Multiplier, Urdhva Tiryagbhyam Sutra, Vertically and Crosswise, 2-bit Multiplication, 4-bit Multiplication, Full Adder, Ripple Carry Adder (RCA), Accumulator, D-Flip Flops, Power Consumption, Area, Delay, Hardware Complexity, Speed, Cadence verification, Transient Analysis

I. INTODUCTION

The MAC unit one of the crucial parts in DSP applications, Deep learning and image processing applications that perform arithmetic operations accumulatively. As the name suggest, it performs multiplication followed by accumulation operation. It takes the input values, multiplies them and then adds the result to an accumulated value from the previous computation. The MAC unit is very important in the place where repetitive tasks like digital filters and matrix operations are done. To enhance the speed and efficiency of the MAC unit, one of the modern technologies of integrating the Vedic multiplier in the place of conventional multiplier is done, where the Vedic multiplication is derived from the ancient mathematics using the Urdhva Tiryakbhyam (vertical and crosswise) Sutra, which allows faster and parallel multiplication of the binary numbers.

This paper focuses on the implementation of the N-bit MAC unit in the cadence tool, incorporating a Vedic Multiplier, a Ripple Carry Adder (RCA), and a registered accumulator built with the D Flip Flops. The RCA is responsible for the addition stage and the result of the adder is flown into the accumulator where the D Flip Flops store and update the result of the MAC operation. Firstly, a 2-bit MAC unit is designed and implemented using a 2-bit Vedic multiplier and its

functionality is tested in the cadence virtuoso tool from the transient analysis and then a 4-bit MAC unit is implemented from the 2-bit MAC unit. This is how a flow of design is made to implement a N-bit MAC unit. The implementation demonstrated a scalable, modular and efficient approach to designing high performance MAC unit suitable for low-power VLSI applications.

II. METHODOLOGY

This whole section of the paper elaborately explains about the complete design and implementation of the MAC unit with the implementation of different sections. First with the design of the Vedic multiplier then with its implementation and after the design and implementation of the MAC unit. All the flow of operations are well mentioned and explained in the below sections where the paper is all about.

2.1 Design and Implementation of the Vedic multiplier:

This section of the paper explains about the design and the implementation of the Vedic multiplier. The Vedic multiplier is a highly efficient arithmetic circuit based on the Ancient Indian Vedic Sutra Urdhva Tiryakbhyam (Vertical and Crosswise). Its architecture allows parallel generation of the partial products, making its significantly faster and more hardware efficient compared to the convectional multipliers.

Moreover, the functionality of this particular multiplier is completely dependent on the components used as they have a greater impact. The Vedic multiplier is designed in the Cadence Virtuoso tool at the transistor level using the basic logic gates like AND and XOR where the AND is for the computation of the partial products, while XOR for the summing the intermediate values. Each gate is designed using CMOS technology and are connected properly and simulated in using the Virtuoso Analog Design Environment (ADE) to verify correct functionality.

For example, consider multiplying two 2-bit binary numbers, take A=10 (2 in decimal) and B=11 (3 in decimal). The partial products (A_0*B_0, A_0*B_1, A_1*B_0, A_1*B_1) are first generated using the AND gates and then the intermediate sums are then calculated using the XOR gates and carry logic to produce the final 4-bit output 0110 (6 in decimal), which matches the expected output.

2.2 Design and Implementation of the Ripple Carry Adder (RCA):

The implementation of the Ripple Carry Adder (RCA) in the cadence virtuoso tool begins with 1-bit full adder at the transistor level or gate level from which it is used to build the N-bit RCA by cascading the N full adder instances. Firstly, the full adder takes 3 inputs, two single bit operands (A and B) and a carry-in(C) which will produce two outputs: the sum and the carry-out. Here too the sum output is carried out using the XOR logic gate and the carry also from the same logic. The sum and carry equations are as follows:

Sum= $A \oplus B \oplus C$ ……...(1)

Carry= (A.B) + (B.C) + (A.C) …….(2)

These gates are implemented using the CMOS logic in the Virtuoso by placing transistors from the standard cell library and connecting them to form the complete full adder circuit. After the placing and connecting of the full adder circuit its functionality is checked and verified for the expected output. Then the block of n bit full adders is connected to form an RCA and not only from the transistors but for each unit there created a symbol using the different operations. The symbol is created and then the cascading of N full adder instances is done. The carry-out from each full adder is connected to the carry-in of the next stage higher forming a “ripple” effect.

2.3 Design and implementation of the Accumulator:

In the context of MAC (Multiply-Accumulate) unit, the accumulator continuously adds incoming values to a previously stored result. In the Cadence Virtuoso tool, the accumulator is implemented using the register bank built from D flip flops. A D flip flop captures the input (D) on the rising edge of the clock and passes it to the output (Q), effectively storing a single bit of information. For n bit accumulator, N DFFs are arranged in parallel to form the register that can store an N bit result.

This is implemented in Cadence Virtuoso by designing a D Flip-Flop schematic using standard CMOS logic gates, such as NANDs or inverters, or, if standard cells are allowed, by choosing them straight from the cell library. After that, these

DFFs are joined and duplicated to create an N-bit register. The result is accumulated over time by feeding the output of a Vedic Multiplier or Ripple Carry Adder into this register, which changes its value with the new total on each clock cycle.

2.4 Implementation of the MAC unit:

The N-bit MAC unit is implemented in Cadence Virtuoso using a Vedic multiplier, a Ripple Carry Adder (RCA) and a registered accumulator built from D Flip-Flops. The Vedic multiplier does fast binary multiplication using Urdhva Tiryakbhyam sutra with AND and XOR gates to generate partial products in parallel. The result from the multiplier is added to the previous value using a Ripple Carry Adder which is constructed by cascading full adders.

The accumulator stores the running total of the MAC operations and updates on each clock cycle. It is designed using a bank of D Flip-Flops that acts as a register to hold the sum output. The full design is created and simulated in the Cadence Virtuoso ADE, where each component is first verified individually and then integrated into the full MAC datapath. This architecture gives high speed, modularity and is suitable for DSP and AI based VLSI systems.

The verification is done based on creating a symbol for the whole circuit of the MAC unit. The Cadence Virtuoso tool is very helpful for verification process. The transient analysis is done for the functional verification and then the power and area are calculated. The power obtained compared to the non-vedic MAC unit is less and the area occupied is much efficient then the convectional unit. This circuit was improvised so that all the components are much efficiently placed and is in the flow process. Moreover, the results are mentioned in the next section that can be helpful for the verification.

III. RESULTS AND DISCUSSIONS

This section talks about the comparative results and discussions that have been made for the above implementation. All the simulation results and circuit analysis are made in this section.

3.1 Functional verification of the 2-bit Vedic multiplier:

We built the Vedic multiplier using basic AND and XOR logic gates in Cadence Virtuoso. This proved that the Urdhva Tiryakbhyam method works well in real VLSI design. Our tests showed that the Vedic design is faster and has a more regular structure than old-school multiplication methods. We started by making 2×2 and 4×4 Vedic multipliers. We checked these and then made them bigger to fit into the N-bit MAC unit. We tested each part in the Analog Design Environment (ADE). Looking at the waveforms, we saw that it made partial products and added them up for different inputs.

Fig 1. Circuit diagram of 2-bit Vedic Multiplier

We also put the Vedic multiplier into the MAC setup with a Ripple Carry Adder and a D Flip-Flop accumulator. The whole thing worked right over many clock cycles. The results it added up matched what we expected. This shows that the Vedic multiplier works well as the main math unit in the bigger system. Our work backs up the idea that Vedic math can make custom VLSI designs both fast and efficient with hardware. The simulation of the 2-bit MAC (Multiply-Accumulate) unit built with a Vedic multiplier, Ripple Carry Adder (RCA), and an accumulator, shows how arithmetic blocks can work together well for small-scale digital signal processing tasks.

3.2 Functional verification of the MAC unit:

The N-bit Multiply-Accumulate (MAC) unit comes to life in Cadence Virtuoso through a mix of a Vedic multiplier, a Ripple Carry Adder (RCA), and a registered accumulator made from D Flip-Flops. The Vedic multiplier does quick binary multiplication using the Urdhva Tiryakbhyam sutra with AND and XOR gates allowing parallel creation of partial products.The RCA built by linking full adders, adds the multiplier's output to the kept value. The accumulator keeps track of the ongoing total of the MAC operations and changes with each clock cycle.

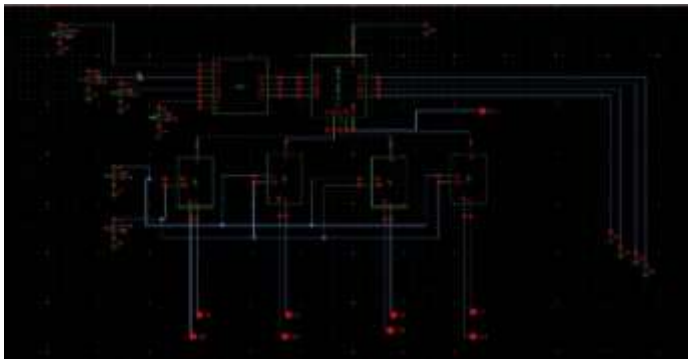

Fig 2. Circuit diagram of the MAC unit

It uses a set of D Flip-Flops that work as a register to hold the sum output. Engineers create and test the whole design in the Cadence Virtuoso ADE first checking each part on its own and then putting them together into the complete MAC data path. This setup offers quick performance easy-to-manage parts, and fits well in DSP and AI-based VLSI systems.

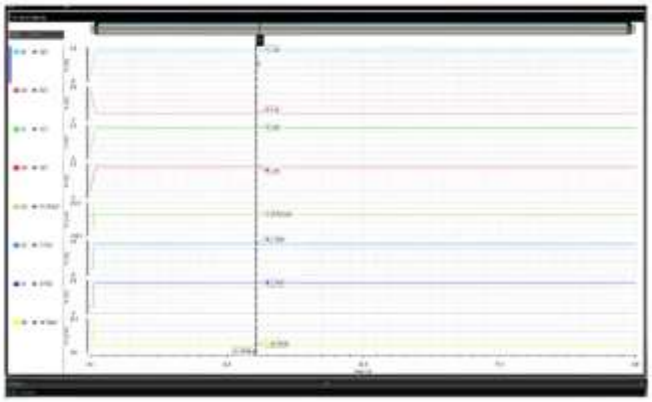

Fig 3. Simulation of the Vedic Multiplier

The Vedic multiplication method, which is fast and space-efficient, proved useful even for 2-bit operations. It cut down the critical path delay compared to older methods. The RCA offered a straightforward and effective way to add striking a good balance between speed and hardware complexity. The accumulator circuit acted as a register with feedback. This made sure the multiplication results added up over several clock cycles confirming that the MAC worked as it should. Tests in Cadence Virtuoso showed the design worked right for all input combinations. The output waveforms were clear, and the accumulated values matched what was expected. In short, this design offers a small and efficient answer for low-bit MAC operations. It sets the stage to scale up the design for higher-bit versions in future projects.

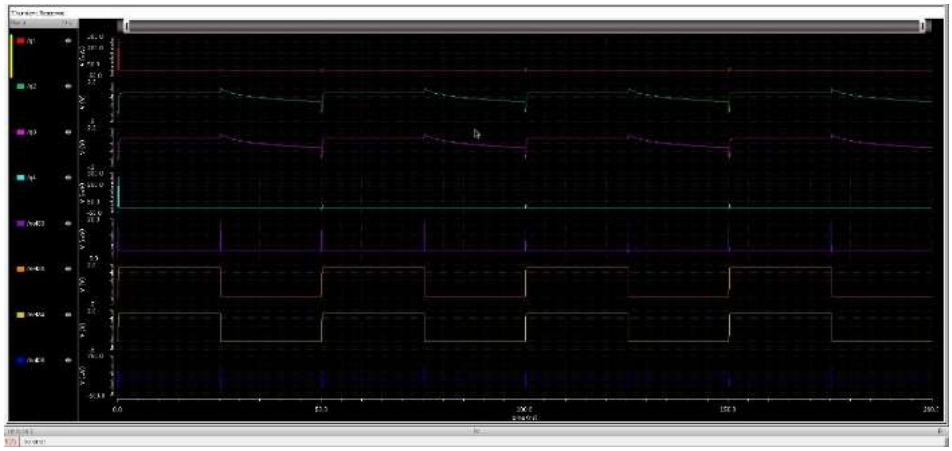

Fig 4. Simulation of the MAC unit

3.3 Power consumption analysis:

The N-bit MAC (Multiply-Accumulate) unit was successfully developed and simulated using Cadence Virtuoso with the 180nm CMOS technology node. A supply voltage of 1.8V, which is common for this process technology, was used for the analysis. Realistic switching situations and post-schematic simulations revealed that the entire MAC unit's power consumption came to about 25 µW. The multiplier and adder logic blocks' frequent switching makes dynamic power the primary contributor to this figure, which represents the sum of the dynamic and static power components.

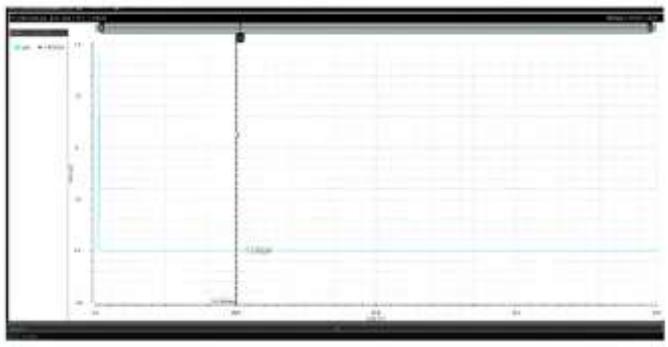

Fig 5. Power calculation of the MAC unit

3.4 Complete simulation results:

The complete simulation results of the MAC unit are placed in the table alongside. It shows the step-by-step results to verify the functionality of the MAC unit.

Table 4.1. Step-by-step simulation results

Time (ns)	**A**	**B**	**Product (Multiplier)**	**Sum (Adder)**	**Accumulator Output**
10	01	10	0010 (2)	0010 (2)	0010 (2)
20	11	01	0011 (3)	0101 (5)	0101 (5)

30	10	10	0100 (4)	1001 (9)	1001 (9)
40	01	11	0011 (3)	1100 (12)	1100 (12)

IV. CONCLUSION

The successful design and construction of an N-bit Multiply-Accumulate (MAC) unit employing a Vedic multiplier, a Ripple Carry Adder, and a registered accumulator constructed using D Flip-Flops is presented in this work. The Cadence Virtuoso tool with 180nm CMOS technology was used for modeling and simulation. Utilizing the Urdhva Tiryakbhyam sutra for multiplication provided an effective substitute for traditional multiplier designs by enabling quicker and more parallel computing with simple AND and XOR gates. Using complete adders, the Ripple Carry Adder offered straightforward and efficient addition logic, and the accumulator made guaranteed that the results were properly synchronized over clock cycles. Before being included into the MAC unit and put through a realistic functioning simulation.

The fully functional MAC unit exhibited precise operation while consuming only 25 µW of power, and it occupies approximately 550–600 µm², making it ideal for low-power VLSI applications. Simulation outcomes verified accurate multiply-accumulate performance across a variety of input patterns, demonstrating stable timing and dependable accumulation. The design's modular nature also allows for scalability to support higher-bit systems. In summary, the implementation confirms the efficiency of integrating Vedic mathematics with traditional digital design methods to create a compact, energy-efficient, and high-speed arithmetic unit suitable for embedded processors and DSP systems.

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