Implementation of the High Speed PLL

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Abstract**—***the most multipurpose application of the phase locked loops (PLL) is for clock generation and clockrecovery in microprocessor, networking, communication systems, and digital circuit and frequency synthesizers.Phase locked-loops (PLLs) are commonly used to generate well-timed on-chip clocks inhighperformance digital systems. Modern wireless communication systems employ Phase Locked Loop (PLL) mainly for synchronization, clock synthesis, skew and jitter (deviation) reduction. Because of the increase in the speed of the circuit operation, there is a need of a PLL circuit with fasterlocking ability. Many present communication systems operate in the GHz frequency range. Hence there is a necessity of a PLL which must operate in the GHz range with less lock time.PLL is a mixed signal circuit as itsarchitecture involves both digital and analog signalprocessing units. The present work focuses on the redesign of a PLL system using the 90 nm process technology (GPDK090 library) in EDA TANNER Design Environment.Here a current starved ring oscillator has been considered for its superior performance in form ofits low chip area, low power consumption and wide tunable frequency range. Thesimulation results ofPLL are reported in this work. It is found that the designed PLL consumes 11.68mW power froma 1.8V D.C. supply and have a lock time 280.6 ns. As the voltage controlled oscillator (VCO) isthe heart of the PLL, so the optimization of the VCO circuit is also carried out using the optimization technique. The results of the VCO designed are shown.*

Keyword: PLL, VCO, GDPK 900, Charge pump (CP).

I. Introduction

Phase locked loop (PLL) [1] is the heart of the many modern electronic circuit as well ascommunication system. Recently plenty of the researches have conducted on the design of PLL circuit and still research is going on this topic. Most of the researches haveconducted to realize a higher lock range PLL with lesser lock time [2] and have tolerable phasenoise. The most versatile application of the PLL is for clock generation and clock recovery in microprocessor, networking, communication systems, digital system, and frequencysynthesizers. PLLs are commonly used to generate well-timed on-chipclocks in high-performance digital systems. Modern wireless

communication systems employ PLL mainly for synchronization, clock synthesis, skew and jitter reduction [3]. Phase locked loops find wide application in several modern applications mostly in advance communication and instrumentation systems. PLL being a mixed signal circuit involves design challenge at high frequency.There are mainly five blocks in a PLL. These are:i. phase frequency detector (PFD)

ii. Charge pump (CP)

iii. Low pass loop filter (LPF)

iv. Voltage controlled oscillator (VCO)

v. Frequency divider

Presently almost all communication and electronics devices operate at a higher frequency, so for that purpose we need a faster locking PLL.

i. Phase Detector or Phase Frequency Detector

The "Phase frequency Detector" (PFD) is one of the main part in PLL circuits. It compares thephase and frequency difference between the reference clock and the feedback clock.Depending upon the phase and frequency deviation, it generates two output signals "UP" and"DOWN". Figure 1 shows a traditional PFD circuit.

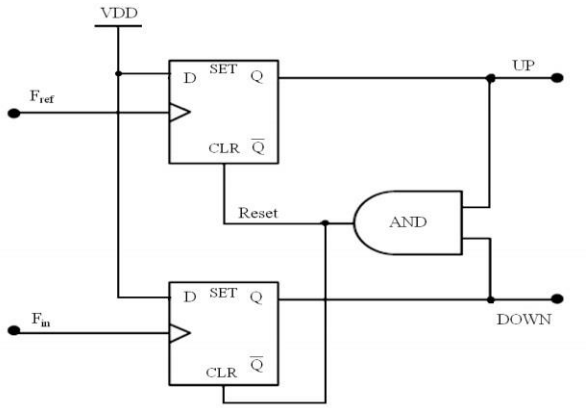

Figure 1 Block diagram of a traditional PFD circuit

If there is a phase difference between the two signals, it will generate "UP" or "DOWN"synchronized signals. When the reference clock rising edge leads the feedback input clockrising edge "UP" signal goes high while keeping "DOWN" signal low. On the other hand if thefeedback input clock rising edge leads the reference clock rising edge "DOWN" signal goes high and "UP" signal goes low. Fast phase and frequency acquisition PFDs [3-5] are generallypreferred over traditional PFD.

ii. Charge Pump and Loop Filter

Charge pump circuit is an importat block of the whole PLL system. It converts the phase orfrequency difference information into a voltage, used to tune the VCO.

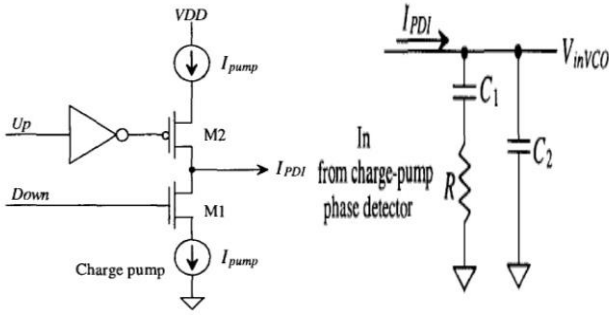

Figure2 Schematic diagram of the charge pump circuit with loop filter

Charge pump circuit is used to combine both the outputs of the PFD and give a single output which is fed to the input of the filter. Charge pump circuit gives a constant current of value IPDI which should be insensitive to the supply voltage variation [3-10]. The amplitude of the current always remains same but the polarity changes which depend on the value of the "UP" and "DOWN" signal. The schematic diagram of the charge pump circuit with loop filter is shown in the Figure 2. When the UP signal goes high M2 transistor turns ON while M1 is OFF and the outputcurrent is IPDI with a positive polarity. When the down signal becomes high M1 transistor turnsON while M2 is OFF and the output current is IPDI with a negative polarity. The charge pumpoutput current [3] is given by

$$I_{PDI} = \frac{I_{PUMP} - (I_{PUMP})}{4\pi} \times \Delta\Phi$$

$$= \frac{2I_{PUMP}}{4\pi} \times \Delta\Phi$$

$$= \frac{I_{PUMP}}{2\pi} \times \Delta\Phi$$

$$= K_{PDI} \times \Delta\Phi \quad (1)$$

Where $K_{PDI} = \frac{I_{PUMP}}{2\pi}$ (amps/radian) (2)

The passive low pass loop filter is used to convert back the charge pump current into thevoltage. The filter should be as compact as possible [2, 3-9].The output voltage of the loop filter controls the oscillation frequency of the VCO. The loop filter voltage will increase if Fref risingedge leads Fin rising edge and will decrease if Fin rising edge leads Fref rising edge. If the PLL isin locked state it maintains a constant value. The VCO input voltage is given by

$$V_{invco} = K_F \times I_{PDI} \quad (3)$$

Where $K_F$is the gain of the loop filter.

iii. Voltage Controlled Oscillator

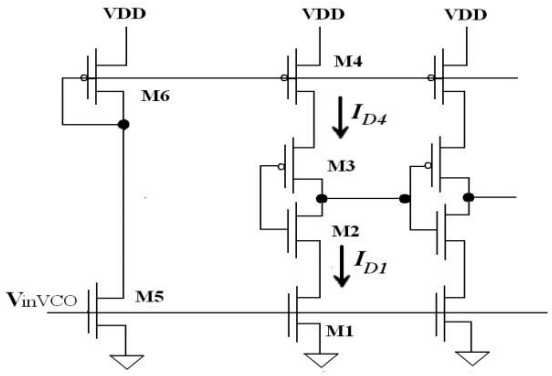

Figure 3 Simplified view of a current starved VCO

An oscillator is an autonomous system which generates a periodic output without any input. The most popular type of the VCO circuit is the current starved voltage controlled oscillator (CSVCO). Here the number of inverter stages is fixed with 5. The simplified view of a singlestage current starved oscillator is shown in the Figure 3.

iv. Frequency Divider

The output of the VCO is fed back to the input of PFD through the frequency divider circuit. Thefrequency divider in the PLL circuit forms a closed loop. It scales down thefrequency of theVCO output signal. A simple D flip flop (DFF) acts as a frequency divider circuit. The schematic of a simple DFF based divide by 2 frequency divider circuit isshown in the Figure 4.

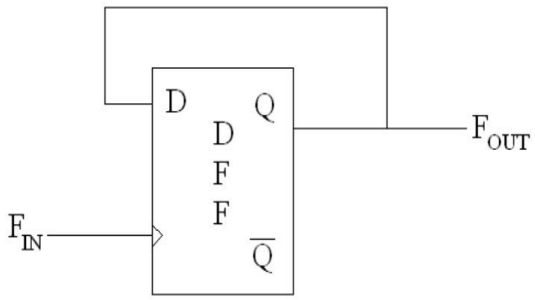

Figure 4 Schematic of a simple DFF based divide by 2 frequency divider circuit

II. Noise and Power Considerations

The primary goal to design a PLL for high-performance digital systems is to generate an output clock with minimum timing uncertainty. The timing uncertainty arises from mismatches in devices and noise sources present in the system. Device mismatches causes a static phase shift (or skew) in the PLL output clock from its desired phase. Skew can be minimized with a careful layout and increasing the device size. Skew is generally less critical than jitter because, due to its static nature, the system can compensate for the static errors. Dynamic noise causes a random phase shift (or jitter) in the PLL output clock. The noise sources in a PLL are device electronic noise such as thermal noise or flicker noise and power-supply or substrate noise.

III. Band Width of PLL

The bandwidth of a PLL is the measure of the PLL's ability to track the input clock and jitter. The closed loop gain 3-dB frequency of the PLL determined the PLL bandwidth. The bandwidth is approximately the unity gain point for PLL open loop response. A high bandwidth PLL provides a fast lock time and tracks jitter on the reference clock source, passing it through to the PLL output. A low bandwidth PLL filters out reference clock jitter, but increase lock time.

IV. Phase Noise and Its Causes

Phase noise is the frequency domain representation of rapid, shot-term random fluctuation in the phase of a wave. The term phase noise is used to describe phase fluctuation due to random frequency fluctuation of a signal. Phase noise can be caused

by a number of conditions, but is mostly affected by an oscillator's frequency stability.

Causes of Phase noise

a. The noise figure of active component such as transistors, integrated circuits, voltage regulator zeners etc.

b. Thermal noise in passive component such as resistors.

c. Flicker noise in active components.

d. Noise process in the oscillator

e. Higher Q crystal will improve lower offset frequencies of phase noise generally less than 100 Hz offset. As the crystal frequency increases the 'Q' of the crystal decreases and the phase noise at lower frequency offset will increases.

f. The crystal has a g-sensitivity that will degrade the phase noise under dynamic vibration conditions.

g. Long-term frequency stability can be affected by a long term drift caused by the crystal and component aging assuming temperature remains same.

h. Frequency Change due to temperature changes can also affect system stability.

V. Limited Range Problem Of conventional VCO

The most common used architecture for VCO in CMOS technology is voltage controlled ring type oscillator. It consists of several delay cells forming a closed loop as shown in figure. The output clock frequency is determined by the delay of each delay cell which in turn is controlled by control voltage. A wide frequency range of oscillator means a wide tuning range of each delay cell. The delay cell is usually a differential pair with a tail current and some active loading. The delay of each cell is controlled by the tail current. There are some difficulties associated with this architecture to achieve the wide tuning range. By using a single tail current, the tuning range is limited by the control voltage range. The control voltage is usually constraint by the power supply voltage, i.e. $0 \leq$ Vcontrol $\leq$ Vdd .If we choose the small tail current, the tail current is still not large enough even that the control voltage reach the up limit so that the high end frequency range of VCO is small. On the other hand, if we choose the large tail current, the tail current is still large even that the control voltage reached the lower limit so that the lower end frequency range of VCO is large.

VI. Result and Conclusion

Result: In case of analog circuit CAD, classical optimization methods [1-4, 5-7], such as steepest descent,sequential quadraticprogramming, and Lagrange multiplier methods are mainly used. These methods are used with more complicated circuit models, including even full SPICE simulationsin each iteration. This method can handle a wide variety of problem. For this there is a need of aset of performance measures and computation of one or more derivatives. The main is advantage of the classical optimization methods

is that the global optimal solution is not possible. This method fails to find a feasible design even one exist. This method gives only the local minimainstead of global solution. Since many different initial designs are considered to get the global

optimization, the method becomes slower. Because of the human intervention (to give "good" initial designs), the method becomes less automated. The classical methods become slow ifcomplex models are used.

Conclusion and Future scope of work:

1. In this work a PLL with a better lock time is presented. The lock time of the PLL is foundto be 280.6 ns.
2. The PLL circuit consumes a power of 11.9 mW from a 1.8 V D.C. supply.
3. The lock time of the PLL mainly depends upon the type of PFD architecture used and theparameters of the charge pump and loop filter. So by properly choosing the PFD architecture and adjusting the charge pump current and the loop filter component values abetter lock time can be achieved.
4. The center frequency of oscillation of the VCO depends upon the sizing of the transistors.The frequency deviation from the desired value can be reduced by properly choosing thetransistor sizes.
5. By applying the convex optimization technique with frequency of oscillation as the main objective function, the deviation of oscillation frequency is minimized to 0.00457% from1.2%.
6. Here the convex technique is used to find out the transistor sizing to meet only the desired frequency specification. The other constraints like area, power and phase noise can also be applied.

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