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IMPLEMENTATION OF UART WITH STATUS REGISTER USING VHDL

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ABSTRACT: Today in real world the actual applications, usually needed only a few key features of UART. Specific interface chip will cause waste of resources and increased cost. Particularly in the field of electronic design, SOC technology is recently becoming increasingly mature. This situation results in the requirement of realizing the whole system function in a single or a very few chips. Universal Asynchronous Receiver Transmitter (UART) is a kind of serial communication protocol. In parallel communication the cost as well as complexity of the system increases due to simultaneous transmission of data bits on multiple wires. Serial communication alleviates this drawback of parallel communication and emerges effectively in many applications for long distance communication as it reduces the signal distortion because of its simple structure. The UART implemented with VHDL language can be integrated into the FPGA to achieve compact, stable and reliable data transmission. Advanced Peripheral Bus (APB) is used for solved interfacing problem. With APB other devices are easy to connect with UART. The proposed design of UART satisfies the system requirements of high integration, stabilization, low bit error rate, and low cost. It also supports configurable baud rate generator and variable data length from 5-8 bits per frame. This project focuses on the VHDL implementation of UART with status register which supports asynchronous serial communication. The project presents the architecture of UART which indicates, during reception of data, parity error, framing error, overrun error and break error using status register. For solving interfacing complexity used an APB.

Keywords: UART, FPGA, VHDL, UVM, PSW

I. INTRODUCTION

A UART is usually an individual (or part of an) integrated circuit used for serial communications over a computer or peripheral device serial port. UARTs are now commonly included in microcontrollers. A dual UART or DUART

combines two UARTs into a single chip. Many modern ICs now come with a UART that can also communicate synchronously; these devices are called USARTs (universal synchronous/ asynchronous receiver/transmitter).

Some early telegraph schemes used variable-length pulses (as in Morse code) and rotating clockwork mechanisms to transmit alphabetic characters. The first UART-like devices (with fixed-length pulses) were rotating mechanical switches (commentators). Various character codes using 5, 6, 7, or 8 data bits became common in teleprinters and later as computer peripherals. Gordon Bell designed the UART for the PDP series of computers. The teletypewriter made an excellent general-purpose I/O device for a small computer. To reduce costs, including wiring and back-plane costs, these computers also pioneered flow control using XON and XOFF characters rather than hardware wires.

II. OBJECTIVE

a) VHDL implementation of UART which has a Status Register that can indicate the Parity error, Frame error, Overrun error and Break error during the reception of data.

The proposed project describes the Universal asynchronous receiver/transmitter i.e. UART which is the kind of serial communication protocol which allows the full duplex communication in serial link. This paper present the hardware implementation of a high namely transmitter speed and efficient UART using FPGA. The UART consists of three main components, receiver and baud rate generator which is nothing but the frequency divider. In telecommunications and computer science, serial communication is the process of sending data one bit at one time, sequentially, over a communications channel or computer bus. This is in contrast to parallel communications, where all the bits of each symbol are sent together.

Serial communication is used for all long-haul communications and most computer networks, where the cost and synchronization difficulties of cable make parallel communications impractical. Serial computer buses are becoming more common as improved technology enables them to transfer data at higher speeds.

LITERATURE SURVEY

1. **M Srinath & Professor Sujatha Hiremath – "Verification of Universal Asynchronous Receiver and Transmitter (UART) uses System Verilog", in Vol. 11 Issue 07, July-2022 (IJERT) pp 307-309.**

   This paper aims at designing a UART using System verilog and verifying the same using a UVM based test bench. UART is one of the most frequently utilized serial communication protocols without the need for a clock

excitation. The design includes baud rate generator, control, bus interface, interrupt control and the receiver-transmitter FIFO blocks. Parallel data from system bus are serialized and transmitted and the vice versa process is performed at the receiver end. The verification environment is a reusable and flexible one thereby reducing the complexity and time. Constrained randomization is adopted for random stimulus generation and a functional coverage of 100% and approximately 76.4% code coverage was achieved.

2. **Pranay Anand Tiwari & Dr. Rajani Bisht – "Design of Low Power Universal Asynchronous Receiver and Transmitter" in Vol. 11 Issue 09, September 2022 -** Power dissipation is one of the key challenges in Electronic Circuit design and their performance in portable applications. Among high performance and high-density chips for example processors, high power dissipation restricts the amount of on chip transistors and increases the demand of essential heat removal, and that lessen the performance and increases the cost and size of the system. Consequently, analysis, power estimation along with optimization is vital challenges for CMOS Circuit design. Dynamic power dissipation is occurred when there is switching activity at some nodes in a CMOS circuit. Dynamic power dissipation is directly proportional to activity switching rate. In this paper, precise and simple method has been proposed to minimize the dynamic power dissipation in UART.

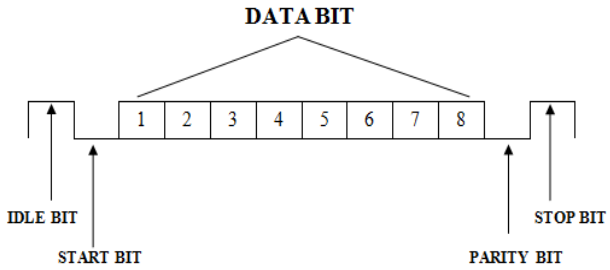


FIGURE: The UART data format

III. STATUS REGISTER

A status register or flag register (also: condition code register, program status word, PSW, etc.) is a collection of flag bits for a processor. An example is the FLAGS register of the x86 architecture.

The status register is a hardware register which contains information about the state of the processor. Individual bits are implicitly or explicitly read and/or written by the machine code instructions executing on the processor. The status register in a traditional processor design includes at least three central flags: Zero, Carry, and Overflow, which are set or cleared automatically as side effects of arithmetic operations. They may then be

tested via conditional branch or jump instructions. A status register may often have other fields as well, such as more specialized flags, interrupt enable bits, and similar types of information. During an interrupt, the status of the thread currently executing can be preserved (and later recalled) by storing the current value of the status register along with the program counter and other active registers into the machine stack or a reserved area of memory.

IV. SYSTEM STUDY AND ANALYSIS

VHDL implementation of UART which has a Status Register that can indicate the Parity error, Frame error, Overflow error and Break error during the reception of data. The proposed project describes the universal asynchronous receiver/transmitter i.e. UART which is the kind of serial communication protocol which allows the full duplex communication in serial link. This paper presents the hardware implementation of a high speed and efficient UART using FPGA. The UART consists of three main components namely transmitter, receiver and baud rate generator which is nothing but the frequency divider.

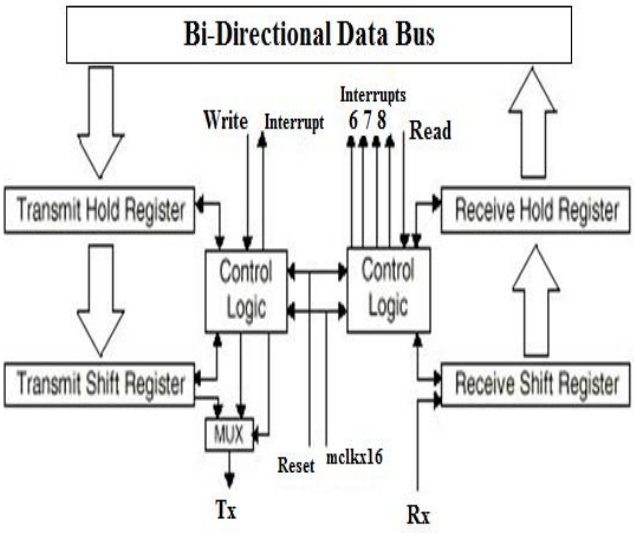


Figure: Block diagram of bi-directional UART

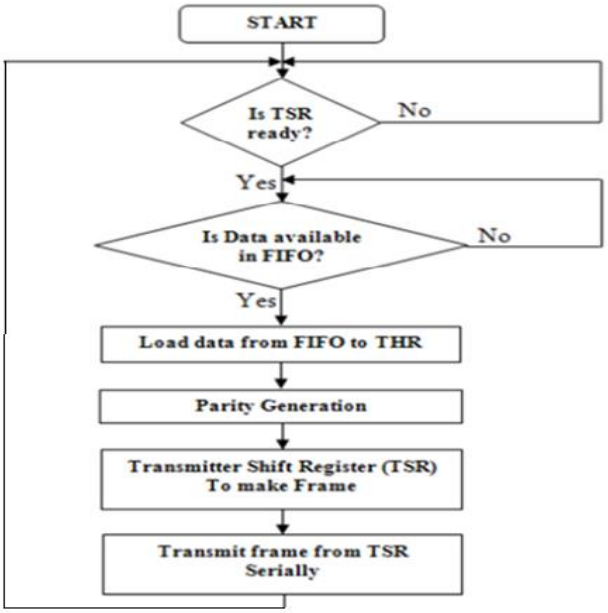
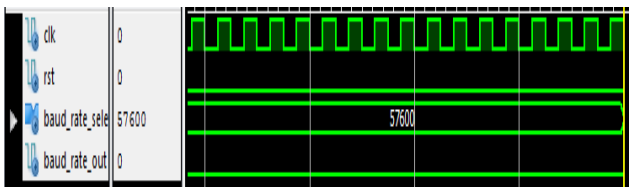
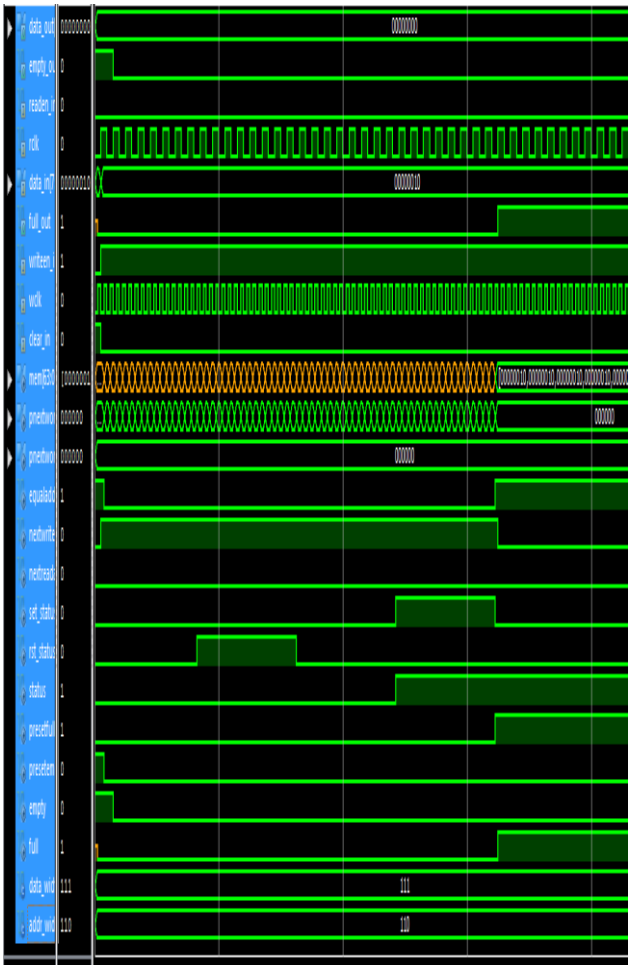


Figure: Receiver flowchart (Input to FIFO)



P.D: Baud rate simulation

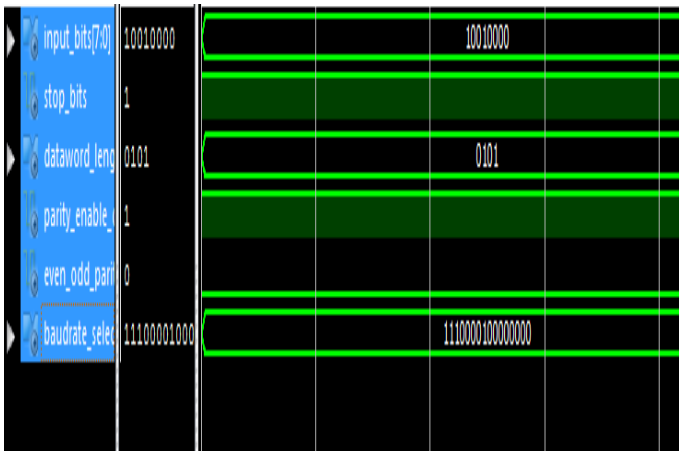
In this simulation is present on 57600 baud rate clock is generate. In normal baud rate is fixed but in this project baud rate is not fixed.



P.D: FIFO SIMULATION

LCR SIMULATION

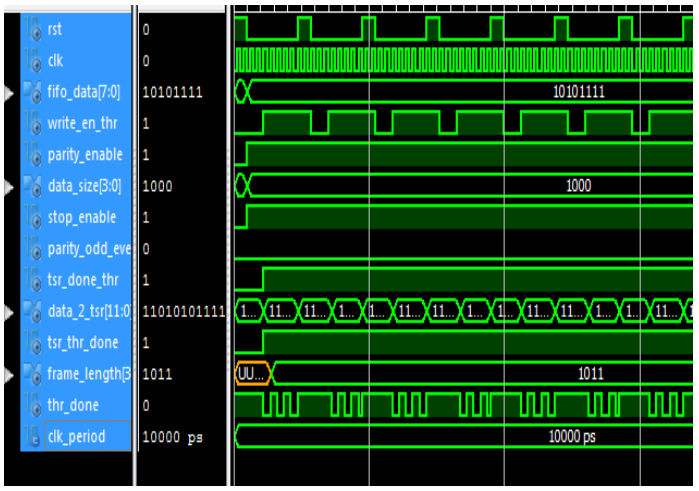
When input bit will be set to logic 1 when RBR data is valid and will be reset to logic 0 when RBR is empty. When line errors (OE/PE/FE/BI) happen, input bit will also be set to logic 1 and data will be updated to reflect the Data bits portion of the frame.



Transmitter Simulation

The simulation shows the transmission of an 8-bit UART frame format with 1 stop bit and without a parity bit. The transmission was set at 115.2kbps using 40MHz clock, which is equal to 25ns (1/40MHz = 25ns) period.

This simulation shows the signal results of the 8-bit data (“00000111B”) transmission via DATA [7:0]. The transmitted UART frame format can be observed at TXD (1 low start bit, 8 data bits (LSB to MSB), and 1 high stop bit).



V. REFERENCES

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