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IMPROVE POWER QUALITY USING CASCADED MULTI-LEVEL INVERTER

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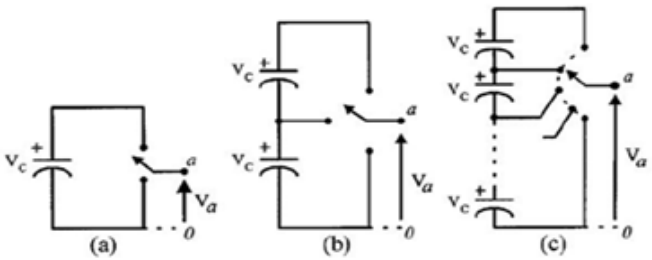
Abstract - The cascaded multilevel inverter (CMLI) has gained much attention in recent years due to its advantages in high voltage and high power with low harmonics applications. A standard cascaded multilevel inverter requires n DC sources for 2n+1 levels at the output, where n is the number of inverter stages. This paper presents a topology to control cascaded multilevel inverter that is implemented with multiple DC sources to get 2n+1 – 1 levels. With using Pulse Width Modulation (PWM) technique, the firing circuit can be implemented which greatly reduces the Total Harmonic Distortion (THD) and switching losses..

1.INTRODUCTION

In this paper, a digital logic control circuit is proposed for a solar-powered CMLI to achieve higher levels with a reduced number of switches without requiring bidirectional switches, filter components, detailed look-up tables, and output transformers. The techniques include "binary", "trinary" and "modified multilevel connections" (MMC) to achieve 15 levels and 27 levels respectively. In some literatures, voltage balancing, ultra-capacitors, PWM switching and transformers are required, which will cause increased cost and manufacturing problems, therefore not desirable for motor drive applications. In MMC, a level of 15 is achieved with the single-stage inverter by adding the input voltages using the built-in controller based on the proposed switching sequence. Comparison of three methods with existing techniques is analyzed and experimentally verifiedPower Multilevel inverter provides a suitable solution for medium and high power systems to synthesize an output voltage which allows a reduction of harmonic content in voltage and current waveforms. Multilevel refers to the multiple connections of individual inverters termed as ‘stages’ to provide the output voltage with required ‘levels’. Increasing the number of levels will result in the reduction of harmonic distortion. The three topologies such as flying capacitor (FC), neutral point clamped (NPC) and cascaded multilevel inverters (CMLIs) are preferred for various applications depending upon its structure and modulation algorithms. Among the three topologies, CMLI is highly preferred for the interconnection of renewable energy systems because of the advantages such as absence of voltage unbalance problem, possible elimination of DC–DC boost converter, adaptive at low switching Frequency and absence of clamping capacitors and diodes.



(a)Two levels, (b) Three levels and (c) N levels

Fig.1 One phase leg of an inverter

2. LITERATURE SURVEY

1. **“A. Rockhill, Graduate Student Member, IEEE, Marco Liserre, Senior Member, IEEE, Remus Teodorescu, Senior Member, IEEE, and Pedro Rodriguez, Member, IEEE** This paper describes the design procedure and performance of an LCL grid filter for a medium-voltage neutralpoint clamped converter to be adopted for a multimegawatt (multi-MW) wind turbine. The unique filter design challenges in this application are driven by a combination of the medium-voltage converter, a limited allowable switching frequency, component physical size and weight concerns, and the stringent limits for allowable injected current harmonics. Traditional design procedures of grid filters for lower power and higher switching frequency converters are not valid for a multi-MW filter connecting a medium-voltage converter switching at low frequency to the electric grid.

- **Jih-Sheng Lai, Senior Member, IEEE, and Fang ZhengPeng, Member, IEEE Multilevel Converters-A New Breed of Power Converters multilevel voltage source converters are emerging as a new breed of power converter options for high-power applications**. The multilevel voltage source converters typically synthesize the staircase voltage wave from several levels of dc capacitor voltages. One of the major limitations of the multilevel converters is the voltage unbalance between different levels. The techniques to balance the voltage between different levels normally involve voltage clamping or capacitor charge control. There are several ways of implementing voltage balance in multilevel converters. Without considering the traditional magnetic coupled converters, this paper presents three recently developed multilevel voltage source converters

- **Rahim, N.A., Selvaraj, J.,2010 „Multistring five-level inverter with novel PWM control scheme for PV application", IEEE Trans. Ind. Electron., , 57, (6), pp. 2111–2123. Multistring Five-Level Inverter With Novel PWM Control Scheme for PV Application** This paper presents a single-phase multistring five-level photovoltaic (PV) inverter topology for grid-connected PV systems with a novel pulse-width-modulated (PWM) control scheme. Three PV strings are cascaded together in parallel configuration and connected to a five-level inverter to produce output voltage in five levels: zero, +1/2V dc, V dc, -1/2V dc, and -V dc. Two reference signals that were identical to each other with an offset that was equivalent to the amplitude of the triangular carrier signal were used to generate PWM signals for the switches. DSP TMS320F2812 is used to implement this PWM switching scheme together with a digital proportional-integral current control algorithm. The inverter offers much less total harmonic distortion and can operate at near-unity power factor. The validity of the proposed inverter is verified through simulation and implemented in a prototype. The experimental results are compared with a conventional single-phase multistring three-level grid-connected PWM inverter.

- **Selvaraj, J., Rahim, N.A. 2009„Multilevel inverter for grid-connected PV system employing digital PI controller", IEEE Trans. Ind. Electron., 56, (1), pp. 149–158 - Multilevel converters offer high power capability, associated with lower output harmonics and lower commutation losses. Their main disadvantage is their complexity, requiring a great number of power devices and passive components, and a rather complex control circuitry.** This paper proposes a single-phase seven- level inverter for grid connected PV systems, with a novel pulse width-modulated (PWM) control scheme. Three reference signals that are identical to each other with an offset that is equivalent to the amplitude of the triangular carrier signal were used to generate the PWM signals. The inverter is capable of producing seven levels of output-voltage levels from the dc supply voltage. This paper proposes a new multilevel inverter topology using an H-bridge output stage with two bidirectional auxiliary switches. The new topology produces a significant reduction in the number of power devices and capacitors required to implement a multilevel output using the Asymmetric Cascade configuration.

3. EXISTING METHODOLOGY

The multiple connections of individual inverters which are called as stages provide the output voltage with required levels. And this multiple connections of individual inverters (in case of CMLI) are termed as "MULTI-LEVEL INVERTER". As the number of increases at o/p it goes more nearer to sinusoidal. Multi-level Inverters are found to be of extreme importance in industrial applications now a days. It has found more applicable in medium and high power applications.MLI fed by solar photovoltaic (PV) cells is dealt in various literatures, but it is applicable for low voltage and low level configurations only. The three techniques such as Flying Capacitor (FC), Cascaded Multilevel Inverters (CMLI) and Neutral-point Clamped (NPC) are preferred for various applications. But again it depends upon its structure and modulation algorithms. C-MLI is highly preferred among the above three techniques for the interconnection in the case of renewable energy systems because of the following advantages,

I]Voltage unbalance problem is eradicated,
II]Use of DC–DC boost converter is eliminated,
III]Again use of clamping capacitors and diodes can be avoided.

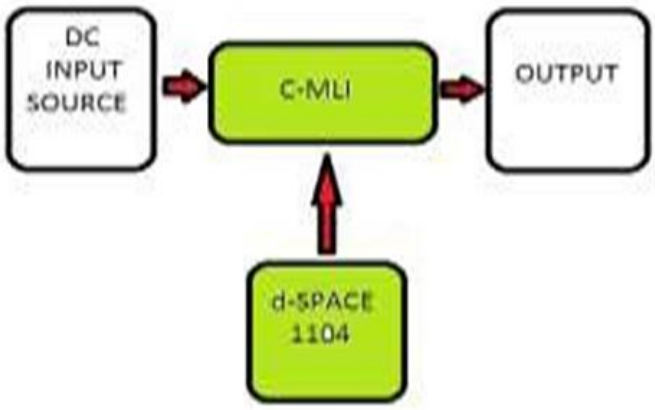


Fig.2 General Block Diagram for Three Modes

4. Switching Strategy

PWM techniques are a conventional approach and in this method reference and carrier signals are compared. And they provide the required gating signals to the inverter switches. The number of output voltage levels obtained from this is method is given by the formula given in equation (1).

M=[2(Ns) +L] 1.

WhereMistheoutputvoltagelevelsandNsistheindividual inverters termed as stages. The number of switches (L) required to obtain M levels at the output is given in the equation (2).

[L=2(M-1)] 2.

So according to above equations to implement 15-level C-MLI using PWM (conventional) technique, the number of switches required is 28 with 7 individual inverters termed as stages. 91 balancing capacitors in case of FC type multilevel inverter along with 14 DC bus capacitors 28 switches, and 182 clamping diodes in case of NPC or diode clamped multilevel inverter are required in addition. Considering above dis-advantages, in this paper a topology is proposed which includes 3 modes namely Binary, Trinary and MMC modes. They have the advantage of reduction of switches. Again the number of levels is also increased which reduces the

Total harmonic distortion (THD). And this leads to improvement of the power quality.

5. MMC MODE

The power circuit in Binary ‟and Trinary ‟mode is same. In above both modes we get 15 and 27 levels using 12 switches and 3 inverter stages. There is change made in power circuit diagram to achieve 15 levels using only 10 switches. Fig shows the power circuit diagram of MMC mode. In this mode input scalling are not compulsory. The input voltages kept here are 48 V, 96 V and 192 Volts.

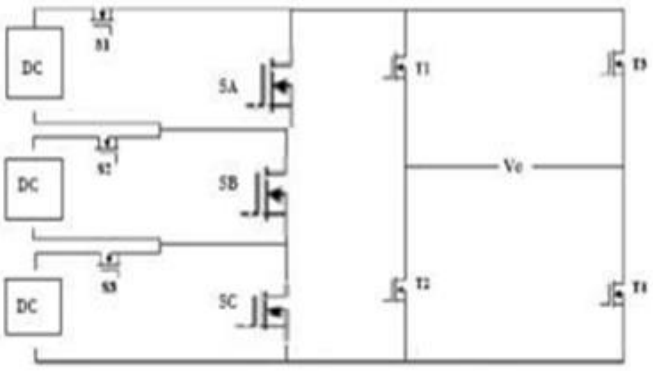


Fig.3 MMC MODE

6. PROPOSED SYSTEM

The Proposed System investigates improvement of power quality for Cascaded MLI with reduced number of semiconductor switches. Binary mode uses only 12 switches to obtain the required 15-level output while that MMC mode uses only 10 switches to obtain same output as that in binary mode that is 15 level output. 27-level output is obtained with 12 switches in trinary mode in addition, power circuit being the same as that of the binary mode. Comparison has been made among the 3 modes by carrying a detailed simulation study in MATLAB for various levels. The method proposed provides with the multiple advantages such as less cost (in case of hardware), reduced THD, minimum computational complexity, simple design and absence of transformers, filter circuit, detailed look-up table and boost converters.

CONCLUSION:

With Improving the power quality of the solar-fed CMLI while reducing the number of semiconductor switchgear was investigated in this project. The required 15-level output is achieved using only 12 keys in binary mode and 7 keys in MMC mode. In addition, 27-level output with 12 keys is obtained through the triple mode. A mathematical model of solar PV is implemented which serves as the input to the phases of the inverter. A detailed simulation study was conducted for different levels and a comparison was made. A CMLI of 3 kWps was implemented for all forms of harmonics and harmonics.

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