

# IMPROVEMENT OF POWER QUALITY USING FUZZY BASED UNIFIED POWER FLOW CONTROLLER

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**Abstract**— The Electricity is contemplated as the back bone for the industrial revolution and in order to conclave the meeting of both industrial and household needs electricity needs to be at a larger transmission. For this paving of the electricity and also regulating the issues which are cascading on the power system something Flexible need to be adapted. Flexible Alternating Current Transmission Systems (FACTS) has been a promising aspect in terms of the power system performance analysis. In this paper a comprehensive analysis on the Unified Power Flow Controller (UPFC) which being one of the FACTS device is presented. Accordingly the UPFC for different cases is perceived using a Proportional Integral (PI) controller and a Fuzzy logic controller (FLC). The Fuzzy logic controller is introduced, developed by the MAMDANI method replacing PI controller on a transmission line under different power system operating conditions. MATLAB/SIMULINK was used in order to delineate the controller network. It was observed that the UPFC with the Fuzzy logic based control technique in lines of alleviating the power quality issues an superior performance than that of UPFC with the PI controller. It could be concluded that the Fuzzy logic controller (FLC) for mitigating the issues of power quality.

**Keywords**— Flexible Alternating current transmission systems (FACTS), Unified Power Flow Controller (UPFC), Proportional integral, fuzzy logic, MATLAB/SIMULINK, Power system, Power Quality.

## I. INTRODUCTION

Initially, the converter branches are characterized by continuous current flow, contrary to the chopped currents of traditional topologies. In addition, a central DC-link capacitor does not exist, since the required storage elements are distributed within the converter branches. This capacitive nature of the phase legs, however, poses challenges in the converter design and operation, especially when the converter faces unbalanced grid conditions. Moreover and unless the sub module capacitance and branch inductance are unrealistically high, so-called circulating currents are expected to flow within the parallel-connected phase legs if the capacitor voltage ripples are not compensated for on a control or hardware level.

Finally, the inversely proportional relation between the line current frequency and the sub module capacitor voltage ripples implies an impediment in the case of an MMC low output frequency operation, such as during motor drive startup or low-speed operation. The aforementioned specificities require special attention for the comprehension of such a system's physical behavior and the development of converter control systems.

The commencement of the FACTS emerge as an riveting approach to help in alleviating several power system difficulties such as the inter area oscillations and controlling all the damping and critical bus voltages on a transmission line. The Flexible AC is corresponding to HVDC and THYRISTORS development designed by using reliable and high speed power electronic controllers leading to a greater transfer of power between controlled areas and damping of the power system oscillations. Among all these devices UPFC is one such Facts device which is versatile. This UPFC is a solid state controller based on the high power electronic used to control individually or sequentially the line parameters voltage frequency line impedance, amplitude and phase angle. However, in order to circumvent the failure of any device the controller present in the device and its design plays a major role. Moreover, the inability to provide effectual power flow control and ignoring dynamic performance of this capacitor dc link were of mere limitations.

The PI controller which was applied the FACTS device was inadequate in terms of providing the transient stability and the robust performance. This draw back was observed due to the hitching of these controlling parameters under different operating conditions To overcome these limitations of this the Fuzzy logic controller based UPFC is introduced in this paper in order to advance the network of power quality of which the PI controller was lagging off. Fuzzy logic controller not only provided the robust performance but also the effective dynamic power flow control. To carry out the simulation MATLAB/SIMULINK is used for the capability of executing faster and better reliable performance.

## II. PROPOSED SYSTEM

The below figure 1 Shows the basic structure of PI based UPFC. This controller block compares the transmission line parameters which are imminent from the Measurement block with the nominal rated values. If the difference zeros in these

values then the setting block will not generate any pulse signal and no signal is designated to the Converter section. In this process if there is a contrast in the values sent by the measurement block and the nominal rated values present the PI Controller will an error is generate which indicates the fault condition. Under this fault condition the setting block generates signal continuously to the PI Controller block. This is given to the two converters with one being Converter 1 which performs shunt compensation and other Converter 2 performs series compensation respectively. These two are connected by a common capacitor DC link. Until and unless the Measurement block parameters and the predefined nominal rated values in the control block are concurred the PI controller permits the pulses from the settings block. Once these values are matched the PI controller stops the pulse from the settings block to the respective converters for the turning off both Series and Shunt compensation.

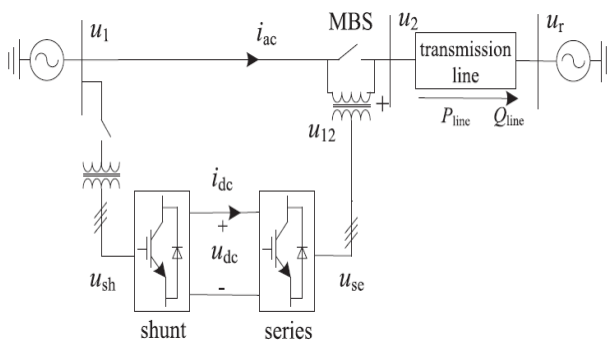


Fig1: Main circuit configuration of the Unified Power Flow Controller (UPFC)

### Equivalent circuit of UPFC

The shunt and series branch between the two buses of voltage source converter is modeled as ideal ac voltage source as shown in figure2.  $I_{sh}$  current inject at shunt branch of UPFC.  $P_{sh}$  and  $Q_{sh}$  are active and reactive power of shunt branch, the direction of these leaving bus  $i$ . The current via UPFC series is  $I_{ij}$  and  $I_{ji}$ ,  $I_{ij} = -I_{ji}$ . The active and reactive power flow of series branch is  $P_{ji}$ ,  $Q_{ji}$  and direction of flow leaving bus  $j$ .

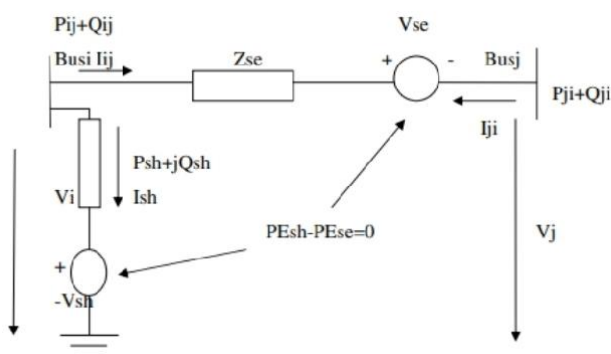


Fig2: Equivalent circuit of UPFC

In the figure equivalent circuit of UPFC is shown. The shunt and series of UPFC power flow constraints are given below,

Where

$$g_{sh}+jb_{sh}=1/Z_{sh}: g_{ij}+jb_{ij}=1/Z_{se};$$

$$\Theta_{ij} = \Theta_i - \Theta_j; \Theta_{ji} = \Theta_i - \Theta_j$$

For shunt branch power flow constraint

$$P_{sh} = V_i \sqrt{2} g_{sh} - V_i \dot{V}_{sh} (g_{sh} \cos(\theta_i - \theta_{sh}) + b_{sh} \sin(\theta_i - \theta_{sh})) \dots\dots\dots 4.1$$

$$Q_{sh} = V_i^2 b_{sh} - V_i V_{sh} (g_{sh} \sin(\theta_i - \theta_{sh}) - b_{sh} \cos(\theta_i - \theta_{sh})) \quad 4.2$$

$$P_{ij} = V_i^2 g_{ij} - V_i V_j (g_{ij} \cos \theta_{ij} + b_{ij} \sin \theta_{ij}) - V_i V_s (g_{ij} \cos(\theta_i - \theta_s) + b_{ij} \sin(\theta_i - \theta_s)) \dots\dots\dots 4.3$$

$$Q_{ij} = -V_i^2 b_{ij} - V_i V_j (g_{ij} \sin \theta_{ij} - b_{ij} \cos \theta_{ij}) - V_i V_s (g_{ij} \sin(\theta_i - \theta_s) - b_{ij} \cos(\theta_i - \theta_s)) \dots\dots\dots 4.4$$

### Series branch power constraints

$$P_{ji} = V_j^2 \left[ \frac{g_{ij}}{V_i V_j} (g_{ij} \cos \theta_{ji} + b_{ij} \sin \theta_{ji}) + V_j V_{se} (g_{ij} \cos (\theta_j - \theta_{se}) + b_{ij} \sin (\theta_j - \theta_{se})) \right] \dots 4.5$$

$$Q_{ji} = -V_j^2 b_{ij} - V_i V_j (g_{ij} \sin \theta_{ji} - b_{ij} \cos \theta_{ji}) + V_j V_{se} (g_{ij} \sin (\theta_j - \theta_{se}) - b_{ij} \cos (\theta_j - \theta_{se})) \dots\dots\dots 4.6$$

### III. CONTROLLERS

### A. Control Strategy for Shunt Converter

The shunt converter which usually performs the shunt compensation has an important function in the operation of UPFC system and it can be termed as a STATCOM is shown in fig3. The STATCOM controller has the AC and DC controller whereas the AC controller controls the reactive power and the DC controller controls the active power. The DC controller generates reference active power reference current  $I_p^*$ . The AC controller generates the reference reactive current  $I_r^*$ . The reference value is compared with the measured value and generate  $E_p$ ,  $E_r$ . In this case  $I_p^*$  will be zero and  $I_r^*$  will be finite. The  $I_p$  and the  $I_q$  are represented as the  $i_d$  and  $i_q$  components respectively generated by parts transformation. One more important aspect of this aspect being the capacitor injecting reactive power. From the  $E_p$  and  $E_r$  values the magnitude and phase angle of compensation reference signals is generated. This below equation is used for the calculation of the Real/Reactive current calculator.

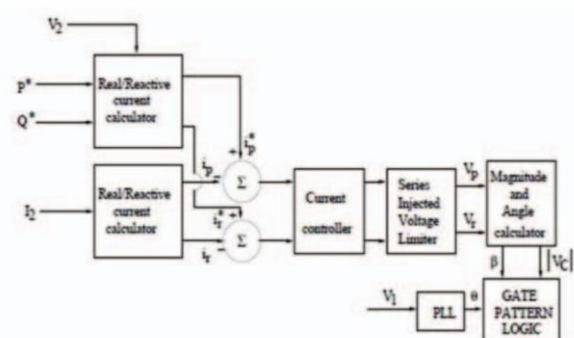


Fig.3: Shunt converter of UPFC

### B. Control Strategy For Series Converter

The series converter accomplishes the main purpose of UPFC as shown in below fig4. The values of both the magnitude and also the phase angle of series- injected voltage is examined by the series converter to pave the desired real and reactive power flow in the transmission line.

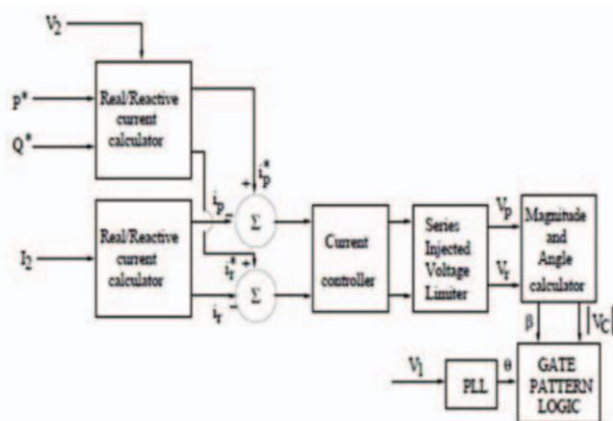


Fig 4 : Series converter of UPFC

The operation is limited as to be same as the shunt converter for the relaxation being that  $Q^*$  is taken as zero value and in the place of  $E$  as both are in series.

### C. PI Controller

It is well known the integral part of the PID controller produces a signal that is proportional to the time integral of the input of the controller. Figure shows the block diagram of a feedback control system that as a plant with transfer function  $G_p(s)$  and a controller with proportional-integral (PI) components.

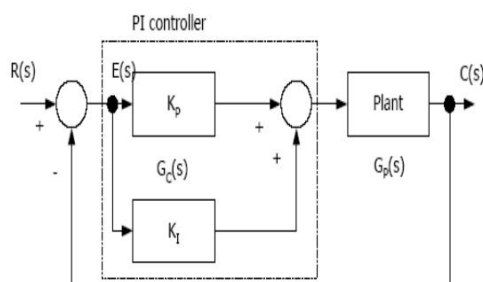


Fig : Basic structure of PI controller

A P.I Controller is a feedback control loop that calculates an error signal by taking the difference between the output of a system, which in this case is the power being drawn from the battery, and the set point.

It is important to point out that due to the complexity of the electronic components within the circuit path (i.e. ESC, power limiter, and motor) I was not able to accurately create model

(transfer function) for the system. Having a transfer function would have allowed me to simulate the system in a software package such as MATLAB/Simulink and assist me in finding the right proportional and integral constant parameters for the controller. Unfortunately, due to the lack of a model, the parameters were obtained via a trial-and-error format.

#### D. FUZZY Controller

The below figure escalates the basic functioning model of the Fuzzy logic controller for any device to be applied in. This fuzzy logic controller mainly consists of 1.Fuzzifier 2. Rule base 3. Control block 4. DEFUZZIFIER. The detailed analysis description about the fuzzy is also described

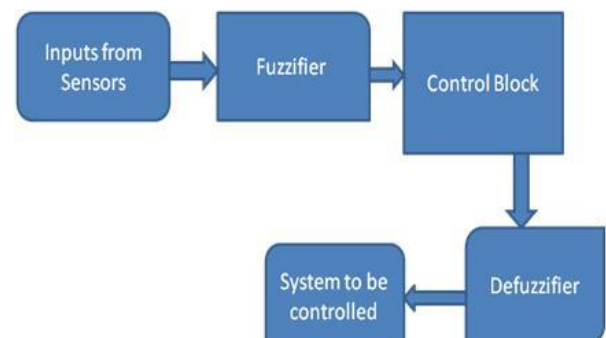


Fig. : Simplified model of FUZZY logic controller

A).FUZZIFIER: FUZZIFICATION is the process of decomposing a system input and/or output into one or more fuzzy sets and the block which performs this is a FUZZIFIER. The process of FUZZIFICATION permits the system inputs and outputs to be defined in linguistic terms to allow rules to be applied in a simple manner to express a complex system.

B) **CONTROL BLOCK:** The error and change in the error are described as linguistic variables such as Negative Big (NB), Negative medium (NM), negative small (NS), Zero (EZ), positive small (PS), positive medium (PM) and Positive big(PB). The input values of the fuzzy controller. The relationship between the input and the output values can be achieved easily by using MAMDHANI method.

E/CE	NB	NM	NS	EZ	PS	PM	PB
PB	Z	PS	PM	PB	PB	PB	PB
PM	NS	Z	PS	PM	PB	PB	PB
PS	NM	NS	Z	PS	PM	PB	PB
EZ	NB	NM	NS	Z	PS	PM	PB
NS	NB	NB	NM	NS	Z	PS	PM
NM	NB	NB	NB	NM	NS	Z	PS
NB	NB	NB	NB	NB	NM	NS	Z

Table. Fuzzy rule base

C). **DEFUZZIFIER**: In many systems whose output is fuzzy, is easier to take a crisp output represented as an single scalar quantity. This, conversion of the fuzzy set to single crisp value is called **DEFUZZIFICATION**.

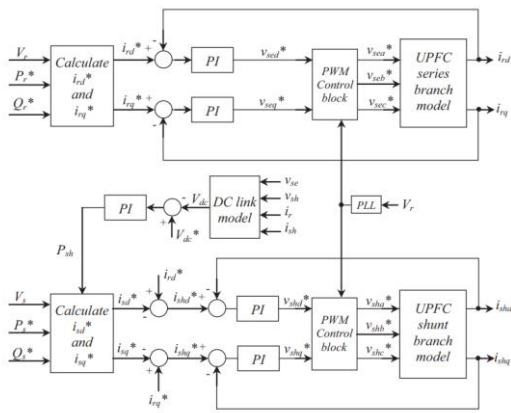
## VI. CONTROLLER DESIGN

The currents through the series branch of the circuit can be expressed by the following differential equations for 3 phases of the system.

$$\begin{cases} L \frac{di_{sa}}{dt} = -r i_{sa} + v_{sa} - v_{sea} - v_{ra} \\ L \frac{di_{sb}}{dt} = -r i_{sb} + v_{sb} - v_{seb} - v_{rb} \\ L \frac{di_{sc}}{dt} = -r i_{sc} + v_{sc} - v_{sec} - v_{rc} \end{cases} \quad (1)$$

The differential equations for the shunt branch currents are obtained as follows

$$\begin{cases} L_{sh} \frac{di_{sha}}{dt} = -r_{sh} i_{sha} + v_{sha} - v_{sea} - v_{ra} \\ L_{sh} \frac{di_{shb}}{dt} = -r_{sh} i_{shb} + v_{shb} - v_{seb} - v_{rb} \\ L_{sh} \frac{di_{shc}}{dt} = -r_{sh} i_{shc} + v_{shc} - v_{sec} - v_{rc} \end{cases} \quad (2)$$



The 3-phase system differential equations can be transformed into a "d, q" reference frame using Park's transformation, as follows

$$\frac{d}{dt} \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} = \begin{bmatrix} -\frac{r}{L} & \omega \\ -\omega & -\frac{r}{L} \end{bmatrix} \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} + \frac{1}{L} \begin{bmatrix} v_{sd} - v_{sed} - v_{rd} \\ v_{sq} - v_{seq} - v_{rq} \end{bmatrix} \quad (3)$$

$$\frac{d}{dt} \begin{bmatrix} i_{sha} \\ i_{shq} \end{bmatrix} = \begin{bmatrix} -\frac{r_{sh}}{L_{sh}} & -\omega \\ -\omega & -\frac{r_{sh}}{L_{sh}} \end{bmatrix} \begin{bmatrix} i_{sha} \\ i_{shq} \end{bmatrix} + \frac{1}{L_{sh}} \begin{bmatrix} v_{sha} - v_{sea} - v_{ra} \\ v_{shq} - v_{seb} - v_{rb} \end{bmatrix} \quad (4)$$

The relations between the different currents can be expressed as follows

$$i_{rd} = i_{sd} + i_{sha} \quad (5)$$

$$i_{rq} = i_{sq} + i_{shq} \quad (6)$$

By writing the power balance, the following dynamic equation is obtained

$$\frac{dV_C}{dt} = \frac{3}{2C V_C} (v_{sed} i_{rd} + v_{seq} i_{rq} - v_{shd} i_{sha} - v_{shq} i_{shq}) \quad (7)$$

The active and reactive powers of the source are as follows.

$$P_s = \frac{3}{2} (v_{sd} i_{sq} + v_{sq} i_{sd}) \quad (8)$$

$$Q_s = \frac{3}{2} (v_{sq} i_{sd} - v_{sd} i_{sq}) \quad (9)$$

The active and reactive powers of the receiver are as follows.

$$P_r = \frac{3}{2} (v_{rd} i_{rq} + v_{rq} i_{rd}) \quad (10)$$

$$Q_r = \frac{3}{2} (v_{rq} i_{rd} - v_{rd} i_{rq}) \quad (11)$$

## V. TEST SYSTEM MODELS AND RESULTS

### Parameters:

#### BUS DATA:

BUS B1,B2,B3 : Base Power = 100e6

Base Voltage = 500e3

TRANSMISSION LINE DATA : length is 75 km

Resistance = 0.01273Ω/km

Inductance = 0.9337mH/km

Capacitance = 12.74nF/km

3phase load : Vrms = 220e3, Frequency = 50Hz, P = 300e6

3phase to phase source : Vrms = 220e3, angle = 9.2degree,

Base voltage = 500e3

3phase series RL : R= 220e3, I=220e3

Breaker : 0.4-0.8 sec

### CASE 1: ASYMMETRICAL TRANSMISSION LINE PARAMETERS:

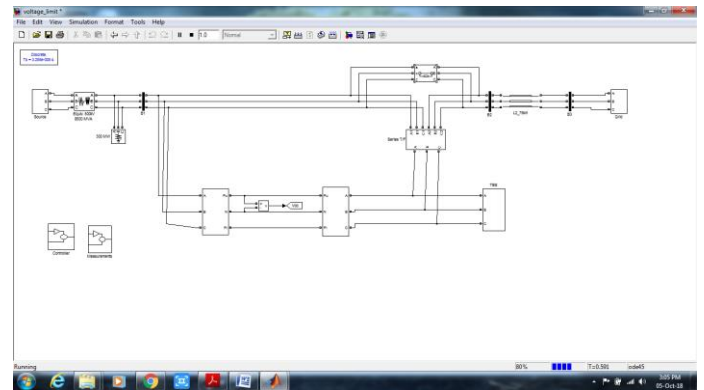


Fig: Simulation diagram for the case of asymmetry of transmission line parameters



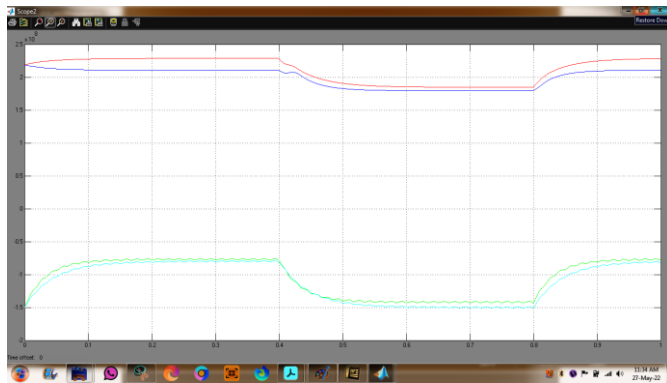


fig: (a) active and reactive power

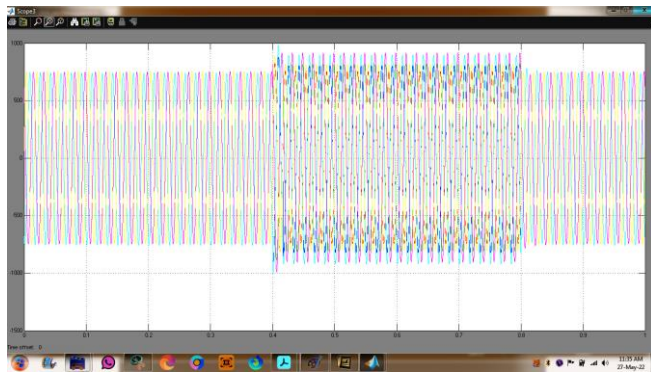


fig: (b) ac currents of transmission line.

In this section, the asymmetry of transmission lines is modeled by the parallel layout of the underground cables. The depth and spacing of the cables is 1 m and 0.12 m, respectively. Before UPFC starts operation at 0.8 s, the original power flow is (175MW, -125MVar) with visible ripples because of the unbalanced currents, as shown in Fig. (a). After 0.8 s, UPFC starts to regulate the power flow at its reference (215 MW, 0 MVar). Fig. (b) shows the current waveform before and after UPFC is activated. With the proposed control, UPFC reduces the unbalance factor of currents from about 15% before 0.8 s to 0.22% after 0.8 s.

#### CASE 2: LOAD IMBALANCE:

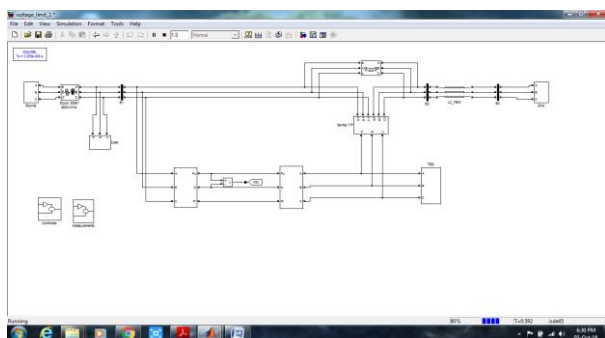
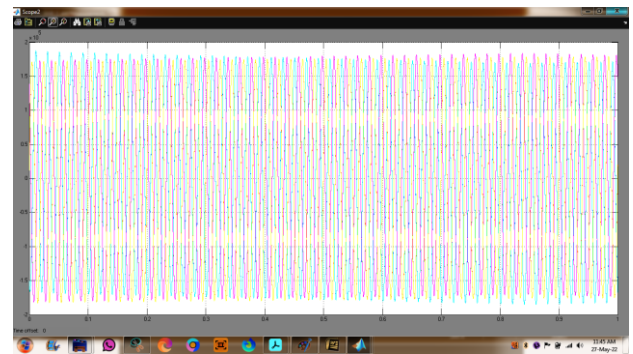
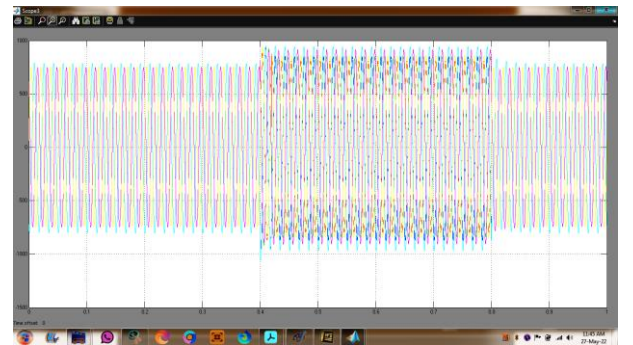


Fig: Simulation diagram for the case of load imbalance



(a) voltage at receiving end



(b) ac currents of transmission line

The load imbalance is modeled by the imbalance of load impedance  $Z_L$ . Meanwhile, the cables are laid in triangle to assure of the balance of transmission impedance  $Z_{line}$ . Fig. illustrates the waveforms of currents and voltages at the receiving end. Due to load imbalance, the unbalance factor of voltages at the receiving end reaches 2.8%, which causes the unbalance factor of currents up to 73.1% without UPFC. After UPFC puts into service at 0.8 s, the unbalance factor of currents reduces to 0.13%.

#### CASE 3: AC FAULT:

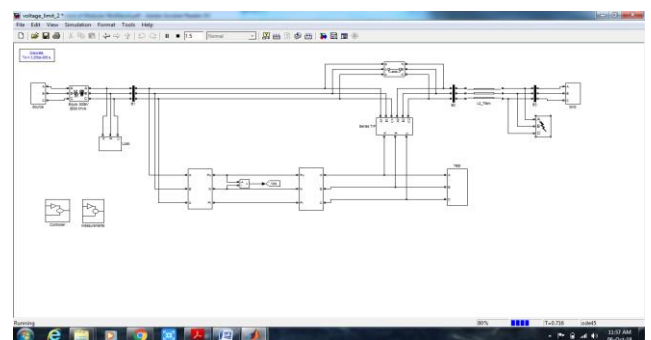
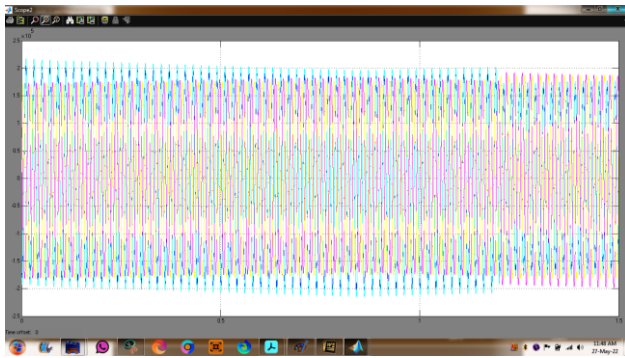
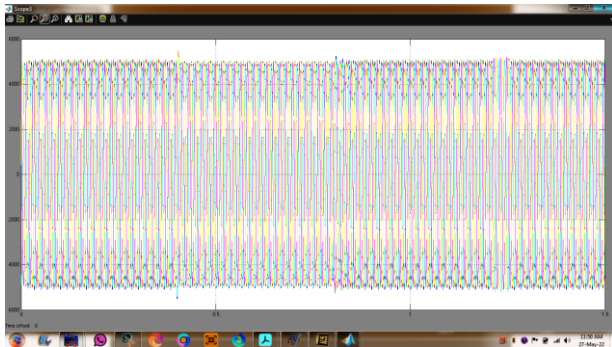


Fig: Simulation diagram for the case of ac fault



(a) voltage at receiving end



(b) ac currents of transmission line

Following the event in case 2, a remote ac fault occurs to the receiving end at 1.2 s. Fig. illustrates the waveforms of currents and voltages at the receiving end. Even though voltages at the receiving end become unbalanced, ac currents get through the fault quickly and still keep balanced with the help of UPFC, as shown in Figure

#### CASE 4: SLIGHT AC FAULT:

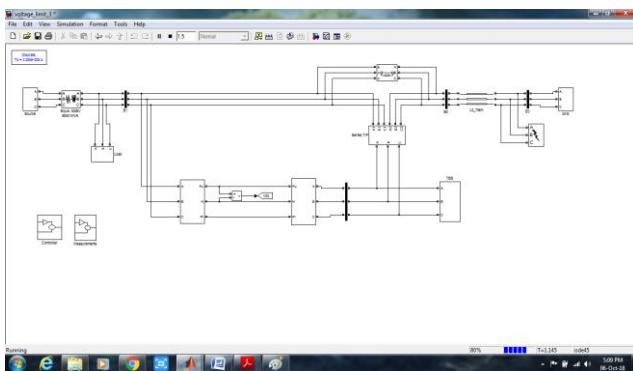
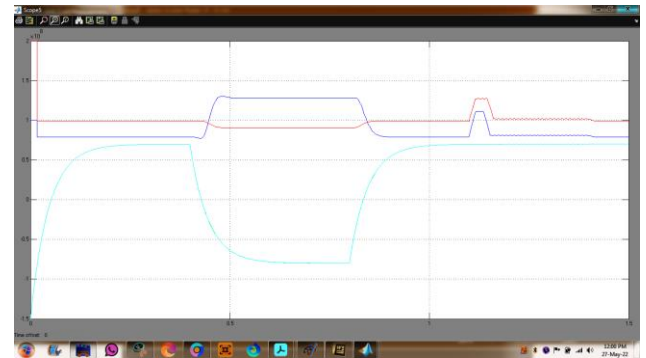
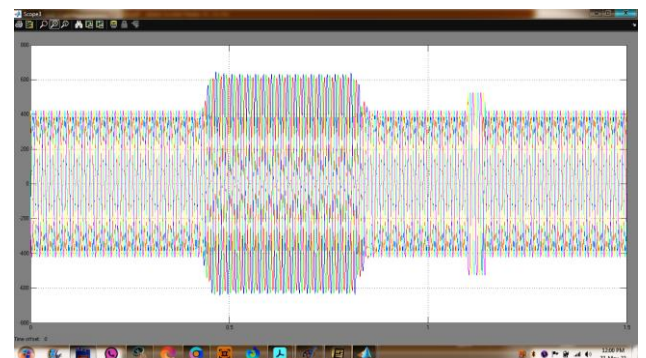


Fig: Simulation diagram for the case of slight ac fault



(a) active and reactive power



(b) ac currents of transmission line

Before UPFC is activated at 0.8 s, the power flow of the transmission line is (185 MW, -128 MVar), as shown in Fig. 8. At 0.8 s, UPFC starts operation with the reference (150 MW, 0 MVar) within the controllable region. An ac faults occurs to the receiving end at 1.1 s and lasts for 0.3 s. The unbalance factor of voltages at the receiving end is 3.4%. In this case, the set power point becomes out of the controllable region corresponding to this unbalanced condition. By the online calculation block, the corresponding original point is obtained as (240MW, -70 MVar).With the proposed voltage limit control, UPFC shifts the power flow from the reference point (150 MW, 0 MVar) to the actual point (168 MW, -14 MVar) on the boundary of  $U_m$ . As shown in Fig, the maximum voltage amplitude among three phases corresponding to (168 MW, -14 MVar) is 10 kV. When the fault is cleared at 1.4 s, UPFC regulates the power to come back to (150 MW, 0 MVar) quickly and steadily.

## VI. CONCLUSION

In this paper the importance of the FACTS device for the reason it is analyzed is observed. The one of the MAJOR FACT device that is the UPFC (Unified Power flow controller) along with the two compensations both series and shunt compensation are examined.. Along with this the performance of the UPFC with PI controller is studied. This Paper introduces a Fuzzy logic controller is proposed with the Unified Power Flow Controller and the performance is analyzed. This is done using a MATLAB/SIMULINK. Moreover this output is compared with the PI Controller based UPFC and the compensating values are extracted. From this

observation could be made that the introduced Fuzzy Logic Controller based UPFC has a better compensating values with in comparison to the PI controller based UPFC. Thus this could be concluded that the Fuzzy logic controller is an ideal controller for mitigating the issues of Power Quality.

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