International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 03 Issue: 11 | Nov -2019 ISSN: 2590-1892

Latest Trending Multilevel Inverter Designing and Analysis in Simulation for Grid Power System

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Traditional inverters have been for the most part recognized for high-control high-voltage applications. Their display is uncommonly superior to that of standard two-level inverters in light of diminished consonant contorting, lower electromagnetic impedance, and higher dc interface voltages. Regardless, it has a couple of damages, for instance, extended number of portions, complex PWM procedure for balance control methodology, and voltage-altering issue. In this exposition, another topology with a pivoting voltage section is proposed to improve the amazed display by compensating the preventions referenced. This topology requires fewer portions stood out from existing inverters (particularly in increasingly critical levels) and requires less flag and entryway drives. Thusly, the general cost and unconventionality are immensely diminished particularly for better return voltage levels. Finally, a model of the seven-level proposed topology is built and attempted to show the display of the inverter by test results. The sun arranged based lift converter facilitated stunned inverter presented. It uses different changes to make stunned yield wandered waveform. The purpose of the work to make 9 level wave structure using sun fueled and help converter. The standard inverter has various sources and has 16 switches are required and besides continuously number of voltage sources required. The proposed inverter required single daylight based board and reduced number of switches and fused lift converter which increase the information voltage of the inverter. The proposed inverter duplicated and differentiated and R load using MATLAB and model probably affirmed. The proposed inverter can be used in n number of sun situated applications.

Keywords: Multilevel inverter, power electronics, SPWM, topology, switches etc.

1.1 New Multilevel Topology

In traditional multilevel inverters, the power semiconductor switches are consolidated to deliver a high- frequency waveform in positive and negative polarities. Notwithstanding, there is no compelling reason to use every one of the switches for creating bipolar levels. This thought has been incorporated by the new topology. This topology is a crossover staggered topology which isolates the yield voltage into two sections. One section is named level generation part and is liable for level producing in positive extremity. This part requires high- frequency changes to produce the necessary levels. The switches in this part ought to have high-exchanging frequency ability.

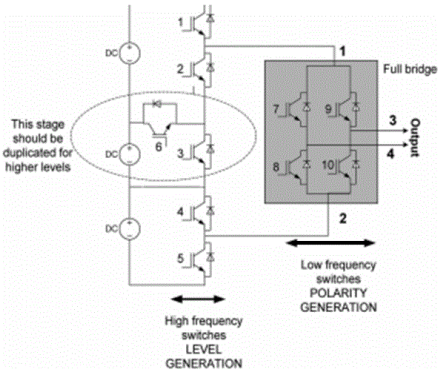

Fig 1.1 Level Generations

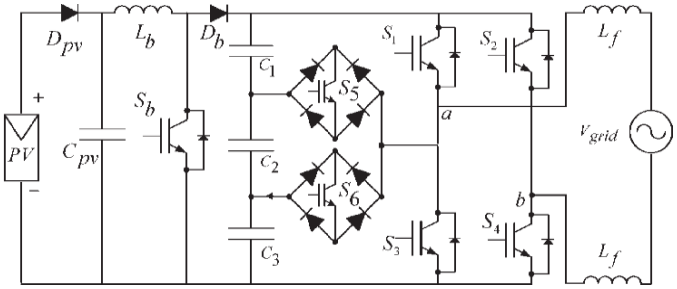

Fig 1.2 Single-Phase Seven-Level Grid-Connected Inverter grid connected system

The other part is called polarity generation part and is answerable for creating the extremity of the yield voltage, which is the low- frequency part working at line frequency. The topology consolidates the two sections (high frequency and low frequency) to produce the multilevel voltage output. So as to produce a total staggered yield, the positive levels are created by the high- frequency part (level age), and afterward, this part is encouraged to a full-connect inverter (extremity age), which will produce the necessary extremity for the yield. This will kill a large number of the semiconductor switches which were responsible to create the output voltage levels in positive and negative polarities.

The RV topology in seven levels is appeared in Fig. 1.1. As can be seen, it requires ten switches and three segregated sources. The vital thought of this topology as a staggered inverter is that the left stage in Fig. 1.1 creates the necessary yield levels (without extremity) and the correct circuit (full-connect converter) chooses about the extremity of the yield voltage. This part, which is named extremity age, moves the necessary yield level to the yield with a similar bearing or inverse course as indicated by the necessary yield extremity. It

inverts the voltage bearing when the voltage extremity requires to be changed for negative extremity. This topology effectively reaches out to higher voltage levels by copying the center stage as appeared in Fig. 1.1. Consequently, this topology is particular and can be effectively expanded to higher voltage levels by including the center stage in Fig. 1.1 It can likewise be applied for three-stage applications with a similar guideline. This topology utilizes separated dc supplies. Along these lines, it doesn't confront voltage-adjusting issues because of fixed dc voltage esteems. In correlation with a course topology, it requires only 33% of secluded power supplies utilized in a course type inverter.

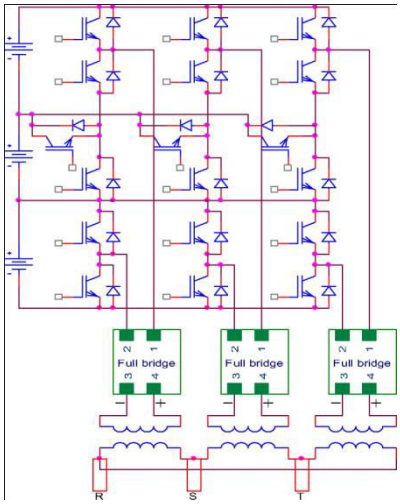

Fig 1.3 RV topology in seven levels

In Fig. 1.3, the total three-stage inverter for seven levels is appeared with a three-stage delta associated system. As indicated by Fig. 1.3, the staggered positive voltage is fed to the full-connect converter to create its extremity. At that point, each full-connect converter will drive the essential of a transformer. The auxiliary of the transformer is delta (Δ) associated and can be associated with a three-stage system. This topology requires less segments in contrast with ordinary inverters. Another favorable position of the topology is that it just requires half of the ordinary transporters for SPWM controller. SPWM for seven-level traditional converters comprises of six bearers, however in this topology, three transporters are adequate.

The explanation is that, as per Fig. 1.1, the multilevel converter works just in positive extremity and doesn't produce negative polarities. Along these lines, it executes the multilevel inverter with a decreased number of carriers, which is an incredible accomplishment for inverter control. It is likewise equivalent to single-bearer.

1.2 Switching Sequences for each level

This topology requires a similar number of input for PWM. Be that as it may, this topology needs one balance signal which is simpler to produce rather than the single-bearer balance technique which needs a few adjustment signals. Another inconvenience of this topology is that all switches ought to be chosen from quick switches, while the proposed topology needn't with quick switches for the extremity generation part. In the accompanying areas, the prevalence of this topology with deference over PWM exchanging and number of segments is talked about.

1.2.1 Switching Sequences

Switching sequences in this converter are simpler than it's another function. As indicated by its intrinsic points of interest, it doesn't have to create negative signal for negative cycle control. In this way, there is no requirement for additional conditions for controlling the negative voltage. Rather, the turning around full-connect converter plays out this undertaking, and the necessary level is delivered by the high-switching frequency part of the inverter. At that point, this level is meant negative or positive as per yield voltage prerequisites.

This topology is redundant and flexible in the switching sequence. Different switching modes in generating the required levels for a seven-level RV inverter are shown in Table I. In Table I, the numbers show the switch according to Fig. 1 which should be turned on to generate the required voltage level. According to the table, there are six possible switching patterns to control the inverter. It shows the great redundancy of the topology. However, as the dc sources are externally adjustable sources (dc power supplies), there is no need for voltage balancing for this work. In order to avoid unwanted voltage levels during switching cycles, the switching modes should be selected so that the switching transitions become minimal during each mode transfer.

This will likewise diminish switching power dissemination. As indicated by the previously mentioned proposals, the groupings of switches (2–3-4), (2-3-5), (2-6-5), and (1, 5) are picked for levels 0 up to 3, separately. These groupings are appeared in Fig. 3. As can be seen from Fig. 3, the yield voltage levels are created in this part by fitting switching groupings. A definitive yield voltage level is the total of voltage sources, which are remembered for the present way that is set apart in strong. So as to conduct seven levels by SPWM, three saw-tooth waveforms for signal and a sinusoidal reference signal for modulator are required as appeared in Fig. 1.3. In this dissertation, PD SPWM is received for its effortlessness. Transporters in this strategy don't have any reoccurrence event, and they have unequivocal counter balanced from one another. They are additionally in stage with one another. The modulator and three transporters for SPWM are appeared in Fig. 1.3.

Pulse Width Modulation Technique

2.1 Introduction

To fulfill partial power requirements, variable resistance devices such as rheostats were used to control the current entering a device (i.e. sewing machines) these devices suffered from major energy losses from heat in the resistor elements. Other device power control devices included voltage stepping autotransformers such as the Autrastat. There was a need for a low cost, efficient, and compact option for providing adjustable power for electronic devices.

2.2 Pulse Width Modulation

Pulse Width Modulation is a technique that conforms a signal width, generally pulses based on modulator signal information. The general purpose of Pulse Width Modulation is to control power delivery, especially to inertial electrical devices. The on-off behavior changes the average power of signal. Output signal alternates between on and off within a specified period.

If signal toggles between on and off quicker than the load, then the load is not affected by the toggling. A secondary use of PWM is to encode information for transmission.

2.2.1 Duty cycle

The Duty Cycle is a measure of the time the modulated signal is in its "high" state.It is generally recorded as the percentage of the signal period where the signal is considered on.

2.2.2 Advantages of Using PWM

Average value proportional to duty cycle, this dependence is often observed to follow a linear trend due to the previous formulaic definition. Low power used in transistors used to switch the signal, and fast switching possible due to MOSFETS and power transistors at speeds in excess of 100 kHzAlleviates the problem of high heat loses through resistive elements at intermediate voltage points.

2.2.3 Disadvantages to Using PWM

Cost of integrated circuit packages for PWM, Complexity of circuitry necessary for implementation, Radio Frequency Interference/Electromagnetic Interference limits the performance of the circuitry. Voltage spikes in the pulse signal to a rapid succession of switches similar to an impulse

2.2.4 General Types of Pulse Width Modulation

There are three commonly used types of PWM defined by which edge of the analog signal is to be modulated

- Lead Edge Modulation
- Trail Edge Modulation
- Pulse Center Two Edge Modulation/Phase Correct PWM

2.2.4.1 Lead Edge Modulation

The lead edge of the trigger signal is fixed to the leading edge of the time spectrum and the trailing edge is modulatedTrigger Signal PWM Signal.

2.3 Methods for Pulse Width Modulation Generation

There are several methods for generating the PWM signal, including the following:

- Analog Generation Methods
- The Intersective Method
- Digital Generation Method
- Delta Modulation
- Delta Sigma Modulation
- Space Vector Modulation
- Application Specific Methods
- Direct Torque Control
- Time Proportioning

2.3.1 Analog Generation Methods: Allows for the analog creation of the PWM signal through simply noting the intersections between a sawtooth or triangular trigger signal and a reference sinusoid.

The length of the pulses is dependent upon the intersection of the reference sinusoid and trigger signal when the sinusoid is greater than the signal, the PWM pulse is switched to the on/high position. When the sinusoid is less than the signal, the PWM pulse is switched to the off/low position

2.3.2 Digital Generation Methods

2.3.2.1 Delta Modulation: By using the reference analog signal only, a set of limits set by a constant offset, and the integrated PWM signal, a switching method is created.

To operate the multilevel inverter, low and high switching frequency modulation techniques have been carried out for the research. Based on the suitability of operation and the output requirements, various modulation techniques like Sinusoidal Pulse Width Modulation (SPWM), Space Vector Pulse Width Modulation (SVPWM), staircase modulation, trapezoidal modulation, harmonic injection modulation, etc, are implemented .Among all these PWM methods, multiple carriers PWM offers several advantages over single carrier PWM. Selection of the number of carrier signals for the operation of the PWM technique is chosen by Multiple carrier modulation techniques are divided into level shifting and phase shifting techniques. Level shifting technique is divided into constant switching frequency multi carrier signal and variable switching frequency multi carrier signal techniques. PD, POD, and APOD are the subdivisions of switching frequency techniques.

In this work, a sinusoidal modulating signal for SPWM with triangular multi carrier signals are used to produce PWM pulses for the operation of switches in 5 switch and 8 switch

module. Level shifting pulse width modulation technique is implemented with constant switching frequency and variable switching frequency with their subdivisions. 'L-1' triangular carrier signals are used with the amplitude of 'Ac' and frequency of 'fc'. A modulating signal of sinusoidal waveform with the amplitude of 'Am' and frequency of 'fm' to generate the pulse for the ON/OFF conditions of the switch is done with the signal comparison of the reference and carrier of PWM method. Based on the amplitude and frequency of the modulating and the carrier signal, modulation index 'Mi' and frequency ratio 'Mf' is estimated.

3.1 logical operations and Several Switching Modes

Binary logic consists of various logical operations which represent a logical meaning for various conditions based on the output of systems. In many computer and processor operations, computational analysis and decision making systems, binary logic operations play the key role for system control. Binary logic mainly depends on two values with different names like 'True and False', 'Yes and No', 'On and Off' etc. In this dissertation , the values with '1' and '0' are preferred for convenience. '1' assigned for 'On' condition of the switch and '0' assigned for 'Off' condition. The combination of binary logic and a proper logical operation called Boolean algebra.

INPUT		OUTPUT					
A	B	OR	AND	NOR	NAND	EXOR	EXNOR
0	0	0	1	1	1	0	1
0	1	1	0	0	1	1	0
1	0	1	0	0	1	1	0
1	1	1	0	0	0	0	1

TABLE 3.1 Truth Table of OR, AND, NOR, NAND, EXOR and EXNOR Logic Gates for Two Inputs

Boolean algebra basically consists of three logical operations, which are called basic logic gates: AND, OR and NOT. Each logical operation produces a binary output based on their operation presented as truth table in Table 1 for two input signals. These logic gates are electronic circuits which operate on two or more input signals and generate desired output based on the logical operation except NOT gate. NOT gates operate with one signal and its truth table is given in Table 2. Input signals may be a communication signal, electrical voltage or current signal, etc. The output signal of the logic gates are used to On/Off a switch in the proposed work. An exclusive gate is available for the critical situations of the switching operations. EXOR and EXNOR gates are mostly used for the operation of switches and the truth tables are given in Table 1 for both. OR gate is represented with " +", AND gate with " •", NOR gate with "+¯ ", NAND gate with " ·¯ ", EXOR gate with " ⊕ ", EXNOR gate with " ⊙ " and NOT gate with " ¯ "

The sequence of switching operation of various RSMLI's are presented in many research works with one of the modulation methods. But, to obtain the required sequence of the pulse pattern is a critical part of the presented works. Level shifting and phase shifting multi carrier sinusoidal PWM methods are widely used in the previous works [3], [5], [6]. Obtained pulse pattern from the traditional modulation method is not exactly matching with the required pulse pattern of MLI operation. To achieve the required pulse pattern, basic logic gates are used and convert the generated pulse pattern to the required pulse pattern. Analyzing the logic gates for the generation of the required pulse pattern is the major task of the MLI operation. Using the logic gates for the operation of various MLI's are not properly explained in many researchers workare proposed to achieve the cost minimization, optimal voltage stress, reduced power losses, frequency operations, less harmonic distortions. Cascaded H-Bridge, Neutral Point Clamped, Diode Clamped, and Flying Capacitors are the Conventional MLI. Operation of these conventional MLI's are performed with the support of gating signals (Pulses) to the power switches of respective inverter design.

Type of MLI	No. of DC Sources	No. of Switches	No. of Capacitors for DC- bus	Clamping Capacitors	Clamping Diodes
Diode Clamped	1	2 x (L-1)	L-1	-	(L-1) x (L-2)
Flying Capacitor	1	2 x (L-1)	L-1	(L-1) x ((L-2)/2)	-
Cascaded H-Bridge	(L-1)/2	4 x ((L-1)/2)	-	-	-

TABLE 3.2 Operating modes of Clamped Diode, Flying capacitor & cascaded H- Bridged

Level	S1	S2	S3	S4	S5	S6	S7	S8
0V	1	1	0	0	0	0	0	0
+V	1	1	0	0	0	1	1	0
+2V	1	1	0	0	1	0	0	1
+3V	1	1	0	0	0	1	0	1
+3V	1	1	0	0	0	1	0	1
+2V	1	1	0	0	1	0	0	1
+V	1	1	0	0	0	1	1	0
0V	1	1	0	0	0	0	0	0
0V	0	0	1	1	0	0	0	0
-V	0	0	1	1	0	1	1	0
-2V	0	0	1	1	1	0	0	1
-3V	0	0	1	1	0	1	0	1
-3V	0	0	1	1	0	1	0	1
-2V	0	0	1	1	1	0	0	1
-V	0	0	1	1	0	1	1	0
0V	0	0	1	1	0	0	0	0

TABLE3.4 Switching Sequence of 8 Switch Multilevel Inverter

Design of multilevel inverter with reduce switch is the novel content of many researchers. To obtain the desired output voltage level of reduced switch MLI, a different type of switching operations are performed for the switches. Microcontrollers, microprocessors, real-time simulators are used for the switching operation. Among these methods, the boolean algebra and logic gates are preferred for the operation of switches in this work as per the switching sequence.

Generation of gating signals is achieved by various pulse modulation techniques. Different pulse modulation techniques are proposed by researchers for the operation of

MLI. Control and estimation of switching losses and the total harmonic distortion is obtained by modulation techniques [3], [4]. Switching frequency is an important criterion for the operation of MLI. Based on the value of frequency modulation, techniques are categorized into two major types. Fundamental frequency with less number of cycles and high switching frequency has repeating signal per cycle.

Multilevel Inverter

4.1 Multilevel Inverter

Three types of multilevel inverter have been investigated in this dissertation.

1. Diode Clamped multilevel inverters
2. Flying Capacitor multilevel inverters
3. Cascaded H-bridge multilevel inverters
1. 2.1. Diode Clamped multilevel inverter

The main concept of this inverter is to use diodes to limit the power devices voltage stress. The voltage over each capacitor and each switch is Vdc. An n level inverter needs (n-1) voltage sources, 2(n-1) switching devices and (n-1) (n-2) diodes. 5-level diode clamped multilevel inverter

In a 5-level diode clamped multilevel:
n=5
Therefore:
Number of switches=2(n-1) =8
Number of diodes= (n-1) (n-2) =12
Number of capacitors= (n-1) =4

A 5-level diode clamped multilevel inverter has Switching states For example to have Vdc/2 in the output, switches S1 to S4 should conduct at the same time. For each voltage level four switches should conduct. The maximum output voltage in the output is half of the DC source. It is a drawback of the diode clamped multilevel inverter. This problem can be solved by using a two times voltage source or cascading two diode clamped multilevel inverters. The output voltage of a 5-level diode clamped multilevel inverter is shown in TABLE 5.1 can be seen in TABLE 5.1 all of the voltage level should have the same voltage value.

The switching angles should be calculated in such a way that the THD of the output voltage becomes as low as possible. The switching angle calculation method that is used in this thesis is the harmonic elimination method. In this method the lower dominant harmonics can be eliminated by choosing calculated switching angles. This method will be explained later in this thesis.

4.2. Flying capacitor multilevel inverters

This inverter uses capacitors to limit the voltage of the power devices. The configuration of the flying capacitor multilevel inverter is like a diode clamped multilevel inverter except that capacitors are used to divide the input DC voltage. The voltage over each capacitor and each switch is Vdc.

For a 5-level flying capacitor multilevel inverter:

n=5
Therefore:
Number of switches=8
Number of capacitors= 10

A five level flying capacitor multilevel inverter. The switching states in this inverter are like in the diode clamped multilevel inverter. It means that for each output voltage level 4 switches should be on. Table.2 shows the switching states for a 5-level flying capacitor clamped multilevel inverter. The output voltage was shown before. The switching angles like the diode clamped multilevel inverter should be calculated in such a way that the THD of the output voltage becomes as low as possible. The method is the same as the diode clamped inverter.

4.3. Cascaded H-bridge multilevel inverter

The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The number of output voltage levels are 2n+1, where n is the number of cells. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. One of the advantages of this type of multilevel inverter is that it needs less number of components comparative to the Diode clamped or the flying capacitor, so the price and the weight of the inverter is less than that of the two former types. Fig. 10 shows an n level cascaded H-bridge multilevel inverter. The switching angles calculation method that is used in this inverter is the same as for the previous multilevel inverters.

An n level cascaded H-bridge multilevel inverter needs 2(n-1) switching devices where n is the number of the output voltage level.

The output voltage of this inverter has 5 levels like in the previous multilevel inverters. This inverter consists of two H-bridge inverters that are cascaded. For a 5-level cascaded H-bridge multilevel inverter 8 switching devices are needed.

4.3.1 Level cascaded H-bridge multilevel inverter

The output voltage of the multilevel level inverter has 9 levels the like the previous multilevel inverters. This inverter consists of four H-bridge inverters that are cascaded. For a 9-level cascaded H-bridge multilevel inverter 16 switching devices are needed.

4.4. Harmonic elimination method

The switching pattern that is used in this thesis for all of the multilevel inverters is harmonic elimination method. In this method the switching angles for switches should be calculated in such a way that the lower dominant harmonics are eliminated. In this case 5-level and 9-level multilevel inverters will be investigated. For a 5-level inverter the 5th harmonic will be eliminated and for the 9-level inverter the 5th, 7th, 11th harmonics will be eliminated. The Fourier analysis needs to be calculated to determine the frequency spectra of the output waveform.

The inverter is a power electronic circuit which can convert AC to DC with a basis of two level voltages. The basic inverter is having many issues with its distortion factors, switching losses, and less efficiency. To overcome these issues, multilevel inverters are designed and analyzed by many researchers to provide better features. In the early decades, the integration of inverted power from many power electronic applications is difficult because of distortions in the converted power. The problems causing due to the voltage and current distortions, multilevel inverters are highly preferable from the family of power electronic circuits. The multilevel inverter is having a starting level with three voltage values. Multilevel inverters have been preferred with various levels like 3, 5, 7, 9, 11, 27, etc. Multilevel inverters are having many features and are mostly required for the domestic, commercial and industrial applications based on the selection of voltage and connectivity.

5.1 Result

In this paper, practical results are demonstrated for a single-phase multi-level inverter with the proposed topology as shown in Fig. 5.3. The PWM controller is implemented by a dSPACE. The output *LC* filter is used to remove high-frequency switching ripples and is a combination of a 2-μF capacitor and a 10-mH inductor. The three modules in the level generation part are SKM 50 GB, and the full-bridge module in the polarity generation part is SKM 40 GB. DC power supplies are also adjusted at 50 V. The topology is used to generate seven voltage levels for a resistive and inductive load. The output voltage is 380 VP−P. The switching frequency is 4 kHz. The PWM signals are generated for the inverter by the DSP board according to the PD-SPWM method as mentioned.

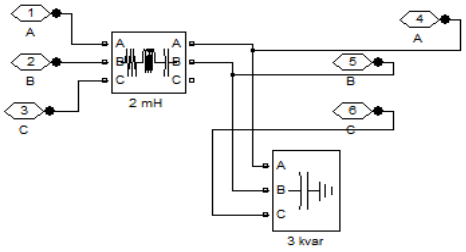

Fig 5.1 LC Filter

5.1 Simulation of Multi -level inverter with R- load

The simulation of PV based boost integrated multi-level inverter with R Load using MATLAB as shown in the figure.6.2. The output to be measured through scope as indicated. The figure 6.2 demonstrates the info voltage of the inverter from the PV board which shows the steady voltage got from the sun powered board at all periods.

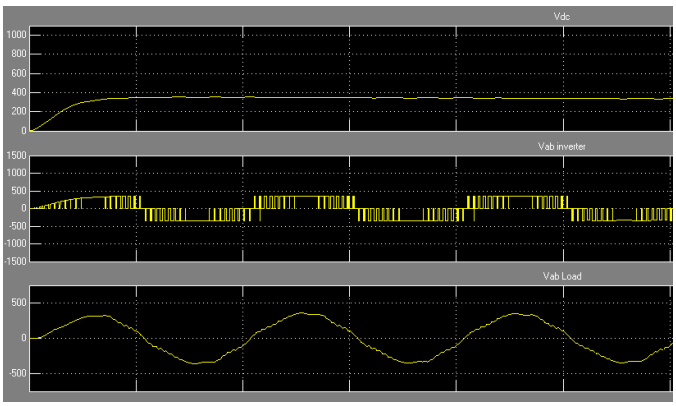

Fig. 5.2 Simulation Model for Multilevel inverter with 390 volts

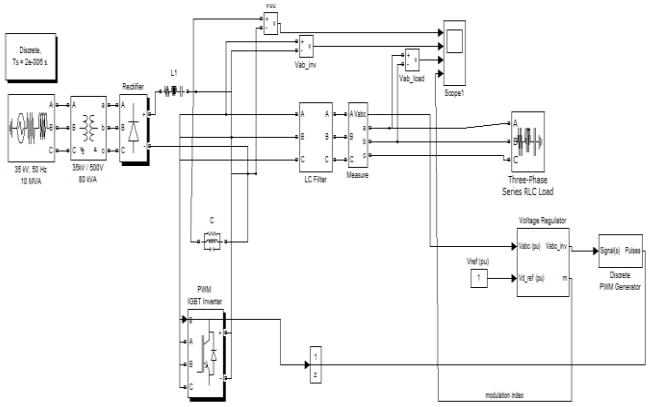

Fig. 5.3 Simulation Model for Multilevel inverter

6.1 Conclusion

In this dissertation, a new inverter topology has been proposed which has superior features over conventional topologies in terms of the required power switches and isolated dc supplies, control requirements, cost, and reliability. It is shown that this topology can be a good candidate for converters used in power applications such as FACTS, HVDC, PV systems, UPS, etc. In the mentioned topology, the switching operation is separated into high- and low-frequency parts. This will add up to the efficiency of the converter as well as reducing the size and cost of the final prototype. The PD-SPWM control method is used to drive the inverter. The PWM for this topology has fewer complexities since it only generates positive carriers for PWM control.

The experimental results of the developed prototype for a seven-level inverter of the proposed topology are demonstrated in this dissertation. The results clearly show that the proposed topology can effectively work as a multilevel inverter with a reduced number of carriers for PWM. In this dissertation the sun power-driven based boost synchronized multilevel inverter are simulated and reenacted and confirmed utilizing various load which uses sin PWM technique. The traditional inverter utilizes 7 switches to distribute 9 level wave contours together with sources where as conventional structure uses 16 switches. The proposed inverter requires single sunlight based board and diminish number of switches and incorporated lift converter which increment the info voltage of the inverter. The proposed inverter mimicked and contrasted and R, RL, RLE stack utilizing MATLAB. The archetype model uncertainly confirmed.

REFERENCES

[1] K. Jang-Hwan, S.-K.Sul, and P. N. Enjeti, "A carrier-based PWM method with optimal switching sequence for a multilevel four-leg voltagesource inverter," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1239–1248, Jul./Aug. 2008.

[2] S. Srikanthan and M. K. Mishra, "DC capacitor voltage equalization in neutral clamped inverters for DSTATCOM application," *IEEE Trans. Ind.Electron.*, vol. 57, no. 8, pp. 2768–2775, Aug. 2010.

[3] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan./Feb. 1999.

[4] T. L. Skvarenina, *The Power Electronics Handbook*. Boca Raton, FL: CRC Press, 2002.

[5] X. Yun, Y. Zou, X. Liu, and Y.He, "A novel composite cascade multilevel converter," in *Proc. 33rd IEEE IECON*, 2007, pp. 1799–1804.

[6] R. H. Osman, "A medium-voltage drive utilizing series-cell multilevel topology for outstanding power quality," in *Conf. Rec. 34th IEEE IASAnnu. Meeting*, 1999, vol. 4, pp. 2662–2669.

[7] E. Najafi and A. H. M. Yatim, "A novel current mode controller for a static compensator utilizing Goertzel algorithm to mitigate voltage sags," *Energy Convers.Manage.*, vol. 52, no. 4, pp. 1999–2008, Apr. 2011.

[8] N. Seki and H. Uchino, "Converter configurations and switching frequency for a GTO reactive power compensator," *IEEE Trans. Ind. Appl.*, vol. 33, no. 4, pp. 1011–1018, Jul./Aug. 1997.

[9] G. Shahgholiyan, E. Haghjou, and S. Abazari, "Improving the mitigation of voltage flicker by usage of fuzzy control in a distribution static synchronous compensator (DSTATCOM)," *Majlesi J. Elect. Eng.*, vol. 3, no. 2, pp. 25–35, Jun. 2009.

[10] K. Nakata, K. Nakamura, S. Ito, and K. Jinbo, "A three-level traction inverter with IGBTs for EMU," in *Conf. Rec. IEEE IAS Annu. Meeting*, 1994, vol. 1, pp. 667–672.

[11] A. Jidin, N. R. N. Idris, A. H. M. Yatim, T. Sutikno, and M. E. Elbuluk, "An optimized switching strategy for quick dynamic torque control in DTC-hysteresis-based induction machines," *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 3391–3400, Aug. 2011.

[12] K. Y. Lau, M. F. M. Yousof, S. N. M. Arshad, M. Anwari, and A. H. M. Yatim, "Performance analysis of hybrid photovoltaic/diesel energy system under Malaysian conditions," *J. Energy*, vol. 35, no. 8, pp. 3245–3255, Aug. 2010.

[13] G. M. Martins, J. A. Pomilio, S. Buso, and G. Spiazzi, "Three-phase lowfrequency commutation inverter for renewable energy systems," *IEEETrans. Ind. Electron.*, vol. 53, no. 5, pp. 1522–1528, Oct. 2006.

[14] S. Daher, J. Schmid, and F. L. M. Antunes, "Multilevel inverter topologies for stand-alone PV systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2703–2712, Jul. 2008.

[15] R. Teodorescu, F. Blaabjerg, J. K. Pedersen, E. Cengelci, and P. N. Enjeti, "Multilevel inverter by cascading industrial VSI," *IEEETrans. Ind. Electron.*, vol. 49, no. 4, pp. 832–838, Aug. 2002.

[16] D. A. B. Zambra, C. Rech, and J. R. Pinheiro, "A comparative analysis between the symmetric and the hybrid asymmetric nine-level series connected H-bridge cells inverter," in *Proc. Eur. Conf. Power Electron. Appl.*, 2007, pp. 1–10.

[17] G. S. Perantzakis, F. H. Xepapas, and S. N. Manias, "A novel four-level voltage source inverter-influence of switching strategies on the distribution of power losses," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 149–159, Jan. 2007.

[18] E. Babaei, "Optimal topologies for cascaded sub-multilevel converters," *J. Power Electron.*, vol. 10, no. 3, pp. 251–261, May 2010.

[19] G. Mondal, K. Gopakumar, P. N. Tekwani, and E. Levi, "A reducedswitch- count five-level inverter with common-mode voltage elimination for an open-end winding induction motor drive," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 2344–2351, Aug. 2007.

[20] E. Beser, B. Arifoglu, S. Camur, and E. K. Beser, "Design and application of a single phase multilevel inverter suitable for using as a voltage harmonic source," *J. Power Electron.*, vol. 10, no. 2, pp. 138–145, Mar. 2010.

[21] G. Ceglia, V. Guzman, C. Sanchez, F. Ibanez, J. Walter, and M. I. Gimenez, "A new simplified multilevel inverter topology for dc-ac conversion," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1311–1319, Sep. 2006.

[22] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2435–2443, Jun. 2011.

[23] J. Selvaraj and N. A. Rahim, "Multilevel inverter for grid-connected PV system employing digital PI controller," *IEEE Trans. Ind. Electron.*, vol. 56, no. 1, pp. 149–158, Jan. 2009.

[24] S. G. Song, F. S. Kang, and S.-J. Park, "Cascaded multilevel inverter employing three-phase transformers and single dc input," *IEEE Trans.Ind. Electron.*, vol. 56, no. 6, pp. 2005–2014, Jun. 2009.

[25] P. Barbosa, P. Steimer, J. Steinke, L. Meysenc, M. Winkelnkemper, and N. Celanovic, "Active neutral-point-clamped multilevel converters," in *Proc. IEEE 36th Power Electron Spec. Conf.*, 2005, pp. 2296–2301.

[26] S. A. Gonzalez, M. I. Valla, and C. F. Christiansen, "Analysis of a cascade asymmetric topology formultilevel converters," in *Proc. IEEE ISIE*, 2007, pp. 1027–1032.

[27] P. Lezana and J. Rodriguez, "Mixed multicell cascaded multilevel inverter," in *Proc. IEEE ISIE*, 2007, pp. 509–514.