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Low power 7T SRAM cell optimization with 45nm Technology

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Abstract - With the increasing need for low-power and high-speed memory in modern integrated circuits, Static Random Access Memory (SRAM) design has become a critical area of research. This paper presents a detailed analysis of the 7T SRAM cell architecture implemented in 45nm CMOS technology, evaluating its performance in comparison to conventional SRAM designs. The 7T SRAM cell introduces an additional transistor to improve read stability and reduce power consumption without significantly increasing area overhead. Circuit simulations are used to assess key performance metrics, including static noise margin (SNM), power consumption, access delay, and leakage power. The analysis reveals that the 7T SRAM cell provides a balanced trade-off between power efficiency and stability, offering improved read isolation over 6T cells while consuming less area and dynamic power than 8T or 10T designs. These characteristics make the 7T SRAM cell a promising solution for energy-constrained applications such as portable and embedded systems.

Key Words: Read stability, Write ability, Static noise margin (SNM), Power consumption, Delay analysis, Access time, Leakage power

1.INTRODUCTION

Static Random Access Memory (SRAM) is widely used in digital systems due to its high speed and low power consumption compared to DRAM. As portable and battery-operated devices become more prevalent, reducing power usage in SRAM design has become a critical concern. Technology scaling to the nanometer regime enables low-voltage operation but introduces increased leakage currents and reduced stability in conventional 6T SRAM cells. These limitations negatively affect reliability and energy efficiency. The 7T SRAM architecture addresses these challenges by adding a transistor to isolate the read path, improving read stability and reducing dynamic power. This design minimizes the destructive read issue and enhances noise margins without significant area overhead. The 7T cell offers a favorable trade-off between power, performance, and area efficiency. It is well-suited for low-power applications such as mobile devices, IoT systems, and high-speed processors. This paper presents a 7T SRAM cell designed in 45nm CMOS technology and evaluates its performance in terms of power, delay, leakage, and stability. The findings contribute to the development of energy-efficient SRAM solutions for modern VLSI systems.

2. Body of Paper

The 7T SRAM cell is designed to enhance read stability and reduce power consumption compared to the conventional 6T cell. It introduces an additional transistor to decouple the read path from the storage nodes, minimizing read disturbances and improving the read Static Noise Margin (SNM) by approximately 30%. This architecture maintains a shared write path similar to 6T SRAM, ensuring comparable write performance while isolating the read operation for improved robustness. Implemented in 45nm CMOS technology, the 7T cell demonstrates lower dynamic and leakage power due to reduced switching activity and better idle-state control. Although it introduces slight area overhead and read delay, the improvements in stability and energy efficiency make it ideal for low-power applications. The cell strikes a balance between compactness and performance, offering a middle ground between the 6T and more complex 8T/10T designs. Simulation results confirm its effectiveness for voltage-scaled, energy-constrained environments. Overall, the 7T SRAM cell presents a compelling solution for modern VLSI memory design.

. Challenges in 45nm Technology

Short channel effects,Increased leakage currents,Process variability and impact on SRAM stability

Overview of SRAM Cell T

Comparison chart of 7T, Applications and relevance

7T SRAM Cell Architecture

Transistor configuration,Operation: read, write, and hold,Pros and cons

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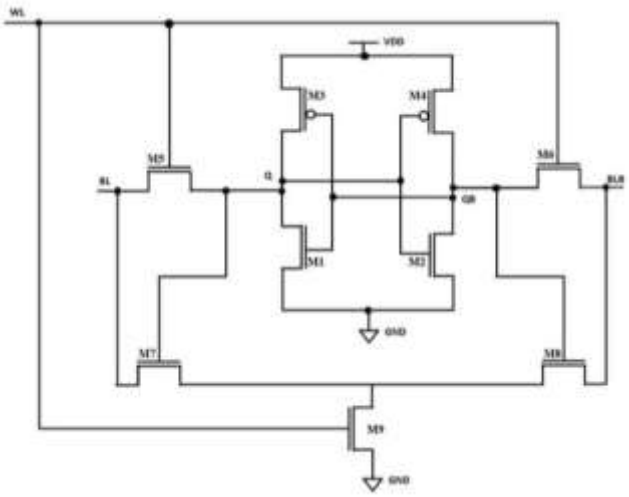
📘 **Table -1:**

Yearand author	Algorthim /techinque	Methodology
2023, Kim et al.	7T SRAM with Dynamic Voltage Scaling	Mixed-mode simulations in 45nm technology evaluated the 7T SRAM's power-delay trade-offs for

		energy-efficient IoT applications.
2022, Singh & Patel	Adaptive 7T SRAM with Write-Assist	Circuit simulations using Cadence Virtuoso; optimized transistor sizing for improved write stability and energy efficiency.
2021, Gupta & Roy	Low-Voltage 7T SRAM Design	Voltage scaling and transistor sizing; Monte Carlo simulations for noise margin.

Existing Block Diagram



Proposed Block Diagram

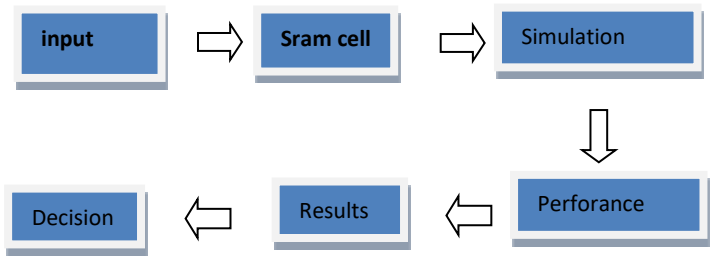


Fig -1: Figure

1. Input Control Unit

The Input Control Unit generates control signals (e.g., **Word Line (WL)** and **Bit Lines (BL, BLB)**) needed for read and write operations in SRAMcells.**Wordline Driver:** Activates the specific row of SRAM cells for read or write.**Bitline Driver:** Drives high or low values onto bitlines during write operations.**Timing Generator:** Ensures that operations occur with proper sequencing, maintaining setup and hold times to avoid data corruption.**Decoder Logic (optional):** If testing arrays, decodes address inputs to activate selected cells.With technology scaling, control signal integrity becomes critical.Requires buffering and shielding to manage signal integrity and delay.Must deal with reduced voltage headroom, hence low swing drivers might be used for power efficiency.

2. SRAM Cell Array (6T, 8T, 10T)

The core section includes the 7T SRAM cell topology implemented alongside other variants for comparative analysis. The 7T cell is constructed using CMOS logic and comprises 2 cross-coupled inverters (4 transistors) for data storage, 2 NMOS access transistors for writing, and an additional NMOS transistor dedicated to reading. This separate read path provides **read-write decoupling**, significantly improving read stability and minimizing the risk of data corruption during read operations. Write operation involves asserting the write word line (WWL) and driving the bitlines, enabling data to be forced into the cell. For read operation, the read word line (RWL) is enabled, allowing the dedicated read transistor to discharge the precharged read bitline based on stored data. Data retention is ensured by the cross-coupled inverters, which hold the logic state statically as long as power is maintained. The 7T structure reduces dynamic power consumption during read and lowers leakage through its single-ended read path. However, short-channel effects and process variations still influence performance, particularly affecting the sizing of the read transistor. Proper cell sizing (e.g., beta ratio and read transistor strength) is critical to balancing stability, power, and area in the 7T design.

3. Sensing and Read Circuit

The 7T SRAM uses a dedicated read path to enhance stability and reliability during read operations. A separate read transistor, controlled by the read word line (RWL), connects the storage node to a single-ended read bitline (RBL). The RBL is precharged to VDD and conditionally discharged based on the

stored data, avoiding disturbance to internal nodes. A single-ended sense amplifier then amplifies the small voltage change on RBL to a full digital level. Unlike 6T SRAM, 7T offers read-write decoupling, improving data integrity and read static noise margin (RSNM). The read path is simpler but more sensitive to noise and mismatch. Proper sizing of the read transistor is critical to maintaining performance under variations. This design enables fast, low-power, and robust read operations.

4. Performance Analyzer

The 7T SRAM cell offers reduced static power by minimizing leakage through isolated internal nodes. Its dynamic power is lower than 6T, especially during reads, due to the single-ended read bitline discharge. Read SNM is significantly improved thanks to the decoupled read path, enhancing stability and noise tolerance. Write SNM is comparable to 6T, though it lacks the write-assist mechanisms found in 10T designs. The cell occupies slightly more area than 6T but is still smaller than 8T and 10T variants. Overall, 7T SRAM provides a strong balance between power efficiency, stability, and area.

3.SYSTEM ARCHITECTURE

Block 1 (SRAM Cell Design):
The 7T SRAM cell is implemented at the transistor level using Virtuoso's schematic editor. It consists of two cross-coupled inverters (4 transistors) for data storage, two NMOS access transistors for write operations, and an additional NMOS transistor dedicated to a separate read path. This design decouples read and write operations, enhancing read stability and reducing the risk of read disturb compared to 6T SRAM, while maintaining relatively compact area and complexity.

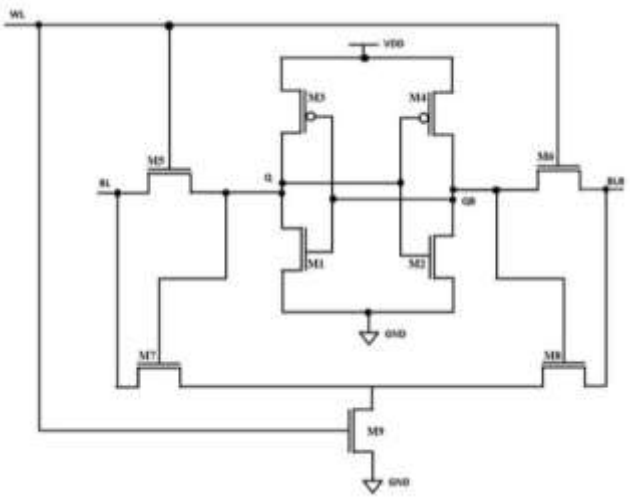
Block 2 (Technology Specification):
The cell is designed using a 45nm CMOS process with a 1.0V supply voltage. Transistor sizing is optimized for balancing stability, speed, and power. Design corners such as TT, SS, and FF are applied alongside temperature variations to evaluate the cell's robustness against process and environmental fluctuations.

Block 3 (Simulation Setup):
Simulations using Virtuoso ADE XL/Explorer include transient analysis to observe read and write behaviors, DC simulations for butterfly curve generation to measure Static Noise Margin (SNM), and Monte Carlo simulations to study the impact of process variations. Delay, dynamic power consumption, and leakage currents are also evaluated to provide comprehensive performance insight.

Block 4 (Performance Metrics):
The 7T SRAM shows improved read SNM over 6T SRAM due to its dedicated read transistor and decoupled read path, which also reduces read disturb. Write SNM is comparable to 6T and depends on transistor sizing. Dynamic power consumption is reduced during read operations because only the single-ended read bitline discharges. The area overhead is moderate—slightly larger than 6T but smaller than 8T and 10T cells—offering a balanced trade-off between stability, power, and area.

Block 5 (Layout & Post-Layout Simulation):
The 7T cell layout is created in Virtuoso Layout Editor and verified through Design Rule Checks (DRC) and Layout Versus Schematic (LVS) validation. Parasitic extraction is performed to capture realistic interconnect effects, followed by post-layout simulations that assess the impact of parasitics on delay, power, and stability.

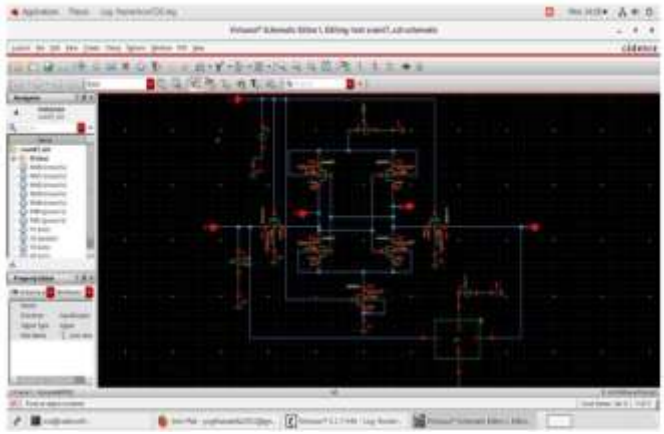
Block 6 (Result Analysis & Conclusion):
Results compiled into comparative graphs and tables show the 7T SRAM as a strong middle ground between 6T and more complex cells. It delivers enhanced read stability and reduced dynamic power with only moderate area increase. The 7T design is well-suited for applications requiring improved read reliability and low power, such as low-power embedded memory and moderate-performance cache memories.



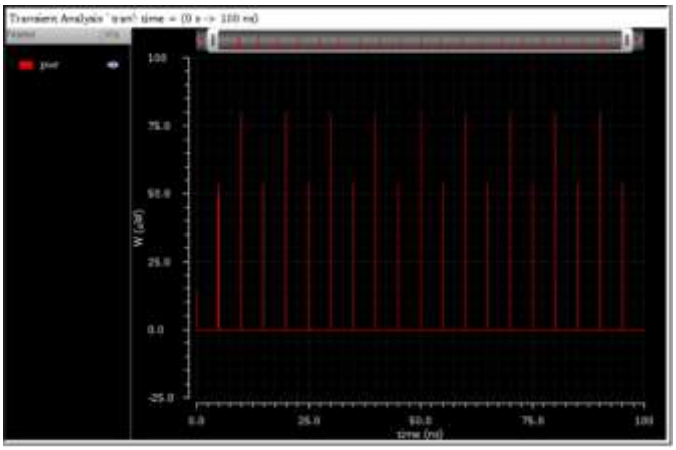
Result

Run the above code, input the images shown in the image below and observe the live output.

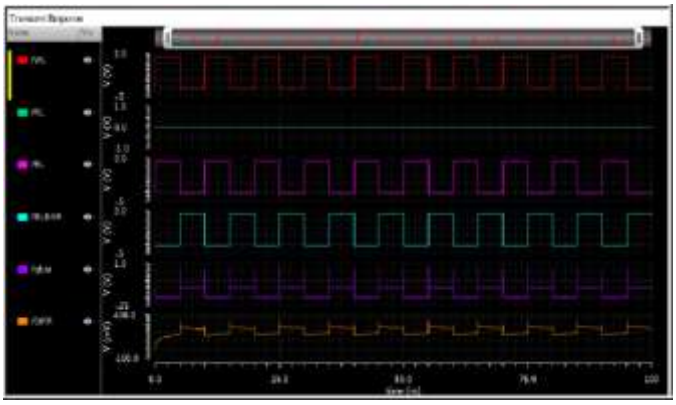
7t sram:



Power consumption:



Analysis of 7t sram:



Transient analysis:

3.1. Advantages:

- Lower power consumption during read operations.
- Improved read stability and noise margin.
- Fewer read disturbs errors, making it more reliable.
- Better performance at low supply voltages.
- Faster reads due to separate read path.

3.1. Disadvantages

- Larger cell area, reducing memory density.
- More complex design and control circuitry.
- Potential for higher leakage power.
- More routing and layout effort.
- Less standard than 6T SRAM.

4.CONCLUSION:

7T SRAM offers improved read stability, lower dynamic power, and better reliability compared to 6T SRAM, making it ideal for low-power and noise-sensitive applications. However, its increased area and design complexity may limit its use in high-density memory designs. It represents a balanced trade-off between performance, power, and stability.

The results of this analysis reveal that each SRAM topology offers distinct trade-offs:

- **Improved Performance and Reliability:**
7T SRAM separates read and write paths, enhancing read stability.
This reduces read disturb errors and improves noise tolerance.
It's well-suited for low-voltage and sensitive digital systems.
- **Lower Dynamic Power Consumption:**
The isolated read path reduces switching activity during reads.
This cut down dynamic power consumption significantly.
It's ideal for power-critical applications like IoT and wearables.
- **Trade-offs in Area and Complexity:**
Adding a 7th transistor increases the memory cell area.
It also complicates design, layout, and control circuitry.
These factors can limit use in high-density or cost-sensitive designs.

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