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Low Power CMOS Amplifiers for Wireless Application: A Review

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Abstract- *In this review paper, we have studied about the different technique and topologies of configuring wide-band, low-power, low-noise CMOS amplifier for wireless and broadband application. Different simulation tools have been used in past to configuring CMOS amplifier. It is clear that the complementary compound pair topology is more suitable to design the low power, low noise wideband CMOS amplifier for wireless application. In this technique inductor play very important role to improve frequency band of wireless communication.*

Key words- *Low pass filter, Low noise, low power consumptions, cmos , complimentary compound*

1. Introduction

In last two decades, there is a lot of pressure on electronic industries and researchers to design wide band, low power, low noise CMOS amplifier for wireless applications. Wireless amplification is growing day by days. It is very challenging task for electronic industries to configure such amplifier. High speed, very low noise, high data rates, cheap, low power consumptions are parameters of high performance in the broadband communication, compact
designs are remarkable demands in electronics industries competition [1]-[2]. In wireless communication systems broadband amplifiers play very important role to transfers the larger data. Fig.1 shows that symbolic diagram of wireless communication system.

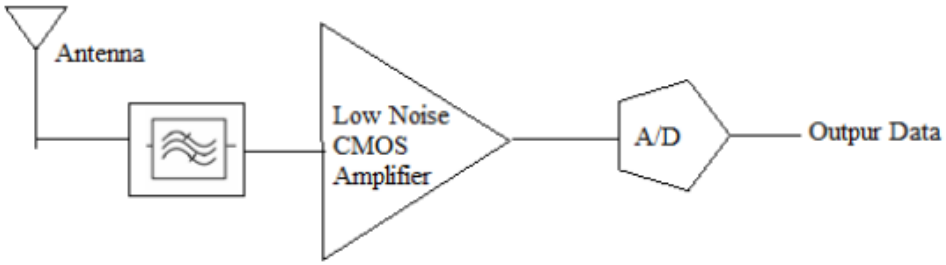

FIGURE 1: Wireless Communication System for Broadband Applications

In above figure, low noise amplifiers could be replaced by CMOS amplifiers of high bandwidths, low noise and low power consumptions. In heterodyne receiver for communication low noise using CMOS technology is an important input part to amplify the weak signal with low noise and is usually preceded by a filter (reject the undesired and unwanted signals) [3]-[10].

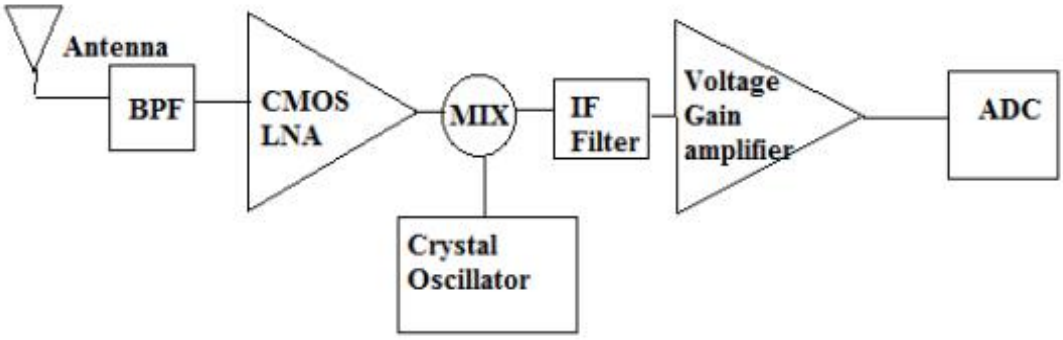

Figure-2: Heterodyne Receiver for Communication System

2. Survey of the Existing Work: Literature Review

There is necessary requirement for wireless communication to make nano devices use as a portable device with high bandwidth wireless applications. It is very critical challenge like power consumption, high gain, low noise high linearity [10]-[15]. Many researchers have presented the ideas to designs the low power low noise CMOS amplifiers using different topology for various application purpose [16]-[20].

In this literature review presents existing work done by various researchers and authors in the electronics communications field to designs CMOS amplifiers. Last two decade so many topologies have been used to achieved high performance of CMOS amplifiers which are given below-

1. Current reuse topology
2. Cascade common source amplifiers topology
3. Source degeneration topology
4. Resistive feedback topology
5. Cross coupled capacitor technique
6. gm- boosted topology
7. Noise cancellation technique
8. CMOS Active inductor etc.

TABLE-1: Comparison Table of Above Literature Survey

S. no.	Year	Topology	Frequency range	Gain	Noise figure	Power consumption
1	2005 [6]	Cross Coupled Gm Boosting Topology	Maximum 6GHz	-	3dB	30mA current consumption
2	2006 [7]	**B**oost the transconductance	Maximum 960 MHz	13 dB	3.6 dB	0.72 mW
3	2007 [8]	Noise Cancellation Topology	3.1-10.6GHz	9.7dB	4.5-5.1dB	20mW
4	2008 [9]	Resistive Inductive Topology	Maximum 3GHz	12dB	3.3dB	30mW

5	2008 [10]	Current Reused Topology	3.1-12.2GHz	13.1dB		13.9mW
6	2009 [11]	gm-boosting from inductively degenerated topology			2 dB	2.6mW
7	2010 [12]	Current Reused Topology	3-10GHz		3.4+0.36dB 3.4-0.36dB	14.8mW
8	2012 [13]	Current reused boosting topology	3-5 GHz	-	-	-
9	2013 [14]	Source Degeneration Topology	3 GHz - 7.5GHz		4.6-5.3dB	
10	2015 [16]	Current Reused Technique and Cascade Common Source Amplifier.	10 GHz	-		
11	2016 [17]	Common Gate Cascade Topology	3.1GHz-10.6GHz	22.1dB		1.3mW
12	2017 [18]	Noise Cancellation, Current Reused, Source Degeneration And Resistive Feedback	3 GHz-12 GHz		1.721dB	23.23mW
13	2018 [19]	CMOS Active Inductor Topology	3.1GHz-10.6GHz	10.74+ 0.01dB	4.85dB	
14	2019 [20]	Cascade Configuration With Resistive Feedback	3.5GHz-31GHz		Less than 4.5dB	
15	2020 [21]	Complementary Compound Pair	64.4 GHz			20.88µW
16	2021 [22]	Improved Complementary Derivative Superposition (ICDS) technique Forward Body Bias (FBB)	3.1-10 GHz	10.5 dB	2.5-4 dB	06 mW

17	2022 [23]	current-steering cascode g_m boosting body floting	71.6-89.5GHz	20 dB	5.5 dB	23mW

3. CONCLUSION

According to the above literature survey of existing work, various topologies have been used to design ultra-wideband low power, low noise amplifier. After this survey of literature, it is clear that the complementary compound pair topology is more suitable to design the low power, low noise wideband CMOS amplifier for wireless application. In this technique inductor play very important role to improve frequency band of wireless communication.

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5. REFERENCES

1. Robert L. Boylested and Louis Nasnelsky Electronics devices and circuit theory Prentice Hall is an Imprint of Pearson, tenth edition, pp. 578-582 (2009).
2. Intel UWB website: http://www.intel.com/technology/ultrawideband/
3. B. Razavi, Design of Integrated Circuits for Optical Communications, McGraw-Hill, 1st ed, September 2002.
4. G. R. Aiello, "Challenges for ultra-wideband (UWB) CMOS integration", IEEE MTT-S International Microwave Symposium Digest, vol. 1, pp. 361 -364, 8- 13 June 2003.
5. Nell H.E. Weste and Kamran Eshraghian, "Principal of CMOS VLSI Design", Reprinted with June1988.
6. Zhuo, W. Li, X. Shekhar, S. Embabi, S.H.K. Pineda de Gyvez, J. Allstot, D.J. and Sanchez-Sinencio, "A Capacitor Cross-Coupled Common-Gate Low-Noise Amplifier' IEEE Transactions on Circuits and SystemsII: Express Briefs. 52:875-879 2005.
7.] Wang, S.B.T. ; Niknejad, A.M. and Brodersen, R.W, "Design of a Sub-mW 960-MHz UWB CMOS LNA", IEEE Journal of Solid-State Circuits. 41: 2449-2456 2006.
8.] Chin – Fan Liao, Shen – Iuan Liu, "A Broadband Noise Cancelling CMOS LNA for 3.1 - 10.6 Ghz UWB Receivers", IEEE Journal Of Solid State Circuits, Vol. 42, No. 2, February 2007.
9.] Kambiz Moez and M. I. Elmasry, " A Low Noise CMOS Distributed Amplifier for Ultra Wide Band Applications", Article In Circuits And System II: Express Briefs; IEEE Transaction on 55 (2) : 126 –130, March 2008
10. Zhe – Yang Huang, Che – Cheng Huang, Yeh – Tai Hung, "A CMOS Current Reused Low Noise Amplifier for Ultra Wideband Wireless Receiver", Microwave and Millimeter Wave Technology, IEEE Explore, ICMMT -2008, vol.3.

11. Joo, S. ; Choi, T.Y. and Jung, B. 2009. 'A 2.4-GHz Resistive Feedback LNA in 0.13-µm CMOS' IEEE Journal of Solid-State Circuits. 44: 3019-3029
12. I - Chuan Chen and Jeng -Rern Yang, "3 -10 GHz CMOS Distributed Amplifier Low Power Low Noise and High Gain Low Noise Amplifier for UWB Systems", Article in TENCON 2010.
13. Khurram, M. and Hasan, S.M.R, "A 3–5 GHz CurrentReuse g_m-Boosted CG LNA for Ultra wideband in 130 nm CMOS", IEEE Transaction on Very Large Scale Integration (VLSI) Systems. 20: 400-409.
14. Jun Da Chen, "A Low Power Ultra Wide Band LNA in 0.18 µm CMOS Technology", Article in Active and Passive Electronic Components 2013: 1 -10.
15. Xiao – Peng, Wen Lin Xy, and Chen Feng, "A 11.2mW, 48 - 62 GHz LNA in 60nm CMOS Technology", Article in Circuits System and Signal Processing, Aug. 2015.
16. Amir. Mahdavi and Fatemeh .Geran, "A Low power UWB CMOS Low Noise Amplifier for 3.1-10.6 GHz in Receivers", 8th International Symposium on Telecommunications (IST'2016), PP.567-600.
17. Monsen Hayati, Sayad Cheraghali, "Design of UWB LNA using Noise Cancelling and Current Reused Technique", ICCCNT, 2017.
18. S.Manjula, M.Malleshwari, and M.Suganthy, "Design of Low Power UWB CMOS Low Noise Amplifier using Active Inductor for WLAN Receiver", International Journal of Engineering & Technology, 7 (2.24) 448- 452, 2018.
19. Jiaqian Wu and Zhangfa Liu, "A 40nm CMOS Ultra-Wideband Low Noise Amplifier Design", Advances in Computer Science Research, International Conference on Wireless Communication, Network and Multimedia Engineering (WCNME 2019), vol.89
20. Tiwari, Raj Kumar, and Shiksha Jain. "GHZ Bandwidth Low Power Low Noise CMOS Amplifiers Using Different Topologies for Wireless Applications." International Research Journal of Engineering and Technology (IRJET) 7.10 (2020): 2395-0056.
21. Tiwari, Raj Kumar, and Shiksha Jain. "Complementary Compound Wide-band Amplifier for Broadband Communication System." International Journal of Advanced Research in Engineering and Technology (IJARET) 11.6 (2020).
22. Yaghouti, Behnam Dorostkar, and Javad Yavandhasani. "A high linearity low power low-noise amplifier designed for ultra-wide-band receivers." *Analog Integrated Circuits and Signal Processing* 107, no. 1 (2021): 109-120.
23. Wang, Yunshan, Tzu-Yang Chiu, Chun-Chia Chien, Wei-Hsuan Tsai, and Huei Wang. "An E-Band High-Performance Variable Gain Low Noise Amplifier for Wireless Communications in 90-nm CMOS Process." *IEEE Microwave and Wireless Components Letters* (2022).