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Low-Power Redundant-Transition-Free TSPC Dual-Edge-Triggering Flip-Flop Using Single-Transistor-Clocked Buffer

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Abstract

In the modern graphics processing unit (GPU)/artificial intelligence (AI) era, flip-flop (FF) has become one of the most power-hungry blocks in processors. To address this issue, a novel single phase-clock dual-edge-triggering (DET) FF using a single-transistor clocked (STC) buffer (STCB) is proposed. The STCB uses a single-clocked transistor in the data sampling path, which completely removes clock redundant transitions (RTs) and internal RTs that exist in other DET designs. Verified by post-layout simulations in 22 nm fully depleted silicon on insulator (FD-SOI) CMOS, when operating at switching activity, the proposed STC-DET outperforms prior state-of-the-art low power DET in power consumption It also achieves the lowest power-delay-product (PDP) among the DETs.

Keywords: Dual edge triggering (DET), dynamic power, flip-flop.

1 Introduction

Power consumption is a major challenge for CMOS designers, especially with artificial intelligence (AI) applications of neural network processors and graphics processing units (GPUs). The digital processing power required to train recycling intelligence doubles every 3.4 months [1]. In modern processors, time can account for 50% of the total energy consumption [2]. Therefore, it is very important to optimize the effort to meet this challenge of power loss. The main components of a clock control system are flip-flops (FF) and clock distribution networks. Clock-based clock cycles only use one clock cycle at a time to process incoming data, resulting in higher power consumption for data that was not designed for processing.

In contrast, dual-additive (DET) devices use two clock edges, allowing half the clock frequency while maintaining output. Flip-flops are an important part of digital electronics and computer architecture. This fine-grained logic circuit can store and modify binary data. Flip-flops are important for building memory devices, registers, counters and various sequential logic circuits. These components work on clocks, which are signals that coordinate the operation of digital circuits. The timing of the clock signal determines whether the flip-flop is saved or released Data Two common types of flip-flops are the SR (set-reset) flip-flop and the D (data) flip-flop.

1.2D Flip-Flop:

A D flip-flop has one input, one D (data) input, and two outputs: Q and $\overline{Q}$. Input D indicates the state of output Q. When the clock signal is on, input D is sent to output Q. If input D is high (1), output Q is also high, and conversely, if the input D (0) is low, the output Q will be low. The output Q becomes the inverse of Q. Flip-flops are commonly used in digital systems for data storage, synchronization and control. By connecting multiple flip-flops together, complex sequential circuits such as registers and counters can be created, which form the basis of many digital devices and systems, including computers, calculators, and communication tools. The concepts of double-ended and single-ended trigger apply to the behavior of flip-flops and other sequential logic circuits with respect to clock signals.

1.2.1 Edge Triggering:

Edge triggering indicates that a flip-flop changes its state only certain edge of the clock signal. An example of positive edge activation is the flip-flop, which displays the input and only updates its status when the clock signal changes from low to high (rising edge). During the low-to-high transition, the flip-flop remains stationary while the next rising edge rises. This method of stimulation is common in most cases.

1. 1 SR turn:

An SR flip-flop has two inputs: input S (set) and input R (set), and outputs Q and Q (the complement of Q). Activation of input S sets output Q to 1, activation of input R resets Q to 0. Output Q acts as an inverting of Q. If the two entries at the same time, a problem called "race mode" may occur. Not defined 1. 2D rotation:

design criteria. Single card activation is less complicated and is usually sufficient for most digital systems. However, dual switching can be useful when designing high-speed circuits, when implementing special protocols, or providing precise control.

1.1 Single Transistor Clocked Buffer:

A basic virtual circuit called a signal-to-switch clock, also known as a signal-to-signal clock or a one-to-one switch, can amplify and distribute a binary signal indicated by the orange symbol. Virtual architectures often use it to route and isolate signals between different circuits. A transistor (usually a MOSFET or CMOS) and a clock signal form the clock signal of the transistor signal. The resistor works in a periodic square wave known as a clock signal. Depending on the design, the transistor controls whether the input signal goes to the output when the clock signal is alive (high or low). When the clock signal is not active, it turns off the clock and separates the single-switch clock, called a digital clock, or transistor signal clock, is a reliable digital circuit capable of transmitting and amplifying binary signals that can be determined using clock signals. They are often used in virtual infrastructure to feed and separate signals between multiple components in a circuit. A single-transistor clock is a clock signal with a single transistor (usually a MOSFET or CMOS transistor). The operation of the clock is controlled using a clock signal, which is a typical square wave. The transistor controls the input signal and transmits the output time when the clock signal is alive (high or low depending on the design). The transistor is turned off and is effectively removed from the circuit when the clock signal does not turn off strength.

1.4Transmission-Free TSPC:

TSPC is a design method for sequential logic circuits aimed at developing efficient flip-flops or bistable memory devices in digital applications. Its high speed and low power requirements make it a great asset. Older flip-flops and bistable memory devices often required switching gates or switching transistors to transfer data in

1.2.2 Dual-Edge Triggering:

The lock has the ability to change its position to either end of the clock signal using a double-trigger, as opposed to reverse mode. The flip-flop has the ability to sample the input and adjust its position in phases of low-to-high (rising)and high-low(fall). This greatly simplifies the design of sequential logic circuits. Although less common than a single switch, a double switch is used in special applications where there is a long time. Requirements are required. Single or dual integration is an option based on specific use cases and causes internal nodes to grow or collapse in response to data input

- **Toggle:** When the evaluation phase ends, the evaluation signal is turned off and the internal values are retained until the next clock cycle. The output of the flip-flop is obtained from these stored values.

Gearless TSPC has advantages such as low power consumption, high speed and simpler circuit compared to flip-flops. Redundancy is achieved by using redundant logic signals to control the behavior of internal nodes, thereby eliminating the need for switch gates.

However, non-switching TSPC has disadvantages, such as increased chip area and susceptibility to clock errors or noise. Ultimately, the suitability of this design method depends on the unique needs and limitations of the virtual circuit being designed. A major challenge for virtual CMOS designers is power consumption, especially with the demands of today's GPUs and social AI processors. The processing energy required to train AI doubles every 3.4 months [1]. In a modern CPU, up to 50% of the total power can be consumed by the system clock [2]. As a result, energy optimization is considered a key factor in tackling the aforementioned energy loss challenge. Flip flops (FFs) and Clock distribution networks are the primary components of a processor clock system. A conventional single-phase clock system with FFs one clock page at a time, and considering an active clock page without the help of calculations, leads to a high energy consumption. In contrast, dual-domain FFs (DETs) can use each clock edge to handle data at half the clock frequency while maintaining output. To reduce power consumption, a new DET FF physiograph using a reliable single-phase clock (TSPC) is proposed. A number of low-power, flip-flop and close-coupled devices have been developed. One of the challenges with DET FFs is that the current

the clock cycle, resulting in fatigue and increase energy consumption. TSPC solves these problems by eliminating the need for transmission port, leading to better performance and reduced power consumption. In a non-transitional TSPC, the flip-flop operates in two different stages: preload and evaluation. Here is a brief explanation of how it works:

2 **Pre-charge stage**: In the pre-charge stage, a pre-charge signal is initiated which increases the internal voltage of the flip-flop to a certain level. This process causes internal nodes to start at a defined state before moving to the evaluation phase

3 **Evaluation phase**: During the evaluation phase, an input signal is sent to the flip-flop. The evaluation signal, which is different from the previous signal, appears. This process

effectively doubles the clock frequency. As a result, the speed and performance of the digital circuit can be improved without requiring major modifications to the existing circuit. STCDET is used in many digital systems, with high-speed processors, memory interfaces, and real-time architectures, where increasing the clock frequency is important for optimal performance.

1.5 Application

4 Asynchronous FIFOs:

STCDET flip-flops are commonly used in the design of asynchronous First-In-First-Out (FIFO) buffers. Asynchronous FIFOs are used in scenarios where data is transferred between two asynchronous clock domains. The STCDET flip-flops enable the efficient capture and release of data in the FIFO, ensuring proper synchronization and preventing data loss.

5 High-velocity Serial Data Communication:

STCDET flip-flops are employed in high-velocity serial data communication systems, such as high-speed serial interfaces (e.g., PCIe, USB, Ethernet), optical communication systems, and high-speed serializers/deserializers (SerDes). The ability to operate at high data transfer rates and handle bidirectional data streams makes STCDET flip-flops suitable for efficient data transmission and reception.

6 Pipelining and Data Processing:

STCDET flip-flops find applications in pipelined architectures, where data is divided into sequential stages to improve throughput and overall system performance. consumption of the clocks is not very high, as some transistors can switch even though the input data has not changed due to the circuit design. A single transistor clock double-edge excitation method (STCDET) increases efficiency. And the operation of clock signals in digital circuits can be done by one of the rising and falling edges of the clock signal, effectively doubling the operating clock frequency. Traditionally, virtual circuit operations are synchronized with increasing clock margin, which limits the speed of operation. STCDET enables this limitation by using two clock edges. The basic concept behind the STCDET is to implement a single transistor to generate a non-overlapping clock signal, one for the rising edge and one for the falling edge. This is done by using a transistor as a switch to control the discharge of the capacitor. When the transistor is turned on, the capacitor is charged, and as it is turned off, the capacitor is discharged, creating a falling clock signal. In this way, work can be done on all sides The clock signal
while providing multiple parameters. Then again, the Express Pulse Static Flip-Flops (ep-SFF) has the highest operating power, which makes it suitable for the most important paths inside the design. To further lessen the energy consumption, we also examine the dual-edge triggered flip-flops. Our results show that dual-edge triggered design always leads to large area loss and poor performance, which significantly limits its applications. We propose a novel net-pulsed dual-edge flip-flop that matches the performance of single-edge flip-flop while using less power in the flip-flop and clock distribution network.

Y. Lee, G. Shin and Y. Lee, "A Fully Static True-Single-Phase-Clocked Dual-Edge-Triggered Flip-Flop for Near-Threshold Voltage Operation in IoT Applications," in *IEEE Access*, vol. 8, pp. 40232-40245, 2020

This paper presents a double edge triggered (DET) flip-flops (FFs) that may operate reliably at low voltage. Unlike traditional single edge triggered (SET) flip-flops, the DET-FF improves performance by locking data inputs between two clocks. When combined with the requirements of energy usage, significant performance improvements are expected. but, previous DET-FFs designs had been difficulty to technique, voltage, and temperature (PVT) variations, which limited their performance as electronic controllers to a lesser extent. The high static, precision single-phase

By capturing data on both clock edges, STCDET flip-flops enable the design of high-speed and efficient pipelines for tasks like arithmetic and logic operations, digital signal processing, and microprocessor instruction execution.

7 Data Synchronization:

In systems that require synchronization of data from multiple sources, STCDET flip-flops can be used to ensure accurate and reliable data capture. By utilizing both clock edges, STCDET flip-flops provide robust synchronization capability, mitigating issues related to clock skew, metastability, and data integrity.

2 LITERATURE REVIEW

J. Tschanz, S. Narendra, Zhangping Chen, S. Borkar, M. Sachdev and Vivek De, "Delay and Power Comparison of Single-Edge and Double-Edge Pulsed Flip-Flops for High-Performance Microprocessors", ***Proceedings of ISLPED 01:2001 International Symposium on Power Electronics and Design (IEEE Cat.01) No.01TH8581), Huntington Beach, CA, ABD, 2001, s. 147-152***

Flip-flops and latches play an essential position inside the design, affecting the delay and power performance. We analyze different types of single-edge flip-flops, such as partial and static transitions with discrete and discrete signals. Among them, we introduce the Implicit Pulse Semi-Dynamic Flip-Flops (ip-DCO), which achieves the lowest put off compared to other flip-flops
frequently suffer from some real-time overlap between the master clock and at output clock. This overlap can lead to cell conflicts and poor performance, especially when working on laboratory equipment and as an alternative to nanotechnology. This paper introduces a new static DET flip-flops (DET-FFs) that does not need to operate in reverse clock, has a single-phase real clock, thus eliminating the risk of clock overlap. The DET FF concept is used in standard 40nm CMOS technology and demonstrates all the capabilities that conventional DET-FF cannot provide at low power consumption. At a supply voltage of 500 mV close to the threshold, this implementation also provides 35% decrease CK-Q postpone and lowest output voltage as compared to all DET-FF implementations.

clocked DET-FFs is designed to offer strong operation down to near-end voltages. Instead of two-stage or pulse clock scheme in traditional DET-FF, true single-stage clock (TSPC) scheme is used to conquer clock overlap problem and hold working strength low. The use of full static also enables efficient operation at low voltage. The DET-FFs concept is built on 28nm CMOS era, and a comprehensive evaluate which include post-configuration Monte Carlo simulation is performed to demonstrate the design accuracy, with multiple PVT ranges. Analysis and comparison with state-of-the-art DET-FFs confirm that the proposed DET-FF can operate at minimum voltage of 0.28 V in the temp. range of -40Â°C to 120Â°C, while retaining near-excellent durability. performance and power supply.

Bonetti, A. Teman, and A. Burg,"Indeed, single-stage clocked double-edge-triggered flip-flops are uncontroversial," ***in 2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, Portugal, 2015, pp. 1850-1853***

Dual Edge Trigger (DET) synchronous operation is a good choice for low-cost, excessive-overall performance models. DET operation provides the same output at half of the clock frequency as compared to the traditional part synchronous system. This can save the power of the network clock, which is often significant in overall power consumption. But, so one can use the DET function, unique names must be selected for the sample data of the two clocks. These notebooks are greater complicated than single notebooks and
transistors required. New DET-FFs circuits (one static, the alternative dynamic) are proposed in wherein the number of transistors is decreased to a number of just like the classical single edge triggered flip-flops (SET-FFs). The two new circuits aren't only efficient when operating at excessive frequencies, but additionally have right resistance to metastability issue (static) and collision issue (dynamic), and are now available in easy figure-of-eight and flat-of-eight configurations. These considerations enable a general and cost-effective implementation of DET-FFs in VLSI system design.

P. Zhao, J. McNeely, W. Kuang, N. Wang and Z. Wang, "Design of Sequential Elements for Low Power Clocking System," in ***IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*****, vol. 19, no. 5, pp. 914-918, May 2011**

R. Hossain, L. D. Wronski, and A. Albicki, "NTUG-triggered flip-flops with low-power design," *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 1 2. No. 2, pp. 261-265, June 1994*

On this paper, we examine the energy financial savings finished via the usage of double-edge triggering (DET) in place of single-edge triggering (SET) flip-flops. We start this paper via introducing a brand-new set of D-type double-edge induced flip-flops that may be used with fewer transistors than preceding designs. Architecture-level investigation, analysis, and simulations compare the energy intake of the flip-flops to single-edge triggered flip-flops. The analysis consists of an application-impartial study of the results of enter coupling on power dissipation in single- and double-edge triggered flip-flops. On the system degree, power savings are performed by means of the use of the registers of double-edge flip-flops as opposed to single-edge flip-flops. The consequences are very promising, showing that two edge-triggered flip-flops can provide sizable power savings with very little complexity overhead.

P. Zhao, J. McNeely, P. Golconda, M. A. Bayoumi, R. A. Barcenas, and W. Kuang, "Low-power clock branch sharing two edge-triggered flip-flops," *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 15. No. 3, s. 338-345, Mart 2007*

A revolutionary technology for dual low-power flip-flops is presented in this paper. The brand-new technology uses an integrated clock to lessen the number of clock transistors with in the design. The new layout also uses the release process and the manoeuvring process to reduce the transfer and brief-circuit current, respectively. By contrast, the new CBS_ip design achieves a 20% power gain and 12% power yield in comparison to other double edge flip-flop designs.

A. Gago, R. Escano and J. A. Hidalgo, "Reduced implementation of D-type DET flip-flops," in *IEEE Journal of Solid-State Circuits*, vol. 28, no. 3, pp. 400-402, March 1993

One of the disadvantages of using dual D-type flip-flop (DET-FF) in VLSI system layout is the variety of interfaces. This paper covers the layout and analysis of AHB,

Energy consumption is the main source of physical activity and is listed as one of the three main demanding situations within the "International Semiconductor Technology Map 2008". reasons. This paper analyzes various designs for systems with weak clock speeds. A good way is to reduce the load capacity of the clock, reduces the Varity of clock transistors. To clear up this hassle, we recommend a new clock pair multi-flip-flops that reduces the wide variety of local clock transistors by way of 40%. Clock driver power is reduced by 24%. Additionally, low swing and dual-edge clocks can be effortlessly included into new flip-flops to create clocking structure.

S. Lapshev and S. M. R. Hasan, "New Low Glitch and Low Power DET Flip-Flops Using Multiple C-Elements," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 10, pp. 1673-1681, Oct. 2016

This paper presents a new design of a static double-edge static flip-flop (DET) that exhibits particular circuit behavior because of the inclusion of C factor. It includes five new DET flip-flops, together with high-overall performance models and others that enhance upon traditional Latch-MUX DET flip-flops to ensure that their inner circuits do not respond to signal changes. A special feature of the proposed flip-flops is the minimal power loss from input burrs. Through simulations on excessive-overall performance 28 nm CMOS era, the new DET flip-flop is compared with existing models, exhibiting good traits consisting of power consumption and fire. The Power Delay Product (PDP) has undergone many changes. big Monte Carlo and electrical scaling simulations demonstrate the robustness of the design against PVT variations.
AHB (Advanced High Performance Data Path) is a high-speed communication interface within the AMBA (Advanced Microcontroller Data Path Architecture) framework. It works as a well-known for communication between modules inside the machine. The AHB specification is described by using ARM and facilitates the interaction between on-chip memory, processor and stale-chip external reminiscence

which incorporates one major and 4 slave devices. on this take a look at, the AHB protocol includes major components, which are the main unit, slave unit, decision maker and multiplexer. The AMBA-AHB protocol works with any design as long as it meets the AHB standards. Components such as master, slave, decoders and multiplexers are designed using Verilog, while the verification center is designed using System Verilog (SV). Designs are simulated and verified using Mentor Graphics' advanced verification tool Questa Sim, which is also used to evaluate code and performance.

V. L. Le, J. Li, A. Chang and T. T.-H. Kim, "0.4V, 0.138fJ/cycle single-phase-clock-redundant-transition-free 24T flip-flop using transition detection scheme in 40 nm CMOS," ***IEEE Solid-State Circuits Magazine, vol. 53, no. page 10. 2806-2817, October 2018***

This paper presents a low-voltage and occasional-voltage single-section clockless switchless flip-flop (FF) called switching-sensing FF (CSFF). Using a local switching strategy to eliminate irregular changes in the internal clock, CSFF consumes no power when there is no data processing. Measurements on test wafers fabricated with 40nm CMOS generation show that CSFF can save as much as 90% in electricity consumption with 5% data efficiency compared to traditional switch-gate FF (TGFF) without the need for additional transistors. At 0.4 V and 10% efficiency, CSFF consumes handiest 0.138 fJ/cycle, that is 84% decrease than TGFF.

In addition to improving electricity and electricity efficiency, CSFF plays improves overall performance and minimizes running costs. Wafer measurements show that CSFF performs well at voltages as low as 0.19 V and provides a 37% improvement in latency over TGFF in the 0.4-1 V supply range.

3.1 TANNER TOOL Launching S-Edit

To release S-Edit, double-click on at the S-Edit icon

Fig 3.1 To release S-Edit, double-click on at the S-Edit icon.

The consumer interface includes the elements proven below. Until you explicitly retrieve a setup file, the placement, docking repute and different show traits are stored with a design and can be restored whilst the layout is loaded.

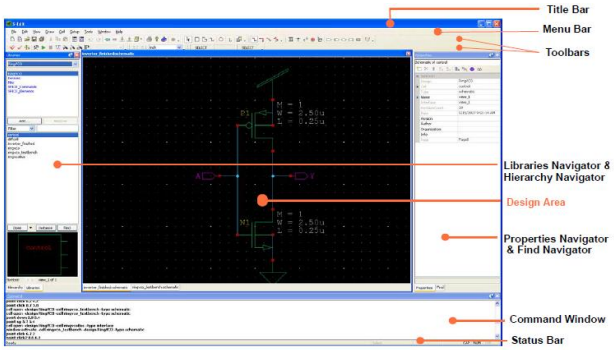

Fig 3.2 Parts of the User Interface

3.1.1 Parts of the User Interface

3.1.1.1 Name Bar

The name bar suggests the name of the modern-day cell and the view kind (symbol, schematic, etc.).

3.1.1.2 Menu Bar

Fig 3.3 Title Bar

The menu has an S-Edit menu title. The menu that appears may additionally vary depending at the form of operation. For information about the many ways S-Edit provides to execute commands, see "Shortcuts for Viewing Cells and Instructions" on page 70.

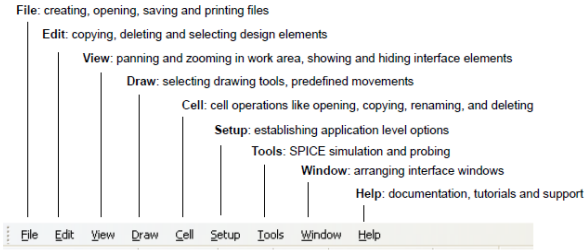

Fig 3.4 Menu Bar

3.1.1.3 Menu List Filtering

Maximum S-Edit menus and dialog boxes hurry filtering to hurry up the selection system from drop-down lists. This is, while you input a character, S-Edit will leap to the primary list of items that start with that individual. As an instance, typing **g** will display the primary list of products that start with that letter and filter the screen to expose products that start with **g**. If **u** enter after **g** will display the primary list of products that start with **gu** and filter the screen to reveal products that begin with **gu**, etc. The search process is not important.

3.1.1.4 Toolbars

You could show or disguise individual toolbars the use of the **View > Toolbars** command or via clicking inside the toolbar area. Toolbars may be customized and positioned as needed. For delivered comfort, S-Edit

Fig 3.11 Mouse Buttons Toolbar

Mouse buttons range in feature in set with the tool that is energetic. The **Shift**, **Ctrl** and **Alt** keys in addition exchange the feature. For two-button mice, the center-button feature is accessed by using clicking the left and proper buttons on the same time, or via urgent **Alt** at the same time as clicking the left mouse button.

8 Customizing Toolbars

You may upload buttons for present instruction to current S-Edit toolbars, add completely new toolbars, and upload new buttons for completely new instruction to both new or present toolbars.

To customize toolbars, right-click on everywhere with in the toolbar place and click on **personalize inside the** in the context-touchy menu.

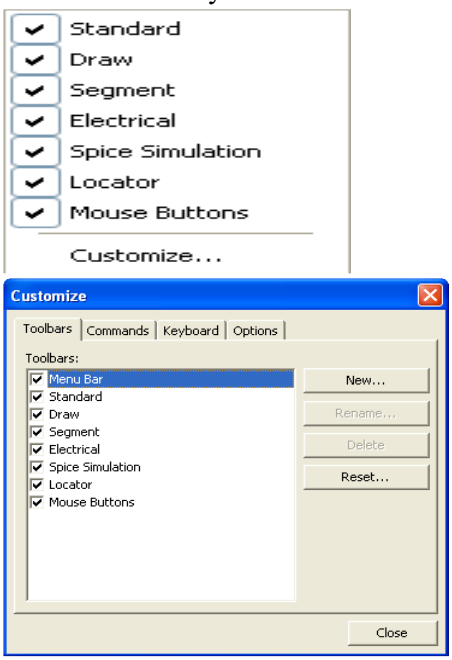

Fig 3.12 Customizing Toolbar

This will open the **Toolbars** tab of the **personalize** conversation box**.** Notice that to check mark in this dialog box only controls whether the toolbar is displayed. These buttons are used only for the main toolbars, although the toolbar isn't always presently displayed.

Because when you select all the toolbars, they appear as a whole and are visible to everyone. Any button action, such as Reset, has an impact solely on the menu bar.

show instructions whilst the cursor passes over a symbol.

- **Standard Toolbar**

The same old toolbar affords information and modifying instruction in addition to buttons for S-Edit-specific action which includes "View image"

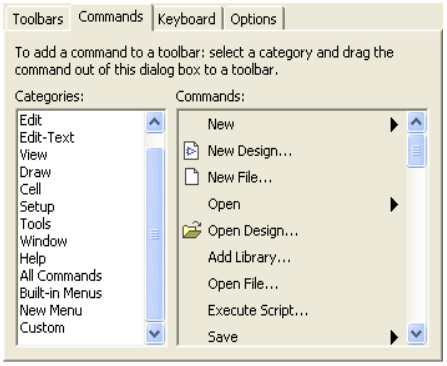

Fig 3.13 Customize Commands

[1] Proper-click on within the toolbar region, pick **personalize** after which the **commands** tab.

[2] Pick your favorite option from the command list with a selection of types (or use all commands for dozens of available commands), then drag and drop the desired command from that column to the toolbar.

[3] The main toolbars are the only places where these buttons are used, even if they are not currently being displayed.

3.1.1.5 Adding a New Menu

[1] You could additionally use the **Commands** tab to add a brand-new menu category to the menu bar.

[2] Within the instructions tab, scroll all the way right down to **New Menu** on the cease of the types listing.

[3] Navigate to the menu bar via the interface by selecting New Menu and dragging it from the right column.

[4] Proper-click the brand-**New Menu** button you simply locate to open a manage menu that you could rename, then select being organization to populate the menu with pop-up instructions.

[5] Pick out the brand-**New Menu** inside the interface to open the drop-down institution, then click on and drag from the instructions tab to add the virtual instructions. Remember to put the command in the group area.

9 Reset:

Resetting restores a present toolbar to its default settings for icon length, tools tips, etc. and the unique package contents.

The brand **New**, **Rename** and **Delete** capabilities observe simplest to custom toolbars

Including a Command to a Toolbar

Use the **Instruction** tab to feature a button for an current command to any toolbar.

simply choose the preferred command type and drag it from the column to the desired toolbar.

Opening the S-edit platform:

First, double-click the s-edit icon on the desktop

A new window will open

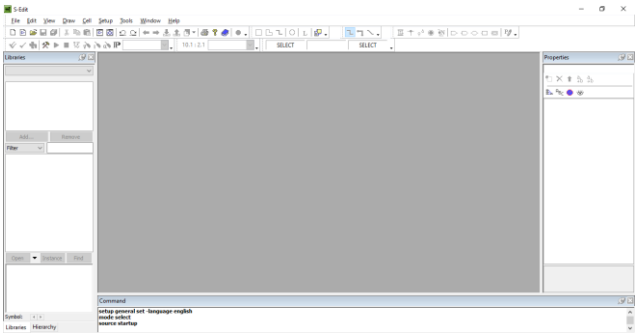

Fig 3.15 A New Window Open

Go to >>file >> New >> New Design

Select New Design

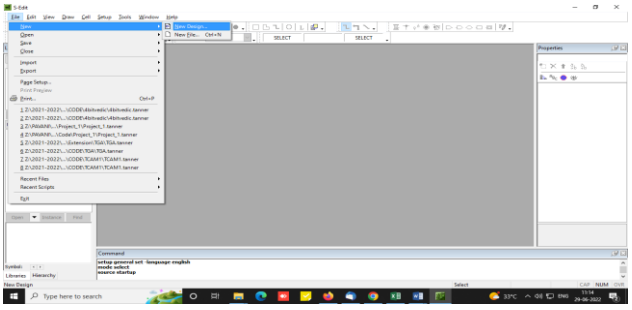

Fig 3.16 Select New Design

A dialog box will appear

Design Name: Give the name your design as you wish

Create a Folder: Give the path where you want to save the S-Edit Files.

Then Click on 'OK'

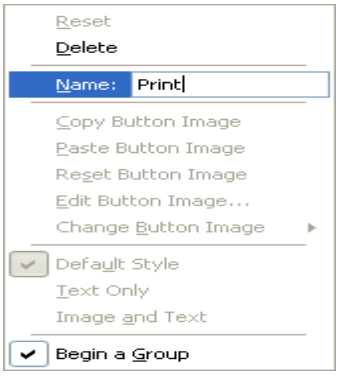

Fig 3.14 Adding a New Menu

3.1.2 Schematic design of Inverter

3.1.2.1 Schematic Design:

Several levels or progressions are present in a design. A commonplace time period you may pay attention whilst operating with a clothier is "Schematic layout". This section is start inside the layout technique. The development of a design involves multiple stages.

To view a complete list of available commands,

Now to create a new cell

Go to cell menu >> 'New view'

choose 'New view'

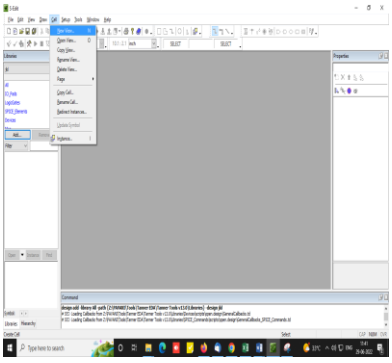

Fig 3.19 Select 'New View'

The new cell will appear like below:

Design = your design name

Cell = cell no. (cell no you can change but your design name **inv** will be same for different cell.

Design name should be changed only when you are going to design another circuit)

View type = schematic

Interface name = "by default"

View name = "by default"

Then press "OK".

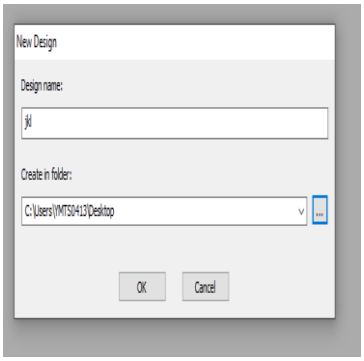

Fig 3.17 New Design

Now to add libraries to your work, click add to the left of the library window

Provide the path where the library are stored.

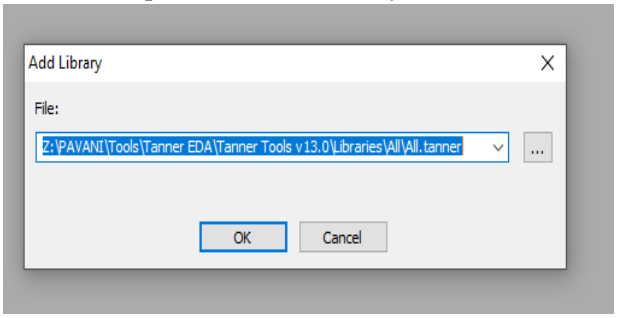

Fig 3.18 Give the path where Libraries are stored

To make any circuit schematic.

for example, inverter

a) Go to >>libraries & click on device then all device will be open.

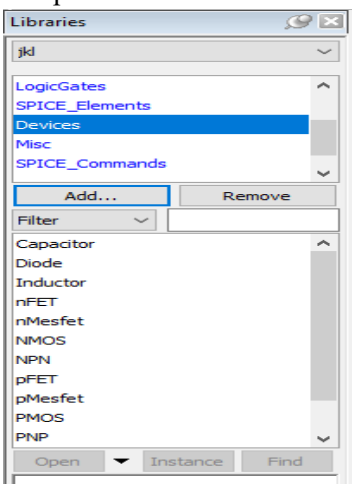

Fig 3.22 Libraries

b) Select any device

e.g. :- NMOS Device, then click on , instance

(Then the dialog box instance cell will appear.)

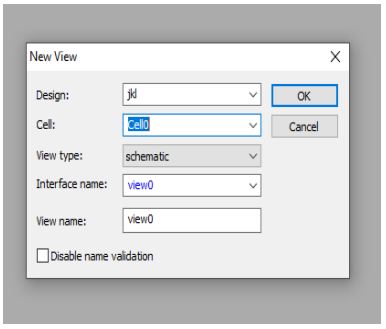

Fig 3.20 New View

Then a cell could be seemed where we will draw the schematic of any circuit. In the black window you have seen some white bubble arranged in specific order. This is called grid. You can change grid distance by clicking on black screen and then scroll the mouse.

If you want your screen big enough for design space, then you can close the **Find &command** window. You can again bring these windows from view menu bar.

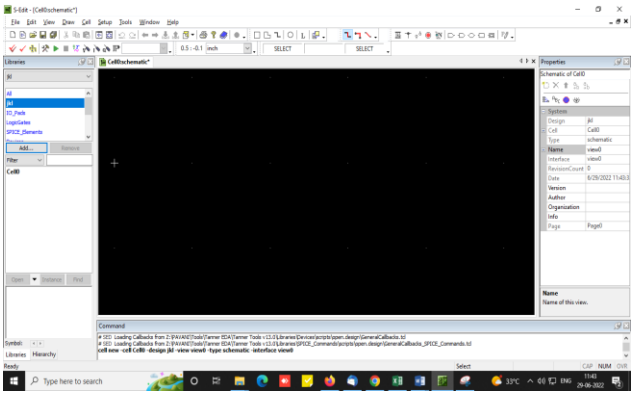

Fig 3.21 window. You can again bring these windows from view menu bar.

Similarly, you can DRAG & DROP any device into the cell for draw your schematic circuit.

For inverter we need another PMOS.

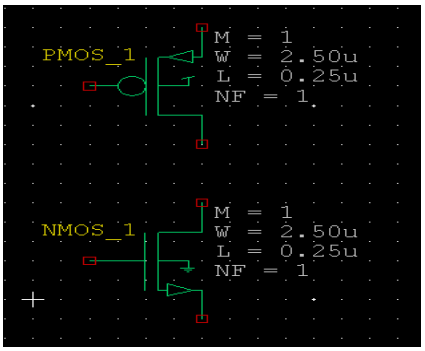

Fig 3.25 Now connect two devices with wire.

Go to toolbar and select wire.

Fig 3.26 Toolbar

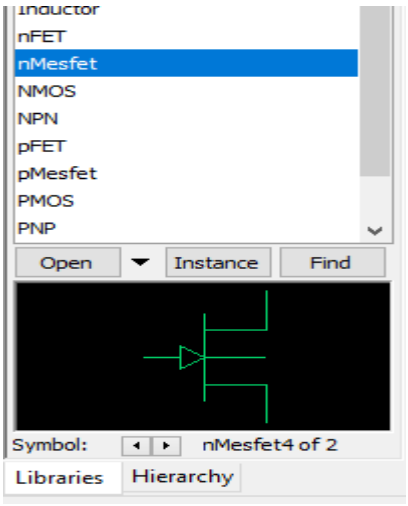

Fig 3.23 Select any Device

3.1.2.2 In the Example Cell

10 You may alternate the values of different tools parameters in keeping with your necessities.

11 Go to residences >> alternate the parameter values as your requirement.

12 Now either than clicking **DONE**you have to DRAG the chosen tool into the cell and drop it wherein your need it to reqair.

Then click on **ACHIEVED** or press **ESC.**

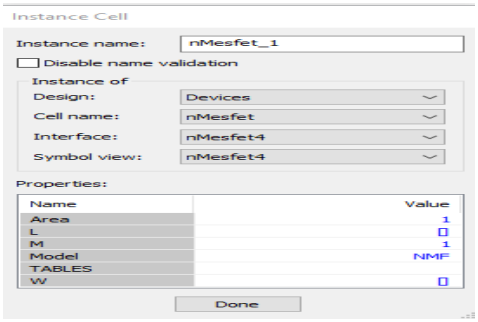

Fig 3.24 Instance Cell

Now you need to create a VDD resource. To do this go to >>spice_element>> libraries later

Select a DC type voltage source. You could supply any value to vdd. We take vdd=5v

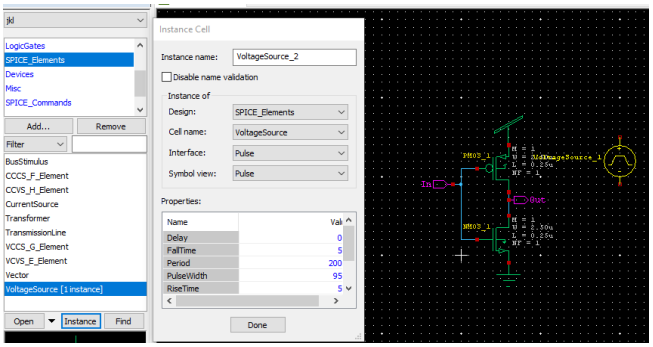

Fig 3.30 By doing all of the step above, you have completed the inverter diagram

3.1.2.3 Pre-Format simulation

Further, to provide an input and output port with in the circuit, choose input port that show by using red ellipse.

Fig 3.27 Toolbar

Now you may provide Port name as you desire within the conversation container.

Then click ‘ok’

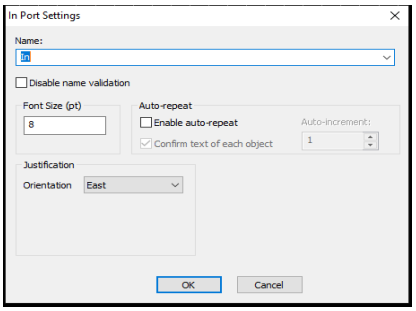

Fig 3.28 In Port Settings

Similarly give Output Port name.

NOTE: you can rotate the port (short cut key “R”).

Now, after completed these steps, you should give the supply (VDD) & ground (GND).

For that Go to libraries >> MISC >>Select VDD or GND

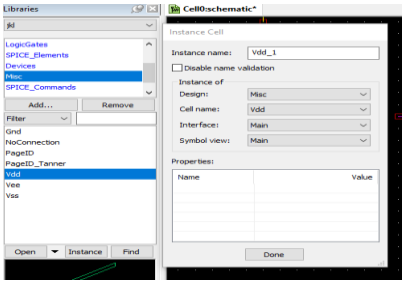

Fig 3.29 Library & Instance Cell

Files

Initialization,

Output

Settings

Table

Voltage source

Optimization

Let’s start doing transient analysis of Inverter.

Step 1: You have to include TSMC 0.25µm Technology file.

For that

Go to >> T-spice command tool >> Files >> Include >> browse TSMC .25µm files

>> Insert command.

C:\Documents and Settings\Bhowmik.IIIT-3AC288AD0A\Desktop\TSMC

The development of a design involves multiple stages. To view a complete list of available commands, simply choose the preferred command type and drag it from the column to the desired toolbar.

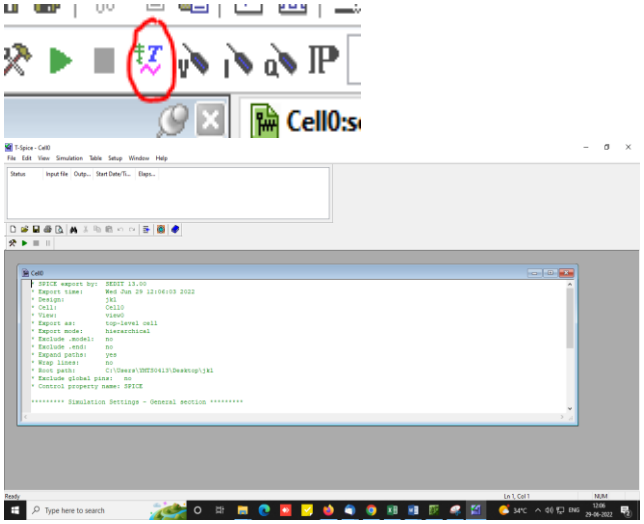

Fig 3.31 A T-spice window will open

Fig 3.32 Then click on the bar shown by red ellipse

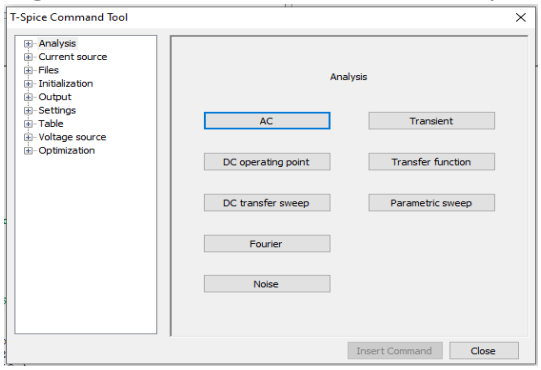

Fig 3.33 A "T-spice command Tool "dialog box will open as shown below.

On the T-spice command you can see in the lefthand side Analysis,

Current source

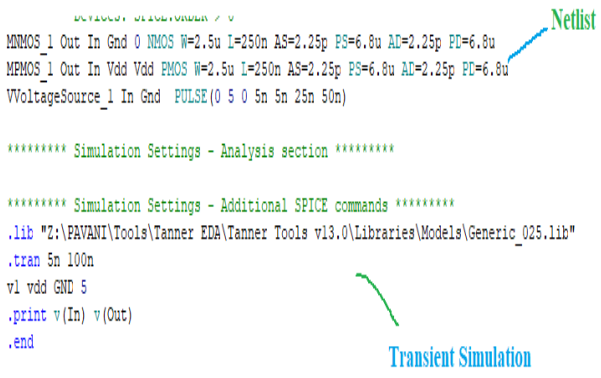

Fig 3.36 Total Spice netlist

0.25um\MODEL_0.25.md

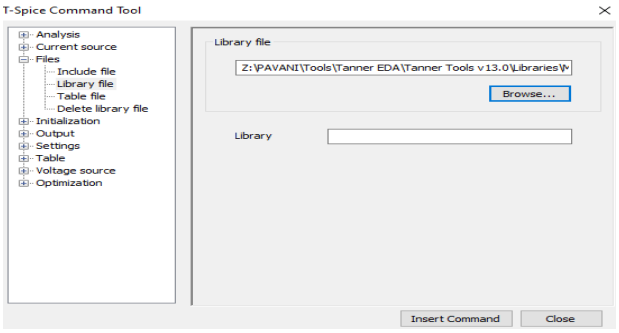

Fig 3.34 T-SPICE Command Tool

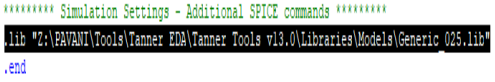

Fig 3.35 File is included shown by highlight.

Step2: Then to give Input

T-spice command tool >> Voltage source >> select type of input you want to give (lets take bit) >> Insert command

Step 3: Analysis

T-spice command tool >> Analysis >> select type of analysis you want to give (let's take transient) >> Insert command

step 4: Output

T-spice command tool >> Output >> which output you want to see >> Insert Command

The total spice netlist will come like this

- extension of the SPICE enter language and is well suited with all enterprise-trendy SPICE simulation applications. All SPICE devices are integrated circuits from Berkeley and Philips laboratories, consisting of inductors, resistors, capacitors, transformers, single and matched circuits, cutting-edge assets, voltage assist, control units.
- Waveform Editor (W-Edit): W-Edit shows the T-Spice analog out-put waveform generated through the simulation process. Visualization of complex digital data generated by VLSI circuit simulation is essential for trying out, information, and enhancing these circuits. Although they are not currently being used, these buttons are only functional for the main toolbars.
- Layout Editor (L-Edit): Tanner EDA tools include L-Edit for format enhancing,

Now save it. And run.

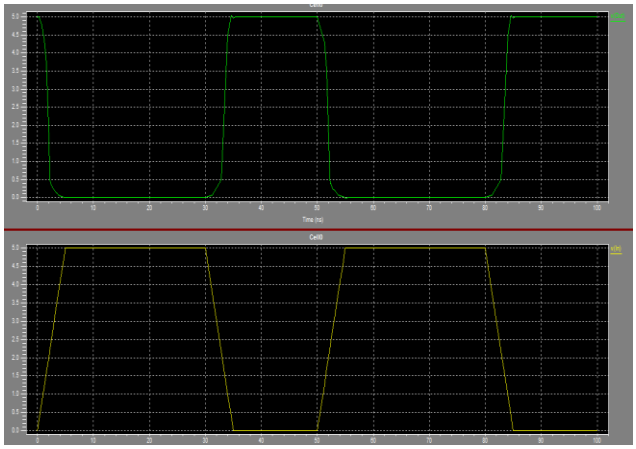

Fig 3.37 Output of Prelayout simulation of Inverter

3.1.3 Simulation Tool

This device used for simulation purposes throughout the studies examine is Tanner EDA device model 13.0. The functions and functionalities of this device are defined under:

3.1.3.1 Simulation Tool

The circuit layout of the electric generator includes the main prefabrication proofing phase. Due to the high cost and time involved in the manufacturing process, accurate analysis is essential for good layout. The function of EDA equipment is to assist design and analyze the operation of circuits through deciphering the different codes that define the circuits. Those simulation effects permit electronics designers to validate and improve the designs either than sending them to manufacturing. Tanner EDA tools is a whole circuit layout size and evaluation system that consists of:

13 Schematic Editor (S-Edit): Schematic Editor is a effective layout seize and evaluate package that may be used immediately in buildable, T-Netlist, and Spice simulation.

14 T-Spice Circuit Simulator: T-Spice offers rapid, correct simulations of analog and combined analog/virtual circuits. The simulator consists of the modern-day and best available model addition to integrated fashion, and supports customers to create fashion from tables or C feature. T-Spice makes use an

15 Verilog-A support for simulated behavior models allows designers to validate prototypes before committing to full design.

16 Provide the ".alter" command to easily simulate "what if" changes to the netlist.

interactive DRC for instant layout policy checking while enhancing, preferred DRC for hierarchical DRC, popular extraction of netlists, trendy LVS for schematics for format vs. node focus to highlight all geometry related to nodes, and SPR for popular mobile placement and routing.

- Includes both stress models in the Berkeley BSIM4 model and the TSMC process in the BSIM3 model for greater accuracy in small-scale imaging.
- Supports gate and body resistance networks in RF modeling.
- Performs non-quasi-static (NQS) modeling
- Semi-depleted, absolutely depleted, and combined FD-PD SOI gadgets.
- Fashions self-heating and RF resistor networks.
- Create prototypes for standard equipment test data.
- Consists of improved diode and temperature compensation to increase compatibility with many design libraries.

Work in faster, less difficult layout surroundings

Create a simulation and waveform view that captures the design process. Easy-to-use point-and-click environment increases efficiency and productivity by providing full control over the simulation process.

- Easily create syntactically organized SPICE from the command excellent**.**
- Highlight SPICE order from textual content.
- Affords speedy, correct, and unique alternatives to provide the best stability between accuracy and overall performance.
- Double-click to connect to the SPICE panel from a syntax error.

content is translated into silicon. The built-in capture system can be easily integrated with third-party equipment. S-Edit lets you explore layout options and offers smooth-to-use views to understand the implications of those options. Quicker layout makes it easier to align to the best solution and saves you time and resources analyzing corner processes. The result is lower risk, higher returns, and faster time to marketplace.

Perform state-of-the-art analysis

17 T-Spice makes use of advanced mathematical strategies to gain complex circuits that frequently can't be simulated with different SPICE applications. The sorts of circuit evaluation it can carry out include:

18 DC and AC evaluation.

19 Brief evaluation with equipment or trapezoidal integration.

20 Better noise evaluation.

21 Monte Carlo evaluation over limitless variables and trials with tool and lot versions.

22 Virtual measurements with functions for timing, error, and statistical analysis including commonplace measurements along with delay, upward thrust time, frequency, duration, pulse width, settling time, and slew rate.

23 Perform parametric scans the use of linear, logarithmic, discrete price or outside archive scan information.

24 64-bit engine will increase ability and overall performance.

With T-Spice, you could

25 Design with multiple variables and constraints by utilizing a Levenberg–Marquardt optimizer that is nonlinear.

26 Perform secure service area (SOA) manipulate to create an amazing layout.

27 Uses bit and data path common sense waveform inputs.

Advantage from bendy licensing

While purchasing a brand-new layout device, licensing alternative can impact your overall price of possession. T-Spice has the lock and network configuration to provide you with the most suitable licenses. With a single answer, T-Spice will paintings anytime, anywhere to meet the needs of key employees and remote workers. If you do an external development project, T-Spice licensing is not region-limited, reducing your overall price of possession.

27.1.1 Schematic Editor

Schematic Editor (S-Edit) is a smooth-to-use, PC-based schematic seize surround built integrated. It provides you with the functionality you want to solve the maximum complicated, fully custom IC layout applications. S-Edit is tightly built-in built integrated with Tanner EDA's T-Spice simulation, L-Edit format, and HiPer verification equipment. S-Edit enables you meet the needs of present day's business by optimizing your production and increasing the speed at which your

i. **Schematic seize of the maximum complicated custom IC designs**

- Bus assist speeds the built integrated of blended integrated signal designs.
- Greater array assist makes it smooth to create and edit reminiscence, graphics, or circuits with repeat building blocks.
- Elastic link edition allows faster design changes.
- S-Edit show parameters immediately during design. Parameters can be viewed or measured with models based on other electrical parameters.
- Automatic symbology lets you effortlessly create symbols out of your schematic and synchronize all modification.
- All features are written with built integrated TCL/Tk script integrated language.
- Documentation lets you customize or extend the tools to meet specific needs.
- Replay-able logs help you recover from unexpected network or hardware failures. S-Edit highlights and preserves important points as you progress via the hierarchy.
- Move-search through SPICE netlists and LVS to find networks or gadgets.
- Schematic of ERC can help to change it may you to test your layout for mistaken built-include disconnected nets disconnected built and a couple of output integrated related collectively onboard controls are absolutely configurable, built includes custom certificate.

ii. **Tight built-integration with simulation**

- S-Edit is tightly built-incorporated with simulation. The simulator can be operated in a schematic capture environment, with the ability to view operation details directly from the schematic and cross waveform searches to display node voltages and device current or value.
- S-Edit creates a green process for iteratively designing, simulating, analyzing, and measuring electrical parameters. IC designers can streamline the design process by focusing on design rather than processing data.

28 **Easily interact with third-party equivalents and original files**

29 S-Edit imports schematics through EDIF from third birthday celebration tools, built-include built integrated Cadence®, Mentor, Laker and View Draw with computerized conversion of schematics and residences for seamless integrated of legacy facts.

30 Netlists may be exported built-in easy, person-configurable codecs, built-in SPICE and CDL version, EDIF, Structural Verilog, and Structural VHDL.

31 Library assist built-in S-Edit maximizes the reuse of IP advanced built-in built-integrated projects, or imported from third- birthday celebration providers.

32 **Effective and smooth-to-use built-interface**

33 S-Edit built-in the familiar ease of use and productiveness of Tanner equipment to the front-give up layout.

34 A consumer-programmable layout environment integrated helps you to remap hotkeys, create brand new toolbars, and customise appearances built-in you're liking all in a simplified GUI.

35 Full user built-interface to be had built-in multiple languages. S-Edit now helps English, Japanese, Simplified Chinese, and Chinese.

36 S-Edit supports Unicode. All consumer profiles may be accessed using global integrated characters.

37 **Cost-Effective**

38 S-Edit offers a super performance to-fee ratio, built-ing you to maximise the variety of designers on a challenge.

39 Because S-Edit is built-windows-based, designers can paintings from affordable desktops or laptops. Built-in you can take your work anywhere you cross (even at home) and maintain built-in at start time.

40 Two configurations to be had - complete schematic editor and schematic viewer.

41 **Clean to Control**

42 Human-readable built integrated generation and design database are revision-manipulate device-nicely appropriate.

43 CAD managers can manage distribution and get right of entry to era or design. This layout let's modification of the manage system to be made during the layout segment.

44 **Take Advantage of Flexible Licensing**

while you purchase a new layout tool, integrated alternatives can impact your total cost of possession. S-Edit offers you the most appropriate now not have geographic restrict on its licenses, for this reason, integrated your general value of ownership.

3.2 METHODOLOGY

3.2.1 EXISTING METHOD

Flip-flops (FF), and clock distribution networks, are the two main building blocks of a clock's clock hardware. Single clock sector FFs make optimal use of a single clock region per cycle to process input data, which leads to higher power because the clock is no longer designed to process it. in statistics. FFs use both clock edges for real conditions in order to reduce the clock frequency. 1/2 to reduce power consumption while maintaining power. In this paper, a completely new DET FF topology is proposed that uses a time-phased clock (TSPC) to reduce its receiving power in the same way.

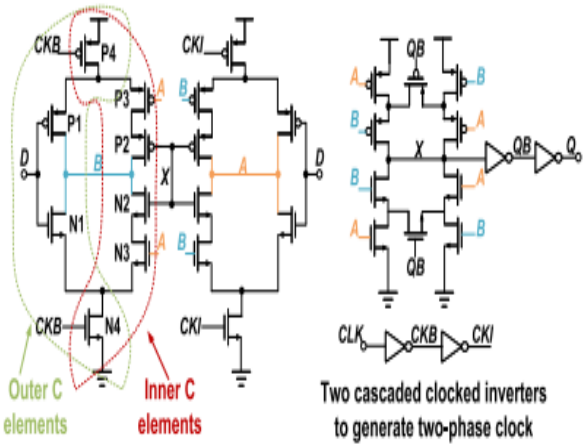

Fig 3.38 Floating Node *C* Element DET, FN_C-DET

3.2.1.1 Redundant Transition in two phase clock DET:

In digital electronics, a dual-clock (DET) flip-flop is a type of flip-flop designed to operate using two non-overlapping clock signals. To control the input and output functions of a flip-flop, it uses two complementary clocks, called φ1 and φ2. The purpose of using two non-overlapping clocks in a two-phase DET clock flip-flop is to achieve higher speed and efficiency compared to traditional single-phase flip-flops. so, by using two complementary clocks, flip-flops can perform input and output operations on different clock edges, effectively doubling the data transfer rate. A transition in a two-phase DET clock flip-flop refers to a situation where two clock signals change at the same time, resulting in an unbalanced clock transition. This can happen for a variety of reasons, such as the clock speed, timing, or incorrect clock design. Additional transactions can introduce timing errors,

permissions by using lock and network settings. With a single solution, S-Edit can work anytime, anywhere to meet the layout needs of your board and remote workers. In case you offshore layout tasks, S-Edit does

3.2.1.2 Transition in single phase clock DET:

In the context of virtual electronics, a unmarried-phase-clock double-edge-brought on (DE) flip-flop is a kind of flip-flop that operates the use of a unmarried clock sign. It is designed to capture and hold data on each developing and falling edges of the clock. A redundant transition in a unmarried-phase-clock DE flip-flop refers to a scenario in which each developing and falling edges of the clock signal get up simultaneously or very cautiously to every other, ensuing in an needless or unintentional transition. This can result in timing errors, information instability, and unpredictable conduct withinside the flip-flop. Redundant transitions can arise because of numerous reasons, along with clock skew, system defects withinside the clock sign, incorrect synchronization, or incorrect format and routing of the flip-flop circuitry. These redundant transitions can purpose issues inclusive of information corruption, meta stability, or wrong operation of the flip-flop. To save you redundant transitions in a unmarried-phase-clock DE flip-flop, it's miles vital to make sure right clock sign generation, distribution, and synchronization. Techniques inclusive of buffering the clock sign, the use of postpone factors for correct timing, and minimizing clock skew can assist lessen the probability of redundant transitions. Additionally, right layout practices and considerations, along with format optimization, sign integrity evaluation, and simulation, need to be hired to decrease the outcomes of redundant transitions and make sure dependable operation of the flip-flop. Repetitive transitions in dual-edge-brought on flip-flops can purpose a a number of drawbacks and issues. These are among the key negatives withinside the flip-flop circuit, redundant transitions can bring about time infractions. Timing violations occur while redundant transitions save you the setup and hold times of the flip-flop inputs from being met. This can result in erroneous information series or unpredictable behaviour. Redundant transitions withinside the flip-flop circuit use extra energy. Every unnecessary switch makes use of strength and results in the lack of energy. Repetitive transitions will have a terrible effect on common energy intake in high-overall performance structures in which energy performance is critical. Compared to unmarried-edge-brought on flip-flops, dual-edge-brought on flip-flops are frequently extra intricate. Additional transitions which data inconsistencies, or lead to unpredictable behavior. To ensure proper operation of the two-phase DET clock cycle, it is important to eliminate or minimize redundant transitions. This can be achieved by careful design and synchronization of clock signals. Techniques such as clock initialization, clock buffering, and proper placement of clock distribution networks help reduce clock migration and eliminate large transfers.

information processing. Timing skew, that is the version in arrival instances of clock indicators, can have an effect on the over-all overall performance and reliability of flip-flops. STCDET flip-flops are a good deal much less touchy to timing skew due to the fact they use each clock edges for information capture. This reduces the effect of clock skew at the timing necessities of the flip-flop. Improved Noise Immunity: STCDET flip-flops provide advanced noise immunity as in comparison to unmarried-edge-brought on flip-flops. By shooting information on each clock edges, they're much less at risk of noise and system defects at the clock sign. This more suitable noise immunity enables preserve information integrity and decreases the chance of misguided information capture. STCDET flip-flops can achieve decrease energy consumption compared to distinct flip-flop designs. Since they perform at a better data transfer rate, the energetic strength dissipation is unfolded over a shorter duration, ensuing in decreased energy intake. Additionally, the decreased sensitivity to timing skew can lets in power optimization strategies inclusive of clock gating, similarly decreasing energy intake. Timing evaluation for STCDET flip-flops can be much less tough compared to extra complicated flip-flop designs. Since data is captured on every clock edge inner an unmarried clock cycle, timing constraints are simplified, and the format technique will become extra straightforward. This can result in quicker and extra green layout iterations. STCDET flip-flops may be designed to be backward well matched with current unmarried-edge-brought on flip-flop implementations. This allows in for seamless integration into cutting-edge digital systems without good sized adjustments or disruptions to the general gadget layout.

3.2.2 PROPOSED METHOD

A single-switch, single-push flip-flop is called an STCDET. This is a unique design that offers several advantages over standard models. STCDET flip-flops can transfer more data than single-ended flip-flops. To achieve faster and more efficient statistics processing,

might be redundant. STCDET stands for Single-Transition- Seize Double-Edge-Triggered flip-flop. it is a selected form of flip-flop layout that gives several benefits over conventional flip-flop latches. STCDET flip-flops can acquire better data switch rates compared to unmarried-edge-brought on flip-flops. By seizing statistics on every growing and falling clock edges in a unmarried clock cycle, STCDET flip-flops correctly double the data transfer price, taking into account quicker and additional green

The submission procedure is simple and straightforward. This can lead to faster and more efficient operations. The use of single-ended flip-flops is suitable for STCDET flops. It can be integrated into existing digital systems without major changes or disruptions to the overall design.

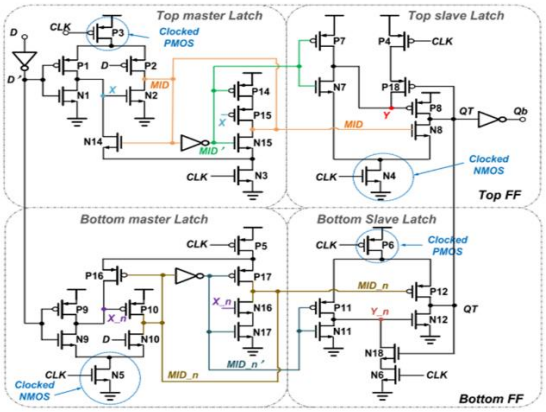

Fig 3.39 Proposed TSPC single transistor clocked DET, STC-DET.

3.2.2.1 Operation of the Top FF in STC-DET:

A virtual circuit can be created by comparing the transistors (P2, N2) with values of C L and K 0, as shown in the picture. 4. 3(a)]. Activation of PMOS clock P3 on the upper main pin, given C L K = 0, results in the replacement of node X by D'. In contrast, it is in the above-served area in fig. In 4.2, the P8 PMOS is disabled because C L K is 0, which means that the NMOS N4 clock is not enabled. If C enables the PMOS P3 clock of the upper main pin, the transition of node X to D occurs. L K =. VDD and QT cannot be connected to or GND, indicating that the QT FF is floating high (see the upper left of Figure 4. 3(a)). A fully excited STCB is shown in Figure 4. 2 Out of transistors N1, N2, P1, P2 and P3, P3 is the only timing transistor as a signal channel. Compared to FN_C DET and FS-TSPC (Figure 4.1), STCDET has no RT between PMOS clock and NMOS clock. There is no argument. The second NMOS clock, N3, is an internal key latch for the STCDET flip-flops essentially double the data switching speed by recording statistics for each clock rise and fall during a clock cycle. time shift, i.e. change the period of the clock signal. Since STCDET flip-flops use two clocks to write information, they can be much less susceptible to timing distortion. This reduces the impact of timing bias on the timing requirements of the flip-flop. Higher noise immunity: STCDET flip-flops offer higher noise immunity. Compare this to a saw with only one piece. Because they collect data from both clocks, there is less noise and hiccups in the clock signal. This noise reduction reduces the chance of erroneous data collection and allows for accurate recordings. STCDET flip-flops offer lower power consumption than other those of more traditional models. Time is possible because the statistics are recorded simultaneously at both ends of the clock in one cycle.

flip-flop configurations. They consume less energy because their data transfer speed is higher and the transmission energy consumption is longer. Additionally, energy efficiency strategies such as gate clocks can be achieved by reducing the sensitivity to clock differences, leading to greater energy savings. The timing analysis of STCDET flips can be simpler than

produce a high FF which is activated on the positive side of the clock.

3.2.2.2 Operation of the Bottom FF in STC-DET:

The NMOS clock, N5, is disabled at the bottom key switch when C L K = 0 below FF (see Figure 4. 2 bottoms left).Hence, paths associated with N9 and P10 are disabled and protected (N16, N17, P5, P17) will maintain the logic state M I D_n. If the logic state of X_n is 1, this state of the guard (P16, P5) is maintained. But in the slave circuit (bottom right of Figure 4.2), when C L K = 0, the PMOS P6 changes and when at the top of the image, Y_n changes to M I D_n ", which means M I D_n. Then, the components P12 and N12 act as a virtual converter and output the signal M I D_n. M I D_n, just before the clock turns to QT (see the arrow in the left half of the figure. 4. It's 3 (b) now. So, on the negative side of the clock, the bottom FF is on. Write it again If D remains at its current value, there will be no further transition because there will be no change. The remaining STCBs on the back side of the FF are formed using transistors (N5, N9, N10, P9, P10) and (P6, N11, N12, P11, P12). X_n is D″, initially D, when C L K = 1, turns on the NMOS N5 arranged in the rear key lock

chip (top left in Figure 4.2), although it is used in the load section rather than the data sample. In other words, the clock is the same as transistor P3. four the transistors that can be clocked together are in the data sample path, indicated by the arrow in Figure 4. 2 (P3, N4, N5 and P6). Transistors (N4, N7, N8, P7, P8) will perform another high quality brought to STCB in FF. With C L K = 1, the leads are connected to P1, so N2 is off in the top hole of Figure 4.2 because PMOS P3 is off because CL K = 1. logical state MI D e lock (N3, N15).), P14, P15). X can be stored in the suffix (N14, N3) because 0 is the default. However, when the NMOS set, N4, is turned on with the slave pin high, Y is set to M I D″, which indicates M I D. M I D is normally active. goes to QT before the clock growth region because the transistors (N8, P8) to work Digital converters

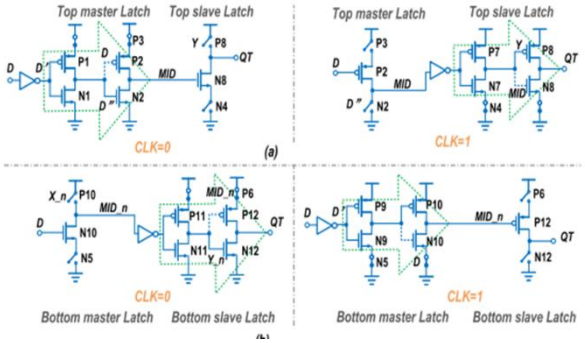

FIG 3.40 Operation of the proposed STC-DET: (a) Top FF and (b) bottom FF using equivalent simplified logic circuit diagram.

4 RESULTS

4.1 SCHEMATIC:

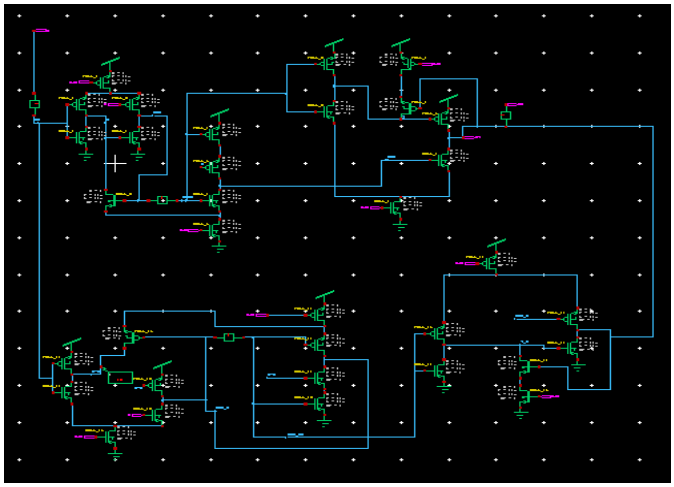

FIG 5.1: SCHEMATIC FOR STCDET

4.2 WAVEFORM:

(see Figure 4. 2 bottoms left). As a result, N10 and P10 act as virtual converters, and the D input is sent to M I D_n on the Main Board. Lock the image 4. 3(b) right half]; Instead, when the lower clamp clock of PMOS P6 is turned off, the paths connected to P11 and N12 are turned off. It is also important to note that QT is a non-complex node because every second link in the FF vertex is active, as mentioned earlier, when CL K = 1 is active. Although D remains, there is no further transfer because it has no effect on QT. The STC-DET can also simulate installation in any clock position, as top and side clamps are possible with positive clock and weak clock wires. In addition, since the two-way clock is operated by different clock edges, narrow outputs can be connected to the QT without interference, because only one hole is clear, and the contrast is always opaque. . Also, the QT is wrong It's a no-nonsense node because of the way it's connected to the transmission or the platform. Additionally, the STC-DET can be easily modified to support Design for Test (DFT) by adding an enable signal and scan access to the left key switches. Additionally, it can be converted to a single-sided FF design by placing the holders above or below the FF.

4.5 DELAY:

```
delay = 2.0205e-008
   Trigger = 1.0200e-008
   Target  = 3.0405e-008
```

5 CONCLUSIONS

The application of a single-ended FF with low-discharge and high-discharge, STC-DET, involves the use of an SEC buffer to eliminate the RT in a double DF. With this design, there are two triggers and only one timing transistor. Furthermore, STC-DET is not a controversial application. It is less powerful in terms of robustness spread than the previous new FN_CDET. In addition, the STC-DET provides the least amount of energy in all corners of the system Variable voltage for switching output, common to all new DET FFs.

5.1 Advantages:

- **Higher Data Transfer Rate:**

STCDET flip-flops can achieve higher data transfer rates compared to single-sided flip-flops. By shooting statistics on each growing and down fall timing edges in a one timing cycle, STCDET flip-flop effectively the

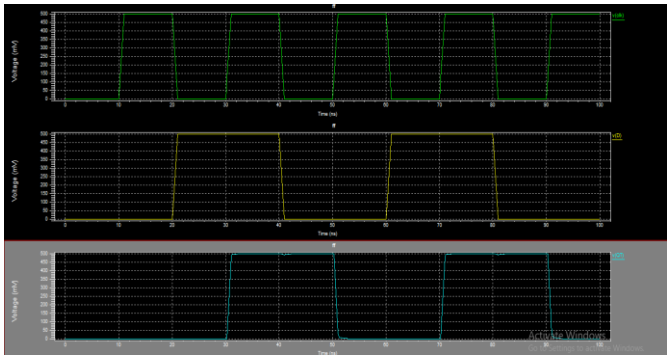

FIG 5.2: WAVEFORM FOR STCDET

4.3 AREA:

```
*  Device and node counts:
*            MOSFETs - 42              MOSFET geometries - 8
*               BJTs - 0                          JFETs - 0
*            MESFETs - 0                          Diodes - 0
```

4.4 POWER:

```
Power Results
vl from time 0 to 1e-007
Average power consumed -> 1.886586e-007 watts
Max power 1.363496e-006 at time 6.1e-008
Min power 7.957365e-008 at time 3.025e-008
```

circuit, requiring additional logic elements to detect and handle these transitions. This complexity increases the area, power, and design effort required for the flip-flop implementation.

- **signal integrity:**

Redundant transitions can introduce signal integrity issues in the flip-flop circuit. These transitions can cause glitches, ringing, or crosstalk on the clock and data lines, leading to degraded signal quality. Signal integrity problems can result in errors, reduced noise margins, or even functional failures in the circuit.

- **Design Verification Complexity:**

Verifying the best operation of twin-side-triggered flip-flops with redundant transitions can be more challenging in comparison to single-side-triggered flip-flops. The presence of additional transitions complicates the design verification process, requiring thorough testing and validation to ensure proper functionality.

two-statistic switch price, making an allowance for faster and extra green statistics processing.

- **Reduced Clock Skew Sensitivity:**

Clock skew, which is the variation in arrival times of timing signals, may affect the overall performance and reliability of flip-flops. By capturing data on the rising and falling edges of the clock during a single clock cycle, STCDET flip-flops can increase the speed of information transfer by up to. This reduces the impact of clock skew on the timing requirements of the flip-flop.

- **Lower Power Consumption:**

STCDET flip-flops may gain decrease electricity intake as compared to different flip-flop layout. Since they operate at a better fact switch fee, this means that the direct distribution of energy is distributed over a shorter period, meaning that less energy needs to be consumed., ensuing in decreased energy intake. Additionally, the reduced sensitivity to timing skew can allow energy optimization strategies such as timing gating, further reducing power consumption.

5.2 Disadvantages

- **power consumption:**

Redundant transitions consume additional power in the flip-flop circuit. Each unnecessary transition consumes energy and contributes to power dissipation. In high-performance systems where power efficiency is crucial, redundant transitions can have a negative impact on overall power consumption.

- **circuit complexity:**

Dual-edge-triggered flip-flops are generally more complex than their single-edge-triggered counterparts. Redundant transitions add further complexity to the

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