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Low-Power Transmission Gate-Based SRAM Architecture with Dynamic Power Gating for Sub-Threshold Applications

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Abstract: The growing demand for energy-efficient memory in sub-threshold computing environments, especially in IoT and embedded systems, necessitates the development of optimized SRAM architectures. Traditional 6T and 8T SRAM cells suffer from high leakage power, increased latency, and poor scalability. This work presents two novel design methodologies to address these limitations. The first incorporates Transmission Gate (TG) logic to improve read access stability and reduce delay. The second integrates a dynamic power gating scheme to minimize leakage power and enhance overall energy efficiency. The proposed designs are modeled and evaluated using the Tanner EDA tool with 45nm technology files. Simulation results demonstrate over 80% reduction in latency and significant power savings compared to conventional SRAM designs, highlighting the architecture's suitability for low-power, high-performance applications in modern SoC and IoT systems.

Keywords: Static Random Access Memory (SRAM), Transmission Gate Logic, Power Gating, Low-Power VLSI, Sub-Threshold Operation, IoT, Tanner EDA, 90nm Technology

I. INTRODUCTION

Static Random-Access Memory (SRAM) forms the dominant component of modern SoC architectures, occupying nearly 60–70% of the total die area. As technology scales towards deep-nano regimes, leakage power and read/write instability become major bottlenecks for SRAM operation under low-voltage and sub-threshold environments. Applications such as biomedical implants, portable sensors, wearables, and IoT devices require memory units with extremely low switching energy, compact area, and reliable operation at voltages as low as 0.3–0.5 V. Traditional 6T SRAM cells suffer from degraded Read Static Noise Margin (RSNM), reduced Write Ability (WA), and increased susceptibility to process variations at low supply voltages.

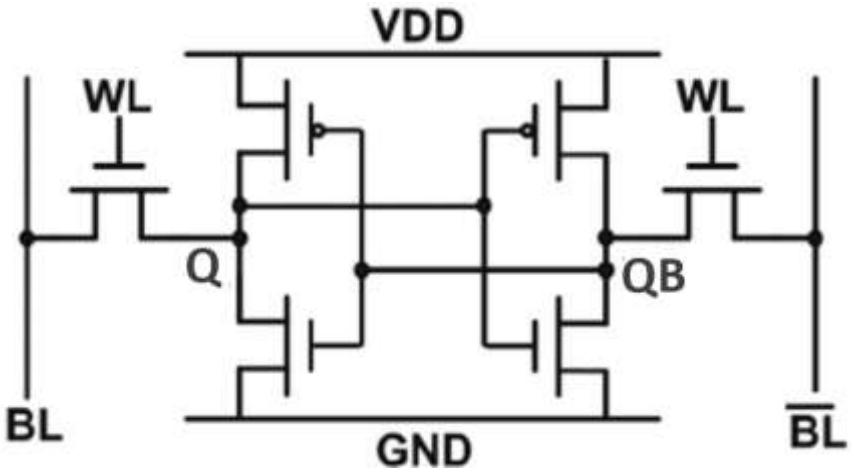

Fig. 1. 6T SRAM Cell

Meanwhile, 8T and 10T SRAM topologies provide improved noise margins but incur greater area and energy overheads. Transmission Gate (TG)-based techniques offer enhanced read-path isolation, while power-gating methods suppress leakage during inactive periods. This paper integrates both approaches to achieve highly efficient SRAM architectures for ultra-low-power systems.

II. BACKGROUND AND RELATED WORK

Extensive research has focused on enhancing SRAM performance in low-voltage conditions. Prior work includes:

- 6T SRAM designs using FinFET technology to enhance RSNM and reduce leakage [6].
- 8T and 10T cells for sub-threshold operation using isolated read paths [15], [17].
- Power gating with header/footer transistors to suppress standby leakage [20].
- TG-based SRAM architectures enabling improved read stability and bidirectional current flow [10] [11].

Despite these advancements, an architecture that jointly delivers **low area, low power, strong stability, and fast access times** remains an open challenge. This motivates the present TG-based and power-gated SRAM architectures.

III. PROPOSED DESIGN METHODOLOGY

A. Transmission Gate Based 8T SRAM Architecture

A Transmission Gate (TG) consists of parallel-connected NMOS and PMOS transistors, enabling full-swing conduction of both logic '0' and '1'. Integrating a TG into the read path of a standard 6T SRAM cell forms an enhanced 8T topology.

Advantages include:

- Bidirectional conduction
- Stronger read access
- Isolation of storage nodes
- Reduced read-disturb failures
- Lower propagation delay due to reduced resistance

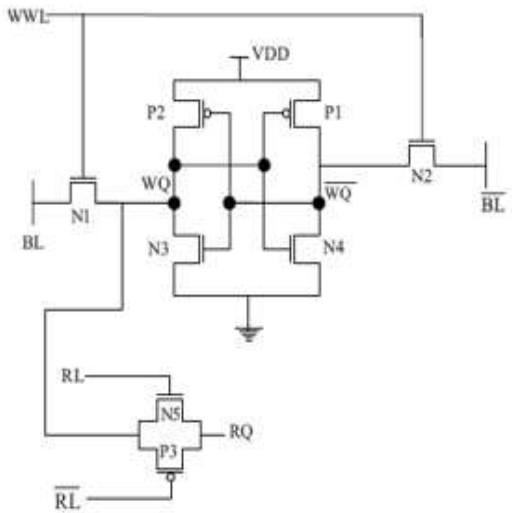

Fig. 2. Transmission Gate Based 8T SRAM

During read operation, the RL and R$\bar{L}$ signals activate the TG, transferring the stored value directly to the read node. This reduces read latency significantly.

B. Dynamic Power Gated TG SRAM Architecture

The second architecture integrates **header and footer power-gating transistors** controlled by complementary enable signals. When the cell is idle, the supply path is cut off, minimizing leakage.

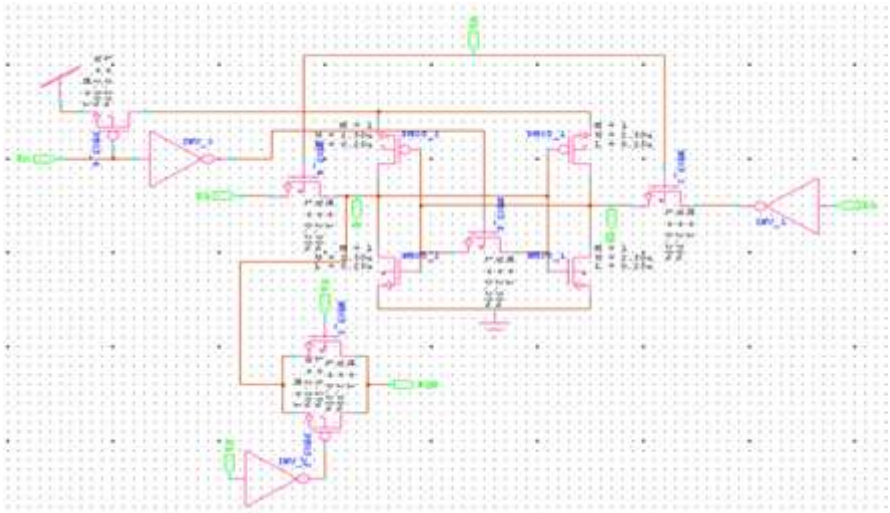

Fig. 3. Dynamic Power Gated TG SRAM Architecture

Key Features:

- Header PMOS gating between VDD and storage nodes
- Footer gating between ground and inverter stack
- Only one gating transistor active at any time
- TG-based read port maintains isolation and speed

During active mode:

- EN = 1 activates the header transistor
- SRAM performs normal read/write operations

During sleep mode:

- EN = 0 disconnects VDD or ground
- Leakage reduces drastically
- Stored data retained via cross-coupled inverters

C. Power and Delay Models

Dynamic power:

$$P_{dyn} = \alpha C V_{DD}^2 f$$

Leakage (static) power:

$$P_{static} = I_{leak} \times V_{DD}$$

Reduction in both dynamic and leakage power is achieved through TG isolation, reduced switching, and power gating.

IV. SIMULATION AND RESULTS

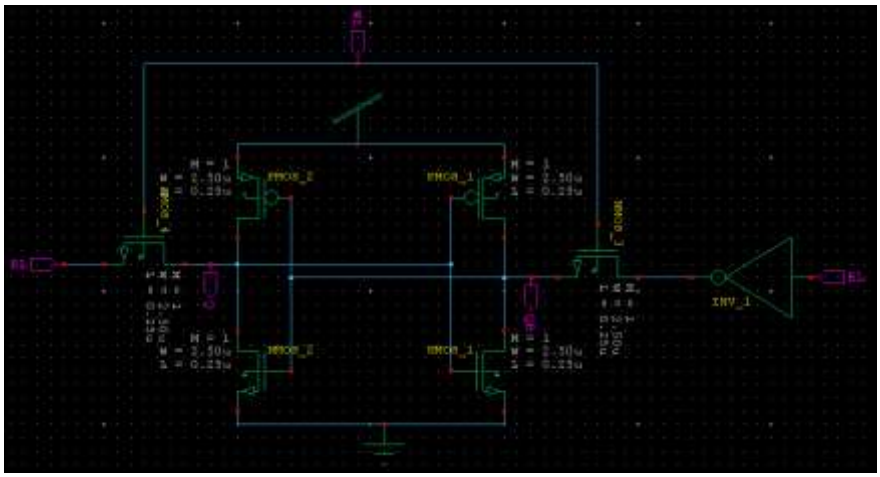

Fig. 4. Schematic Diagram of 6T SRAM cell

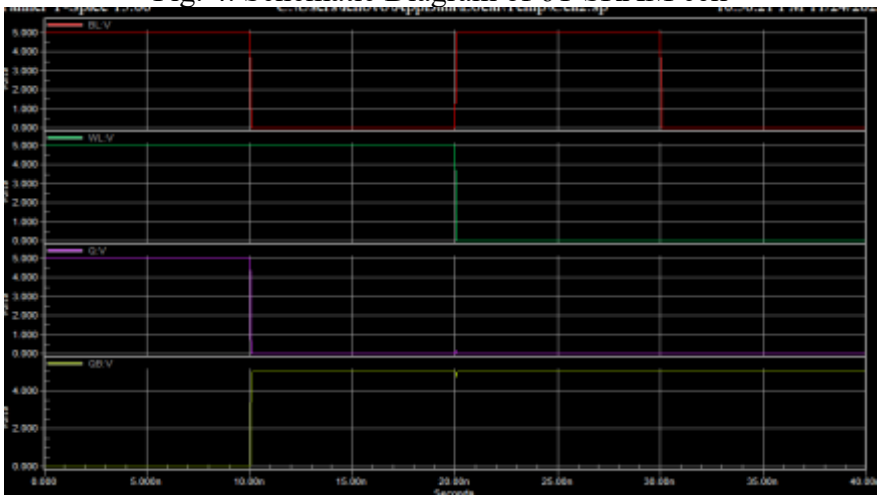

Fig. 5. Output Waveform of 6T SRAM cell

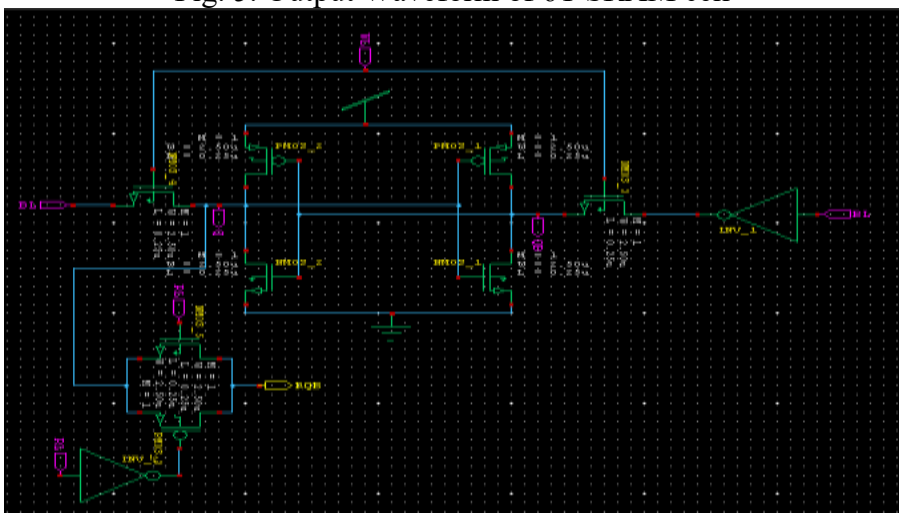

Fig. 6. Schematic Diagram of Transmission Gate Based 8T SRAM

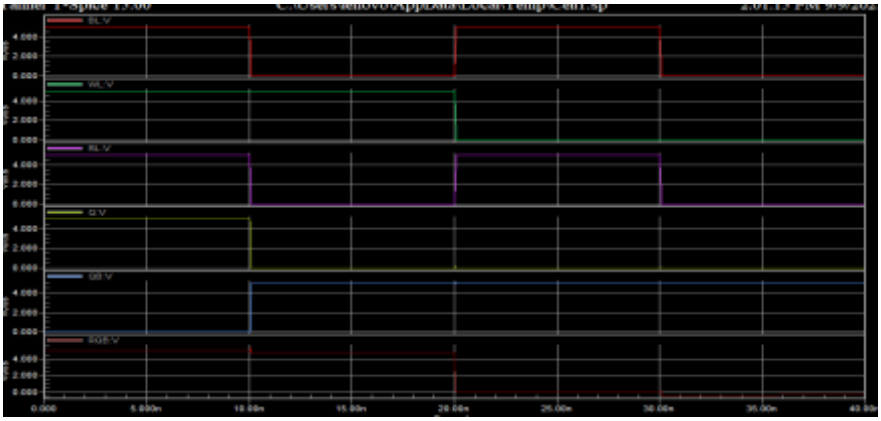

Fig. 6. Output Waveform of Transmission Gate Based 8T SRAM

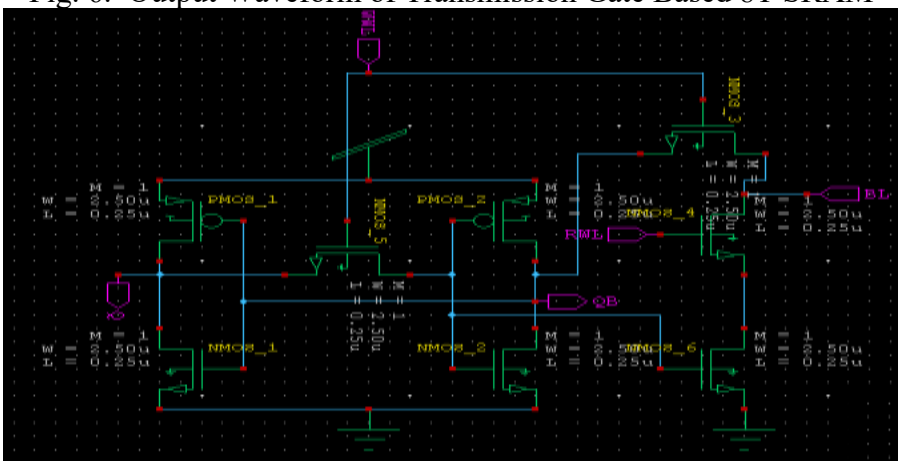

Fig. 7. Schematic Diagram of 8T SRAM

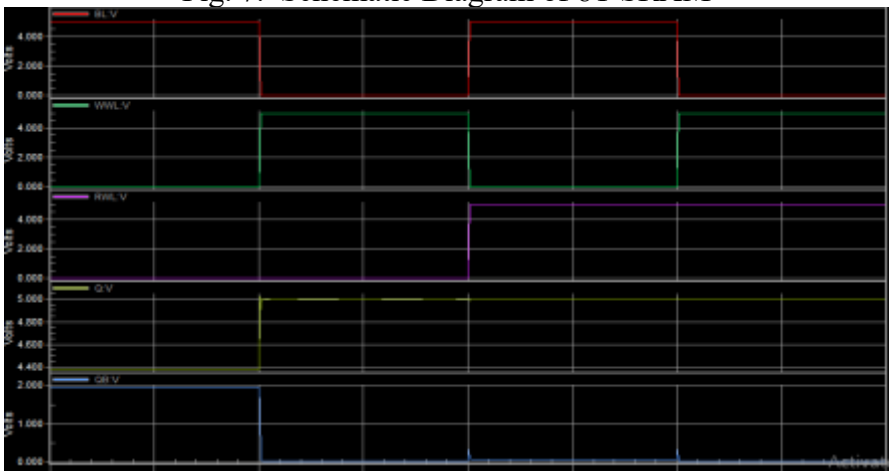

Fig. 8. Schematic Diagram of 8T SRAM

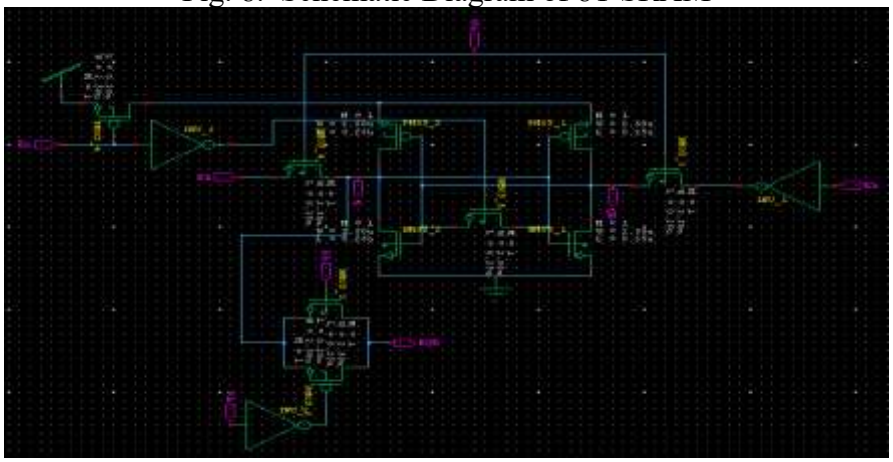

Fig. 9. Schematic Diagram of Dynamic Power Gated TG SRAM

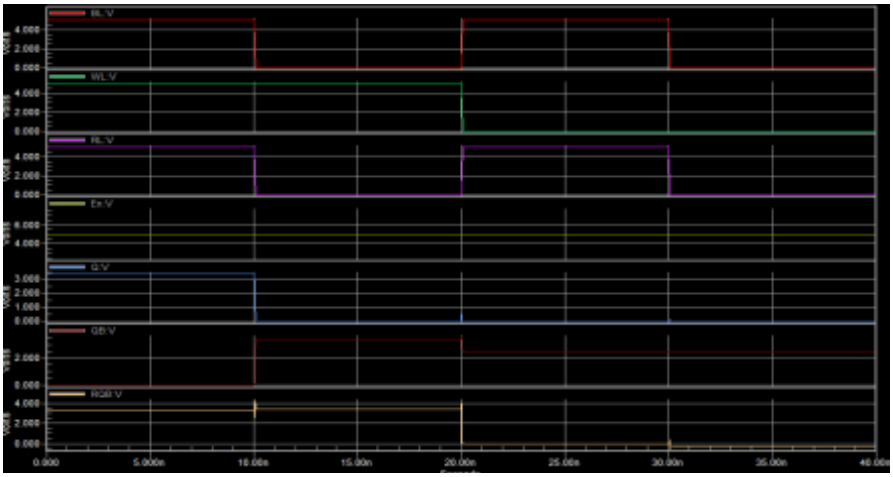

Fig. 10. Output Waveform of Dynamic Power Gated TG SRAM

Table. 1. Comparative Evaluation

Architecture	Transistor Count	Power	Latency
6T SRAM	6	6.75 µW	5.44 ns
TG-Based 8T SRAM	12	0.712 µW	2.415 ns
8T SRAM	8	0.895 µW	6.248 ns
Proposed Dynamic Power Gated SRAM	16	0.52 µW	0.15 ns

V. CONCLUSION

This work presents an optimized SRAM architecture combining TG-based read enhancement and a dynamic power-gating strategy. The proposed design achieves superior performance compared to conventional SRAM structures, with significant improvements in latency, power consumption, and read stability. These advantages make it suitable for applications requiring ultra-low-power memory such as IoT edge devices, biomedical implants, and high-efficiency wearable electronics.

Future Scope: SRAM can be further optimized using advanced device technologies such as CNTFETs, GNRFETs, FinFETs, or Floating-Gate MOSFETs, enabling additional improvements in area efficiency, threshold tunability, and leakage reduction.

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