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"Low-Power VLSI Design in Full Adder Using Body-Biasing Techniques"

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ABSTRACT

This paper presents five distinct low-power full adder designs based on XOR/XNOR gates and multiplexer blocks, enhanced through body biasing techniques. In the first approach, the adder achieves a power dissipation of 204.09 µW with a delay of 5.9849 ns. The second method shows improved power efficiency, reducing consumption to 128.92 µW and exhibiting a delay of 5.9875 ns, thanks to the use of voltage biasing on two PMOS transistors (P1 and P2) alongside substrate biasing. The third design significantly minimizes power dissipation to 0.223 nW, with a delay of 5.2352 ns. An even lower power consumption of 0.199 nW is observed in the fourth methodology, which operates with a delay of 5.1002 ns. Finally, the fifth design further reduces minimum power to 0.192 nW. Additionally, the power delay product (PDP) has been analyzed across all proposed methods. When compared to previously reported designs, the proposed adders demonstrate superior performance in both power efficiency and delay.

Keywords: *Body bias, exclusive-OR (XOR), exclusive-NOR (XNOR), full adder design and low power.*

1. INTRODUCTION

In recent years, reducing power consumption in CMOS circuits has become a key concern in VLSI design. With the increasing demand for portable electronics such as smartphones, laptops, and personal communication devices, the focus on low-power design has grown significantly. In VLSI systems, power usage is generally categorized into dynamic and static power, with dynamic power being the dominant component. However, as MOSFETs continue to scale down to nanometer dimensions—driven by Moore's law—leakage currents have increased, making static power a more important factor in total power consumption. This static power primarily comes from leakage between the source and drain, and managing the bulk terminal of CMOS devices can help enhance performance by reducing both power dissipation and delay. One effective method to achieve low power is to operate transistors in the sub-threshold region.

Adders are essential components in systems like processors, memory units, and arithmetic logic units (ALUs), and XOR/XNOR gates are fundamental building blocks in these designs. Therefore, optimizing the design of these gates plays a major role in improving overall performance and reducing power consumption in VLSI systems. Many techniques have been proposed to enhance XOR/XNOR gate performance. Traditional implementations using static CMOS pull-up and pull-down networks tend to require more transistors. Some designs, such as a three-input XOR with minimal transistor count and no complementary inputs, have been introduced. Other approaches like pass transistor logic (PTL)-based XOR/XNOR circuits using 4 or 6 transistors have also been proposed, although they suffer from signal degradation issues. More innovative designs, like powerless XOR and groundless XNOR circuits, as well as circuits based on transmission gates and inverters (offering better drive strength at the cost of higher power), have also been studied. XOR/XNOR designs with dual feedback networks have been suggested for further improvements.

In this paper, modified XOR/XNOR gates are introduced using body biasing techniques. Five different approaches have been proposed with the goal of improving the power efficiency of single-bit full adders while reducing the number of transistors. The structure of the paper is as follows: Section II discusses the application of body biasing to XOR/XNOR gates and presents the modified gate and adder designs using a structured approach with multiplexers. Section III reports the simulation results of these modified circuits and includes a comparative analysis. Finally, Section IV summarizes the conclusions.

2. SYSTEM DESCRIPTION

Applying body biasing to XOR/XNOR gates and full adder circuits helps reduce power consumption by increasing the threshold voltage (V_{th}) of each transistor, which in turn lowers leakage currents. The design of single-bit full adders follows a structured approach, as illustrated in Figure 1, utilizing XOR/XNOR gates along with two multiplexers.

For the circuit design, a gate length of 0.35 µm is used for both NMOS and PMOS transistors. The transistor widths are set at 1.0 µm for NMOS and 2.5 µm for PMOS. These circuits have been simulated using SPICE with TSMC 0.35 µm model files, operating at a supply voltage of 3.3V.

The following sections describe the different proposed methodologies in detail.

A Methodology: I

In this method, a full adder is designed using XOR/XNOR gates that incorporate forward feedback loops along with multiplexer blocks. The body terminals of all PMOS transistors are connected to a constant voltage of 3.3V, while a body bias ranging from 0 to -3.3V is applied to the NMOS transistors. The schematic of the XOR/XNOR gate is shown in Figure 2(a), and the complete full adder circuit using body biasing is illustrated in Figure 2(b).

B. Methodology: II

In this approach [Figure 3(a)], an additional voltage bias is applied to the PMOS transistors (P1 and P2) within the XOR/XNOR gates, replacing the ground connection used in Figure 2(a). The applied bias voltage (V3) for P1 and P2 is varied within the range of 0 to 3.3V. Additionally, substrate biasing of 3.3V for the PMOS transistors and -3.3V for the NMOS transistors is used. This modified XOR/XNOR gate is then used to construct a full adder, incorporating two multiplexers, as shown in Figure 3(b).

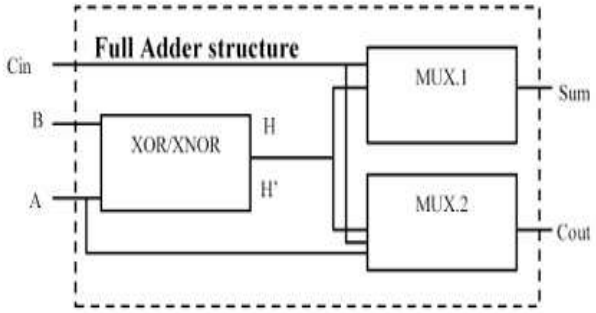

Figure 1. Structure of single bit full adder

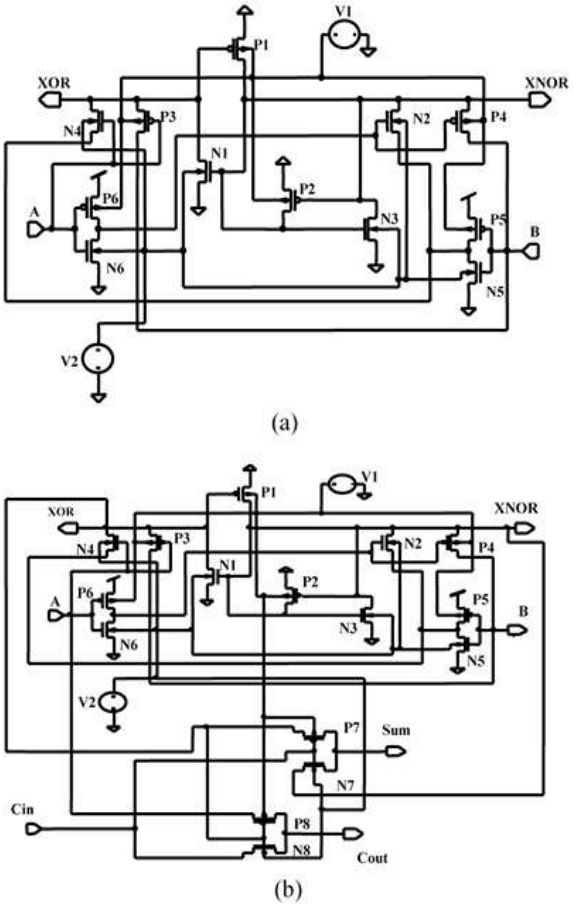

Figure 2. Circuits with body bias (a) XOR/XNOR gate (b) Full adder

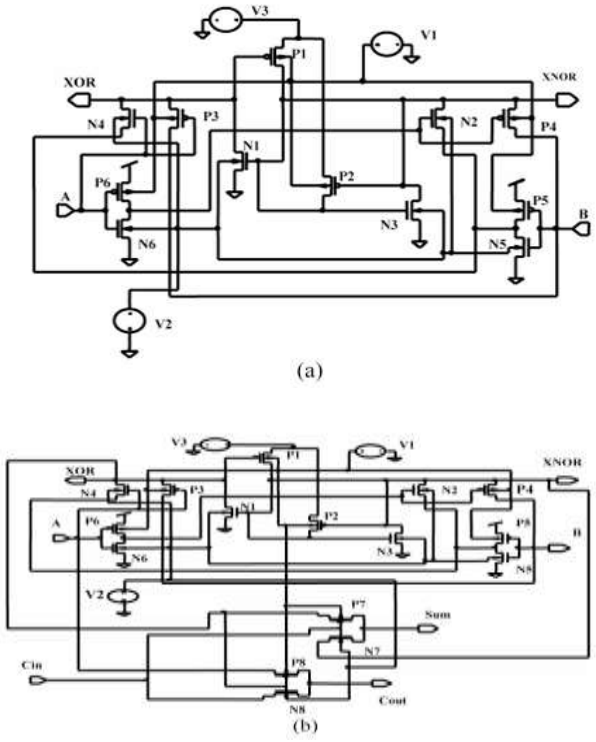

Figure 3. Circuits with an additional biasing of P1 & P2 (a) XOR/XNOR (b) Full adder

C. Methodology: III

In the previous methodology, the XNOR section was identified as the main contributor to power consumption. To address this, the design shown in Figure 4(a) eliminates the XNOR portion entirely, replacing its function with an inverter. A body bias voltage ranging from 0 to -3.3V is applied to the NMOS transistors, while a fixed bias of 3.3V is used for the PMOS transistors. Using this revised circuit, a full adder is implemented as illustrated in Figure 4(b).

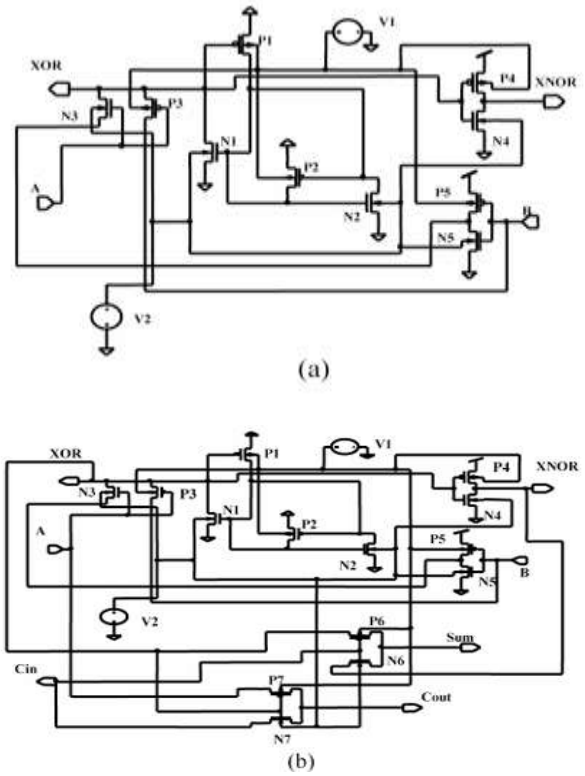

Figure 4. Modified Circuit (a) XOR with inverter (b) Full adder

3. RESULTS AND DISCUSSIONS

Simulation results for the XOR/XNOR gate and full adder without any body biasing indicate high power consumption values—939.15 µW for the gate and 946.99 µW for the full adder. Tables I and II summarize the simulation outcomes for Methodologies I through V under various body biasing conditions. Across all proposed methods, a significant reduction in power dissipation is observed with the introduction of body biasing, while only a slight trade-off in delay is noted. This improvement is primarily due to the increased threshold voltage of the transistors, which helps suppress sub-threshold leakage currents.

In Methodology I, the lowest power consumption recorded for the XOR/XNOR gate is 204.07 µW, while the full adder consumes 204.09 µW at a bias voltage of 3.3V for PMOS and -3.3V for NMOS transistors. The delay for the full adder varies from 5.1120 ns to 5.9849 ns as the NMOS body bias is swept from 0 to -3.3V. The minimum power consumption of 204.09 µW is achieved at a -3.3V bias, with the corresponding maximum delay being 5.9849 ns. The power-delay product (PDP) also improves, ranging from 2501.55 fJ down to 1221.45 fJ as the body bias increases, indicating enhanced efficiency. Table III further highlights that Methodology I provides a substantial improvement in PDP due to effective body biasing.

For Methodology II [Figure 3], results show that power consumption decreases as the additional bias voltage applied to PMOS transistors P1 and P2 is increased, up to a point. Specifically, a reduction in power is seen as the bias increases to 1.5V. This effect is attributed to reduced leakage currents flowing to ground due to the biasing. However, beyond 1.5V, the benefits of biasing diminish, and power consumption begins to rise again. This is likely due to the higher bias voltage starting to directly influence the power consumption, offsetting earlier gains.

Table I. Power Consumption Comparisons of Proposed Methodologies with Body Bias

Methodology-I			Methodology-II			Methodology-III		
NMOS body bias (V)	XOR/XNOR power (µW)	Full adder power (µW)	P1 and P2 Bias (V)	XOR/XNOR power (µW)	Full adder power (µW)	NMOS body bias (V)	XOR/XNOR power (µW)	Full adder power (µW)
0	481.11	489.35	0	204.09	204.10	0	1.24	1.39
-0.5	431.25	431.37	0.5	178.83	178.85	-0.5	0.201	0.516
-1.0	380.37	380.44	1.0	155.53	155.57	-1.0	0.136	0.234
-1.5	334.92	334.95	1.5	128.89	128.92	-1.5	0.151	0.223
-2.0	293.85	293.87	2.0	155.98	156.01	-2.0	0.177	0.259
-2.5	256.55	256.57	2.5	334.03	334.03	-2.5	0.209	0.304
-3.0	222.72	222.74	3.0	633.40	633.65	-3.0	0.246	0.356
-3.3	204.07	204.09	3.3	862.02	862.03	-3.3	0.271	0.391

Table II. Delay Comparisons of Proposed Methodologies with Body Bias

Methodology-I		Methodology-II		Methodology-III	
NMOS body bias (V)	Maximum output delay of full adder (ns)	1 and P2 Bias Volt-age(V)	Maximum output delay of full ad-der (ns)	NMOS body bias voltage(V)	Maximum output delay of full adder (ns)
0	5.1120	0	5.9847	0	5.0928
-0.5	5.1457	0.5	5.9854	-0.5	5.1285
-1.0	5.1833	1.0	5.9859	-1.0	5.17212
-1.5	5.2293	1.5	5.9875	-1.5	5.2352
-2.0	5.298	2.0	6.0191	-2.0	5.3361
-2.5	5.4195	2.5	10.1072	-2.5	5.51078
-3.0	5.6727	3.0	10.0236	-3.0	5.9223
-3.3	5.9849	3.3	10.0251	-3.3	6.4337

Table III. Power Delay Product Comparisons of Proposed Methodologies with Body Bias

Methodology-I		Methodology-II		Methodology-III	
NMOS body bias (V)	Power delay product (fJ)	P1 and P2 Bias Voltage (V)	Power delay product (fJ)	NMOS body bias voltage (V)	Power delay product (fJ)
0	2501.55	0	1221.47	0	0.00707
-0.5	2219.70	0.5	1070.48	-0.5	0.00264
-1.0	1971.93	1.0	931.22	-1.0	0.00121
-1.5	1751.55	1.5	771.90	-1.5	0.00116
-2.0	1556.92	2.0	939.03	-2.0	0.00138
-2.5	1390.48	2.5	3376.10	-2.5	0.00167
-3.0	1263.53	3.0	6351.45	-3.0	0.00210
-3.3	1221.45	3.3	8641.93	-3.3	0.00251

Simulation results for the XOR/XNOR gate and full adder, as described in Methodology III [Figure 4], demonstrate a significant drop in power consumption when body biasing is applied to NMOS transistors. This reduction is primarily due to lower leakage currents resulting from an increased threshold voltage. It has been noted that after -1.0V of NMOS biasing, further increases have minimal effect on power savings. The XOR/XNOR module achieves its lowest power consumption of 0.136 nW with a body bias of -1.0V for NMOS and 3.3V for PMOS transistors. For the full adder utilizing this modified gate, the minimum power usage is observed at 0.223 nW under -1.5V NMOS biasing and 3.3V PMOS biasing.

The delay for the full adder varies between 5.0928 ns and 6.4337 ns as the NMOS body bias is adjusted from 0 to -3.3V. Although this results in a slight increase in delay, the overall power-delay product (PDP) improves significantly, ranging from 0.00707 fJ to 0.00251 fJ. This reflects a favorable trade-off between power efficiency and speed.

Table IV. Power Consumption Comparisons (TSMC 0.35µm, Supply Voltage: 3.3V)

Full Adder configuration	Power Consumption	Output delay
Conventional 28 transistors [10]	1.26nW	2.112 ns
Transmission gate 20 transistors [6]	1.25mW	4.966 ns
Transmission function 16 transistors [7]	1.24nW	25.01 ns
Pass transistor 16 transistors adder [9]	591.11µW	4.982 ns
Pass transistor 14 transistors adder [8]	0.626nW	10.107 ns
10 transistors SERF adder [11]	531.29µW	9.960 ns
Methodology-I with 14 transistors [present work]	204.09µW	5.984 ns
Methodology-II with 14 transistors [present work]	128.92µW	5.987 ns
Methodology-III with 14 transistors [present work]	0.223nW	5.235 ns

4. CONCLUSIONS

Full adder circuits incorporating XOR/XNOR gates with dual feedback and multiplexer blocks have been proposed using body biasing techniques. Compared to previously reported designs, the proposed full adders offer reduced power consumption, shorter delays, and lower transistor counts across different methodologies.

In Methodology I, the application of body biasing leads to a notable improvement in power-delay product (PDP), decreasing from 2501.55 fJ to 1221.45 fJ. Additionally, applying biasing to two PMOS transistors (P1 and P2) further reduces power consumption—from 204.07 µW to 128.89 µW for the XOR/XNOR gate, and from 204.09 µW to 128.92 µW for the full adder.

In Methodology II, PDP values range between 1221.47 fJ and 8641.93 fJ, with the lowest PDP recorded at 771.90 fJ when the bias voltage is set to 1.5V.

Methodology III, which eliminates the XNOR portion from the circuit, achieves minimum power dissipation of just 0.223 nW and a PDP of 0.00116 fJ.

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