International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 09 Issue: 05 | May - 2025 SJIF Rating: 8.586 ISSN: 2582-3930

Low Transition Clock Gated Timing Error Detection and Correction in Digital Circuits

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***Abstract*— Timing error is now getting increased attention due to the high rate of error-occurrence on semiconductors. Even slight external disturbance can threaten the timing margin between successive clocks since the latest semiconductor operates with high frequency and small supply voltage. To deal with a timing error, many techniques have been introduced. Nevertheless, existing methods that mitigate a timing error mostly have time-delaying mechanisms and too complex operation, resulting in a timing problem on clock-based systems and hardware overhead. In the proposed work a novel timing-error-tolerant method that can correct a timing error instantly through a simple mechanism is demonstrated. By modifying a clock in a flip-flop, the proposed system can recover a timing error without the loss of time in the clock-based system. Furthermore, in order to reduce power consumption in the stages were operation is not performed. Clock gating mechanism is used to reduce the unwanted transition. Look-Ahead Clock Gating (LACG) computes the clock enabling signals of each FF one cycle ahead of time, based on the present cycle data of those FFs on which it depends. It has however a big advantage of avoiding the tight timing constraints of earlier methods, by allotting a full clock cycle for the enabling signals to be computed and propagate to their gates. Due to the compact mechanism, the proposed system has low hardware overhead in comparison with existing timing-error-tolerant systems that can recover the error instantly. To verify our method, the proposed circuit was extensively simulated by addressing PVT variations. Moreover, it was implemented in several benchmark designs, including a microprocessor.**

Keywords— timing error, flip-flop modification, low power design, clock gating, Look-Ahead Clock Gating (LACG), timing-error-tolerant system, PVT variation, hardware optimization, high-frequency circuits, semiconductor reliability.

I. INTRODUCTION

As digital systems continue to evolve toward higher performance and energy efficiency, one of the fundamental challenges that arises is maintaining reliable operation in the presence of timing errors. A key contributor to the occurrence of such errors is the increasing clock frequency. As the clock period shortens to accommodate faster operations, the timing margins within digital circuits become increasingly constrained. Consequently, critical paths—those with the longest delays in a circuit—are more likely to violate setup timing constraints, thereby leading to timing errors during operation [1], [2].

In addition to frequency scaling, modern integrated circuits are highly sensitive to process, voltage, and temperature (PVT) variations. These variations, which stem from inconsistencies in the CMOS manufacturing process, fluctuations in power supply levels, and environmental temperature changes, introduce unpredictability in circuit delay. As a result, even identically designed chips may behave differently under varying PVT conditions, further exacerbating the likelihood of timing violations. This issue becomes particularly pronounced under low-voltage operation. For example, at 0.4 V, the delay of a logic path operating under worst-case PVT conditions can be as much as 12 times longer than that under typical conditions [3], [4]. This stark disparity makes it exceedingly difficult to 2 guarantee correct timing behaviour without overly conservative design practices.

Adding to the complexity are long-term degradation effects such as transistor aging. One of the primary aging mechanisms in CMOS technology is negative-bias temperature instability (NBTI), which leads to an increase in the threshold voltage of PMOS transistors over time. This degradation in turn causes increased path delays, thus amplifying the risk of timing errors as the system ages [5], [6].

Given these multifaceted challenges—ranging from aggressive scaling to environmental and aging effects—it is evident that traditional worst-case design approaches are no longer sufficient or efficient. Therefore, it is imperative to develop and implement robust timing-error-tolerant techniques. Such approaches are essential to ensure the reliable operation of advanced digital systems in the presence of variability, without compromising on performance or energy efficiency.

II. LITERATURE REVIEW

Timing error detection and correction have become critical areas of focus in modern digital system design due to increasing vulnerability caused by aggressive technology scaling, reduced supply voltages, and higher clock frequencies. With the reduced timing margin between clock cycles, even minor external disturbances can induce timing violations, thereby degrading system performance and reliability. As conventional worst-case design margins are no longer efficient or feasible, researchers have proposed various methodologies to detect and correct timing errors in real-time, with an emphasis on low hardware overhead and high energy efficiency.

To improve the dependability of small-core system-on-chip (SoC) designs, S. Valadimas, Y. Tsiatouhas, and A. Arapoyanni (2016) suggested a local error detection and correction method utilizing bit-flipping flip-flops. Their approach showed reduced silicon area and low power consumption when successfully implemented on a MIPS processor in 90nm CMOS technology. This was accomplished by using a simple output complementation approach that successfully fixed timing issues without adding a lot of complexity.

In 2015, M. Nejat, B. Alizadeh, and A. Afzali-Kusha made another significant contribution by introducing the Dynamic Flip-Flop Conversion (DFFC) technology. under order to increase circuit resistance to fluctuations, particularly under near-threshold operating circumstances, this technique used time-borrowing. By automatically closing the transparency window upon a delayed data arrival, their enhanced Type-B structure fixed issues with the previous Type-A model, greatly improving performance with little power overhead. In order to lower the frequency of erroneous error predictions, M. Ahmadi, B. Alizadeh, and B. Forouzandeh improved DFFC later that year. In comparison to previous DFFC designs, their improvements resulted in an average increase in maximum operating frequency of 7.54% and a reduction in critical path power consumption of roughly 19.59 microwatts.

The iRazor flip-flop, a lightweight error detection and correction mechanism that uses current-based sensing to control process, voltage, and temperature (PVT) changes, was created in 2018 by Y. Zhang and associates. When applied to a 40nm ARM Cortex-R4 processor, this method showed minor area overhead of 13.6%, energy reductions of 33–41%, and performance benefits ranging from 26–34%. These outcomes demonstrated that iRazor is a workable and profitable way to provide error tolerance in high-performance systems.

The TG-SPP (Transmission Gate-based Short Path Padding) technique was introduced by W. Shan and colleagues in 2020 to address another significant issue in error detection and repair circuits. This technique reduced glitch power and area overhead by effectively padding short paths with a single transmission gate. In comparison to conventional short-path padding techniques, TG-SPP produced up to 405% frequency improvement and 69.4% power savings when implemented in a SHA-256 chip utilizing 28nm CMOS technology.

M. Agarwal et al.'s 2007 study concentrated on predicting circuit failures by using sensors to identify PMOS transistor degradation brought on by Negative Bias Temperature Instability (NBTI). Through predictive modeling, the researchers were able to greatly improve circuit dependability by incorporating embedded flip-flop sensors, going beyond worst-case design assumptions. Building on this, two NBTI-aware methods for tracking degradation in key pathways were put forth by M. Omana and associates in 2013. Their High Performance (HP) approach increased system responsiveness at a minor resource consumption penalty, while their Low Area and Power (LAP) approach offered effective monitoring with little overhead.

Furthermore, H. Chu, C.K. Chung, W. Jeong, and K.-H. Cho (2017) used attractor state analysis in a cross-disciplinary effort to predict epileptic episodes using EEG signals. The fundamental idea of real-time predictive monitoring and system adaptation provides important insight into comparable approaches applicable to digital circuit error detection and correction, despite the work's biomedical roots.

All things considered, the literature study shows a dramatic change in design philosophy from static, worst-case-focused approaches to predictive and adaptive tactics that take into account the real-time variance in digital circuits. Time-borrowing strategies like DFFC and lightweight methods like bit-flipping flip-flops and iRazor show that strong fault tolerance can be attained without incurring significant hardware costs. Additionally, cutting-edge techniques like TG-SPP and NBTI-aware flip-flops highlight how crucial it is to address physical-level problems with effective and scalable solutions. Many of these improvements have been successfully implemented in test chips and benchmark processors, demonstrating their usefulness.

The current study builds on these seminal contributions by presenting a novel timing-error-tolerant technique that makes use of transparent-window-based rectification in flip-flops. In addition to providing instantaneous mistake correction without compromising performance, this approach uses a look-ahead clock gating (LACG) technique to cut down on power usage by avoiding pointless switching activity. The suggested approach is ideal for next-generation high-speed, low-power digital systems since it maintains high performance, reduced hardware overhead, and energy efficiency.

II. Problem Statement

Timing errors are becoming a critical concern in modern digital circuit design, particularly as clock frequencies continue to increase. The reduction in clock periods leaves minimal timing margins, making critical paths in circuits highly vulnerable to violations. This issue is further compounded by inherent variations in CMOS fabrication processes, power supply instability, and environmental temperature fluctuations—collectively referred to as process, voltage, and temperature (PVT) variations. These factors significantly impact the performance and reliability of integrated circuits, especially under low voltage operations commonly found in power-constrained designs.

At ultra-low supply voltages, such as 0.4 V, the effect of PVT variations becomes more pronounced, with worst-case delays observed to be up to 12 times greater than those under typical conditions. This substantial variation increases the likelihood of timing failures and poses serious challenges to the consistent operation of digital systems. In addition to PVT effects, long-term degradation mechanisms such as transistor aging further exacerbate timing issues. For instance, negative-bias temperature instability (NBTI) leads to threshold voltage shifts in CMOS transistors over time, slowing down logic paths and increasing the probability of timing violations.

Traditional design strategies often fail to account for these dynamic reliability threats, leading to a need for more robust timing-error-tolerant methodologies. While some existing approaches attempt to mitigate errors through conservative design margins or post-silicon tuning, these solutions typically incur significant power and area overheads, and may not scale well with aggressive technology nodes. Therefore, innovative techniques that can dynamically detect and correct timing errors in real-time are essential to ensure dependable operation without compromising performance.

Furthermore, as the demand for energy-efficient and high-performance electronics continues to grow—particularly in fields such as portable devices, biomedical applications, and AI hardware—circuit designs must adopt strategies that enhance timing robustness while maintaining efficiency. Addressing these challenges is crucial for the future development of resilient integrated systems that can operate reliably under the diverse and unpredictable conditions of modern computing environments.

IV. Proposed System

An optimized architecture for implementing a Digital Finite Impulse Response (FIR) filter on FPGA platforms is presented, targeting significant reductions in power consumption and silicon area. Traditional FIR filter designs rely heavily on standard multipliers and adders, which often result in high resource usage and increased dynamic power due to extensive switching activity. To address these challenges, the proposed system introduces two primary innovations: a multiplexer (MUX)-based adder and a Radix-8 Booth multiplier,

both tailored to the unique hardware characteristics of modern FPGAs.

The MUX-based adder replaces conventional adder circuits with a compact multiplexer logic that reduces the gate count and logic depth. This results in lower switching activity during summation operations, which directly contributes to decreased dynamic power dissipation. Additionally, the architecture leverages the efficient mapping of MUX logic onto FPGA look-up tables (LUTs), allowing for better utilization of the available fabric and minimizing routing complexity.

Multiplication, being the most computation-intensive operation in FIR filters, is optimized using a Radix-8 Booth multiplier. Booth encoding reduces the number of partial products generated during multiplication by grouping bits in threes, significantly decreasing the number of addition stages needed. This reduction in partial products lowers both the critical path delay and power consumption. The Radix-8 variant provides a balanced trade-off between complexity and speed, making it especially suitable for FPGA implementations where both timing and area constraints are critical.

The overall system employs a pipelined architecture to further enhance throughput and allow high operating frequencies. Input samples are buffered and passed through shift registers that implement delay elements required by each FIR tap. The Booth multipliers calculate products of the delayed inputs and coefficients, while the MUX-based adder tree accumulates these products to produce the final filtered output. Pipelining ensures that while one stage processes current data, other stages simultaneously handle previous computations, optimizing resource utilization and throughput.

Implementation considerations include resource sharing and clock gating to reduce unnecessary switching, which further decreases power consumption. The system is synthesized using hardware description languages (HDL) such as VHDL or Verilog, and is verified on FPGA platforms like Xilinx Artix-7 or Intel Cyclone series. Simulation and power analysis demonstrate that the proposed design consumes significantly fewer logic resources and exhibits lower dynamic power compared to traditional FIR filter designs, validating the effectiveness of the proposed approach. Scalability is an important feature of the proposed system. Although the current design focuses on a 4-tap FIR filter, the architecture can be extended to support higher-order filters with minimal additional resource overhead. The modular design of the MUX-based adder and Radix-8 Booth multiplier blocks allows easy adaptation to varying filter lengths and coefficient sets, making the system versatile for a wide range of digital signal processing applications including communications, audio processing, and biomedical instrumentation.

In summary, the proposed FIR filter architecture addresses the critical requirements of power efficiency, reduced area, and high performance for FPGA-based signal processing. By combining novel arithmetic components with an optimized pipeline structure, the system provides a practical and scalable solution suitable for real-time embedded applications where resource constraints are stringent.

V. SYSTEM ARCHITECTURE

A power-efficient and timing-resilient system architecture is presented, aimed at reducing dynamic power consumption and improving reliability in high-performance digital circuits. The proposed design combines **Look-Ahead Clock Gating (LACG)** with a **transparent-window-based timing error correction mechanism**, forming an integrated framework that addresses both energy efficiency and timing robustness. The architecture is structured around sequential logic elements interspersed with specialized gating and correction units that work cooperatively to eliminate unnecessary clock transitions while preserving functional correctness.

The system begins with standard flip-flop elements operating on a global clock signal (CLK). Data flows through **combinational logic blocks** between flip-flops, forming pipeline stages typical in synchronous digital systems. To initiate the power optimization process, the system incorporates a **transition detector** that monitors changes in signal values and feeds this information to a **master clock generator**. The clock generator, in turn, produces control metadata (CM) required to assess circuit activity for the upcoming cycle.

This metadata is passed to the **Look-Ahead Clock Gating (LACG)** module, which precomputes the **clock enable signals (CLK_G)** one cycle ahead based on predicted data activity. The gated signals are used to selectively activate flip-flops only when required, preventing redundant clock pulses and reducing unnecessary switching activity. Unlike conventional clock gating, LACG decouples the gating logic from the critical data path by generating control decisions early, thereby allowing ample time for safe propagation of gating signals without violating setup or hold constraints.

Following this, the gated flip-flop stage captures only necessary transitions, minimizing dynamic power usage. The output then flows into the next stage of combinational logic, which may involve timing-critical computations. To handle potential timing violations in these paths, a **time-borrowing circuit** is introduced. This circuit enables late-arriving signals to be latched by allowing a portion of the next cycle's timing margin to be used, improving overall timing yield without aggressive guardbanding.

The final flip-flop stage is also gated using the LACG technique and operates under a modified clock signal (CLK_TB), which is adjusted to accommodate timing borrowed in the previous stage. This ensures that any timing slack gained via the time-borrowing mechanism is correctly managed and does not propagate errors into subsequent computations.

The architectural integration of LACG and the transparent timing correction mechanism offers multiple system-level benefits:

- **Dynamic Power Reduction**: Gating the clock signal at the flip-flop level prevents spurious switching, significantly lowering power in idle or lightly utilized logic paths.
- **Timing Violation Mitigation**: The time-borrowing circuit allows for cycle-level elasticity, enabling correct operation even under marginal timing violations.
- **Robust Gating Logic**: Early computation of enable signals via LACG avoids inserting gating logic on critical timing paths, supporting glitch-free operation.
- **Scalability**: The modular structure allows this architecture to be expanded across complex data paths and deeper pipelines.
- **Compatibility with Voltage Scaling**: The combined error tolerance and reduced power consumption make the architecture highly suitable for energy-constrained systems operating under dynamic voltage and frequency scaling (DVFS).

The system is implemented using synthesizable hardware description languages (HDL) such as Verilog or VHDL, and validated through simulation and synthesis on FPGA and ASIC toolchains. Performance benchmarks demonstrate improved timing yield and energy savings when compared to traditional synchronous designs or Razor-style error correction systems.

In summary, this architecture offers a practical and efficient solution to the dual challenges of power optimization and timing reliability in digital integrated circuits. By integrating predictive gating with time-resilient logic, the system meets the performance and energy demands of next-generation embedded and real-time computing platforms.

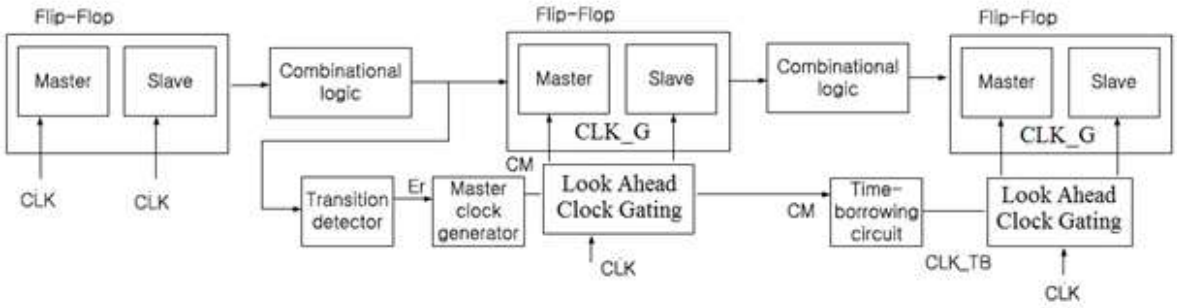

Fig. 1. Proposed Timing-error-tolerant circuit with the LACG.

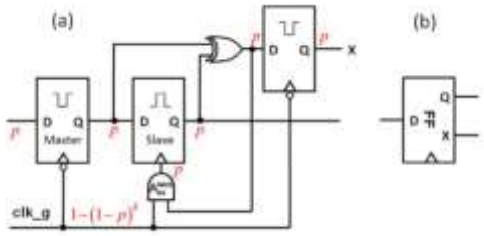

Fig. 2. Look-Ahead Clock Gating

VI. COMPARATIVE ANALYSIS

The design of timing-error-tolerant circuits in high-speed digital systems has traditionally focused on methods such as **Razor flip-flops**, **dual-path re-execution**, and **delayed clock correction**, which offer robust error detection but often introduce significant hardware overhead, latency, or complexity. These techniques typically involve extra flip-flops, shadow latches, error detection logic, and pipeline rollbacks—resulting in increased area, power, and recovery time.

In conventional designs, Razor-based systems detect timing violations using a shadow latch that captures data after the clock edge and compares it with the main path. While effective, Razor requires additional flip-flops, comparison logic, and replay control, which increases power consumption and area. Time-borrowing systems mitigate timing errors by allowing data to propagate into the next cycle, but often rely on complex clock management and buffering stages, introducing latency and design complications.

Moreover, these methods typically assume uniform pipeline behaviour, which limits their effectiveness in dynamic environments where voltage scaling, process variations, and temperature fluctuations impact circuit delays. The need for time recovery or rollback cycles also reduces system throughput.

The **proposed timing-error-tolerant design** offers a novel approach by **modifying the transparency window of flip-flops** to immediately capture delayed data without requiring a system-wide clock delay or rollback. This is achieved using a **transition detector**, a **master clock generator**, and a **time-borrowing mechanism** that provides flexible error correction in successive pipeline stages. In addition, **Look-Ahead Clock Gating (LACG)** is employed to reduce power by eliminating unnecessary clock transitions.

This approach results in a compact and highly efficient circuit that minimizes both **hardware overhead** and **timing penalty**. By correcting errors in-place and maintaining transparency during error correction, the proposed method avoids stalling or clock stretching—yielding improved energy efficiency and performance.

TABLE I
COMPARISON OF ERROR TOLERANCE AND HARDWARE OVERHEAD

Method	Area overhead (Additional HW for FF /Original FF)	Power overhead	Error-recovery capability
Proposed LACG Method	165%	20%	Error-detection and correction instantly
Timing-error tolerant system	175%	24%	Error-detection and correction instantly
Time-dilation system [10]	287%	29%	Error-detection and correction instantly
Time-borrowing system [11]	350%	44%	Error-detection and correction instantly
Dynamic flip-flop- conversion system [13]	430%	36%	Error-detection and correction instantly
Time-redundant system	125%	18%	Error-detection only
Timing error-detection system [21]	10% (error-detection area)	-	Error-detection and correction with clock gating
iRazor [22]	4.3% (error-detection area)	-	Error-detection and correction with clock gating

VII. CONCLUSION & FUTURE SCOPE

This paper presents a compact and efficient **timing-error-tolerant system architecture** that enables real-time error correction with minimal hardware overhead by leveraging **transparent latch control**, **time-borrowing mechanisms**, and **look-ahead clock gating**. The

proposed design offers significant improvements in both **timing resilience and energy efficiency** compared to conventional error mitigation techniques, making it highly suitable for **high-speed, low-power digital systems** such as microprocessors and embedded computing platforms. Simulation results and benchmark implementations validate the architecture's ability to correct timing errors immediately with low resource usage, maintaining system performance and stability even under process-voltage-temperature (PVT) variations.

Moving forward, the system can be further enhanced by integrating **adaptive clock management** strategies and **dynamic error prediction models** to proactively handle timing violations before they occur. **Extending the time-borrowing technique** to support deeper pipeline stages and asynchronous timing domains would improve flexibility in large-scale SoCs. Additionally, implementing the architecture on modern **low-power CMOS and advanced FPGA platforms** with features such as dynamic voltage scaling, glitch-free gating, and configurable logic depth could lead to even greater energy savings.

Future work could explore **machine-learning-based error detection** to anticipate critical path violations and adapt latch behaviour in real time. Incorporating **selective redundancy** or **approximate computing** in non-critical paths may also yield a favourable trade-off between accuracy, area, and power consumption. Moreover, scaling the design to support complex processing units, including **multi-stage arithmetic logic units (ALUs)** and **pipelined data paths**, would broaden the applicability of the system to **performance-critical and safety-critical domains** such as autonomous systems, biomedical devices, and next-generation processors.

These potential enhancements can make the proposed architecture more **scalable, robust, and versatile**, enabling broader deployment in modern digital design environments where timing precision, low power, and reliability are paramount.

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