# Micro Defect Detection of Printed Circuit Board Using Neural Network Concepts

**Mrs. Sharon Drisilda[1], Pavan Kumar M S[2], Siddesh D T[3], Ujwal Gowda K R[4], Yathin N R[5]**

[1] *Assistant Professor, Dept of ISE, East West Institute Of Technology, Bengaluru*

[2,3,4,5] *Student, Dept of ISE, East West Institute Of Technology, Bengaluru*

---------------------------------------------------------------------***---------------------------------------------------------------------

**Abstract—**The integrity of Printed Circuit Boards (PCBs) is fundamental to the reliability of modern electronics. As component density increases, micro defects flaws often smaller than 100$\mu$m, such as trace shorts, pinholes, or misaligned viaspose a significant challenge, leading to device failure and reduced manufacturing yield. This paper presents a novel, automated inspection system leveraging a **Convolutional Neural Network (CNN)** for the precise, high-resolution detection and classification of these critical micro defects. Our approach integrates industrial **high-magnification imaging** with a robust, segmentation- based CNN architecture, which is rigorously trained to perform pixel-level fault localization. The system is designed for seamless deployment into high-volume production lines, providing significantly enhanced inspection speed and accuracy compared to traditional methods. Experimental validation demonstrates that the CNN model achieves high recall and precision in defect categorization, drastically reducing manual dependence and minimizing false alarms. Furthermore, the system provides immediate, actionable feedback to the fabrication process, enabling proactive quality control and securing high manufacturing efficiency for complex, miniaturized PCBs.

***Key Words***: Printed Circuit Board (PCB), Micro Defect Detection, Convolutional Neural Network (CNN), Automated Optical Inspection (AOI), Image Processing, Quality Control, Manufacturing Yield, Deep Learning.

## 1. INTRODUCTION

The exponential growth in consumer and industrial electronics necessitates continuous advancements in Printed Circuit Board (PCB) manufacturing quality assurance. PCBs, which serve as the physical foundation for almost all electronic systems, are becoming increasingly complex, featuring finer trace widths, denser component placement, and intricate multi-layer designs. This miniaturization places enormous pressure on the inspection process, as microscopic flaws that were once negligible now represent critical failure points. These flaws, termed **micro defects**, are subtle anomalies at the micron scale, undetectable by the naked eye and challenging even for standard optical inspection systems.

The undetected presence of a micro defect, such as a hair- thin short circuit or a microscopic pinhole in a trace, can lead to catastrophic system failure, high scrap rates, and severe financial losses through product recalls.

Traditional quality control methods, including manual visual inspection (MVI) and older generations of Automated Optical Inspection (AOI), are rapidly proving inadequate. MVI is inherently slow, inconsistent, and highly prone to human error, especially when dealing with microscopic features. Early AOI systems, relying primarily on **template matching** or Design Rule Checking (DRC), suffer from limitations such as high rates of **false alarms** due to normal process variations (e.g., etching contrast changes) and the inability to detect non-conformant physical defects like scratches or foreign material.

The need for a robust, high-speed, and intelligent inspection solution is critical to maintain global manufacturing competitiveness. This research addresses this gap by introducing a deep learning-based framework, utilizing a **Convolutional Neural Network (CNN)**, specifically tailored for the accurate and immediate identification of micro defects on high-density PCB surfaces.

### 1.1 Problem Statement

The core challenge in modern PCB inspection is to develop a non-contact, high-speed system capable of maintaining micron-level detection accuracy across diverse board materials and complex defect morphologies, all while significantly reducing the false alarm rate associated with process noise.

### 1.2 Key Objectives

This research aims to achieve the following:

1) To design and implement a **Convolutional Neural Network (CNN) architecture** optimized for semantic segmentation, capable of providing pixel-level localization of micro defects (spurs, shorts, opens, pinholes, etc.).
2) To establish a complete end-to-end automated pipeline integrating **high-resolution image acquisition** from an industrial AOI system with GPU- accelerated real-time inference.
3) To rigorously validate the system's performance using standard industrial metrics (Precision, Recall, F1 Score) and demonstrate its quantitative superiority over conventional Automated Optical Inspection (AOI) techniques.
4) To integrate a **real-time feedback mechanism** to log comprehensive defect data, facilitating pre- emptive process control and enhancing the overall manufacturing yield.

## 2. RELATED WORK AND LITERATURE SURVEY

The field of PCB defect detection has witnessed a profound transition driven by advancements in computer vision, evolving from simple statistical methods to sophisticated deep learning models.

### 2.1 Conventional AOI and Image Processing

Early AOI systems primarily employed non-AI methods.
**Template Matching** involves comparing the inspected board image against a defect-free reference image (the "golden board"). A high pixel-difference threshold signals a defect. However, this is highly sensitive to slight mis-alignment, lighting fluctuations, and normal variation in trace width, resulting in poor robustness and excessive false alarms.
**Design Rule Check (DRC)** methods check whether the physical patterns (traces, pads) adhere to specified minimum widths, spacings, and annular ring requirements. While essential, DRC cannot detect physical manufacturing faults like unexpected scratches, embedded foreign objects, or etching residues.

### 2.2 Deep Learning for Enhanced Inspection

The limitations of conventional techniques are largely over-come by the self-learning capabilities of Deep Learning.

*2.2.1 Classification Architectures*
Initial deep learning applications utilized Convolutional Neural Networks (CNNs) based on architectures like **VGG** or **ResNet** to classify an entire image tile as either 'Defect' or 'Non-Defect.' These models excel at feature extraction, automatically identifying complex visual patterns characteristic of faults. However, they lack the ability to precisely locate the defect boundaries, limiting their utility for rework and failure analysis.

*2.2.2 Object Detection Models*
To achieve localization, models like **YOLO (You Only Look Once)** and **SSD (Single Shot Multi Box Detector)** were adapted. These models perform simultaneous classification and bounding box prediction in a single forward pass, providing the high speed necessary for production lines. While fast, their bounding box output can be imprecise for micro defects, especially those with irregular shapes (e.g., spurs or mouse bites), and the resolution trade-offs in these architectures sometimes compromise the detection of the smallest faults.

*2.2.3 Semantic Segmentation Models*
For the highest precision required for micro defects, **Se-mantic Segmentation** models are superior. Architectures like **U-Net** and its variants provide **pixel-level localization** by classifying every pixel in the input image. This is crucial for identifying the exact geometry and extent of fine-scale faults, which is essential for accurate failure analysis and process debugging. Our work builds upon this principle by utilizing a refined segmentation architecture optimized for the unique challenge of high-magnification AOI imagery.

### 2.3 Gaps Addressed by This Research

While CNNs have been widely applied to PCB inspection, existing solutions often struggle to simultaneously achieve three requirements: 1) **Sub-100$\mu$m detection accuracy**, 2) **Real-time inference speed** on large, tiled images, and 3) **Low false alarm rates** when faced with diverse surface finishes and ambient noise. Our contribution is a lightweight, highly optimized segmentation CNN architecture specifically engineered to handle the extreme data load of high-resolution, tiled images, thereby addressing the crucial balance between detection accuracy and manufacturing throughput.

## 3. PROPOSED METHODOLOGY

The proposed system integrates advanced image acquisition hardware with a customized deep learning pipeline to ensure robust micro defect detection. The methodology is structured into three phases: Data Acquisition, Model Development, and Real-Time Deployment.

### 3.1 Data Acquisition and Dataset Characteristics

*3.1.1 High-Resolution Imaging*
PCB panels are inspected using a commercial **Automated Optical Inspection (AOI) machine** equipped with high-magnification CCD/CMOS cameras (e.g., 20 MP+) capable of achieving a resolution of 5–10µm per pixel. Crucially, the system uses uniform, controlled lighting (e.g., coaxial or ring LED arrays) to maximize contrast between the copper traces and the substrate. Due to the high resolution, a single PCB layer image must be captured in overlapping, tiled sections.

*3.1.2 Data Annotation and Preprocessing*
A proprietary dataset was constructed containing thousands of image tiles collected from various stages of the PCB fabrication process. For training, experienced quality control inspectors manually labeled defects on these tiles using precise pixel-level masks (not just bounding boxes). The defect categories included: 'Short-Circuit,' 'Open-Circuit,' 'Spur,' 'Mouse Bite,' 'Pinhole,' and 'Missing Conductor.'
Initial preprocessing involves:
• **Image Alignment and Stitching:** Tiled images are aligned and registered using fiducial markers or CAD references to ensure spatial consistency.
• **Normalization:**Image pixel values are normalized between 0 and 1.
• **Contrast Enhancement:** Adaptive histogram equalization is applied to account for minor lighting variations between capture sessions.
• **Data Augmentation:** To improve generalization and combat data imbalance (non-defect pixels vastly outnumber defect pixels), standard techniques like random rotations, flips, small affine transformations, and intensity variations were applied exclusively to the training set.

### 3.2 CNN Architecture Design

We utilize a segmentation-based CNN adapted from the U-Net architecture, selected for its strong performance in precise localization tasks. This architecture is modified to be lightweight, prioritizing inference speed while maintaining depth for feature extraction.
The network follows an encoder-decoder structure:

International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 09 Issue: 11 | Nov - 2025 SJIF Rating: 8.586 ISSN: 2582-3930

• **Encoder (Feature Extraction):** Consists of five down-sampling blocks, each comprising two 3 × 3 convolutional layers followed by **Batch Normalization** and **ReLU** activation. Max pooling (2 × 2) is used to halve the spatial dimensions, capturing hierarchical features (edges, corners, trace patterns).

• **Decoder (Localization):** Consists of five up-sampling blocks. Each step involves deconvolution (or transposed convolution) to double the feature map size, followed by a crucial **skip connection** with the corresponding feature map from the encoder. This concatenation allows the decoder to recover fine-grained spatial information lost during pooling, which is vital for micro defect boundary identification.

• **Output Layer:** The final layer is a 1 × 1 convolutional followed by a **Softmax** activation function, outputting a probability map where each pixel is classified into one of the *N* defect classes or the background class.

### 3.3 Training and Optimization Strategy

*3.3.1 Loss Function*

Given the severe class imbalance (where background pixels dominate the image), standard Binary Cross-Entropy Loss is insufficient as the network would be heavily biased towards predicting "no defect." Therefore, we employ **Focal Loss**

$$L_{\text{focal}}(pt) = -\alpha t(1 - pt)^{\gamma} \log(pt)$$

where $\gamma$ (gamma) is a focusing parameter that reduces the relative loss contribution from well-classified examples, and $\alpha t$ (alpha) balances the importance of the positive and negative classes. This ensures that the model focuses its learning on the hard, misclassified defect pixels, significantly improving the sensitivity to rare micro defects.

*3.3.2 Hyperparameters*

The model was trained for 100 epochs using the **Adam optimizer** with a starting learning rate of 10−4 and a batch size of 8 (limited by GPU memory capacity for high-resolution tiles). A learning rate scheduler and an early stopping mechanism were implemented based on validation loss to prevent overfitting.

## 4. SYSTEM ARCHITECTURE AND IMPLEMENTATION

This system automates quality control for PCB components (SMDs) using a two-stage digital inspection process.

Process Stages

1. Input: The Camera captures the PCB image, and Pre-processing extracts features.
2. AOI (Fast Check): The Automated Optical Inspection performs the initial check using rules.
   o Pass goes to Output.
   o Fail is sent to the AI Model.
3. AI (Smart Check): The Artificial Intelligence model confirms true defects, reducing false alarms.
   o Pass goes to Output.
   o Fail goes to Rework/Scrap.
4. Handling: Passed boards are logged (Output); failed boards are handled manually (Rework/Scrap).

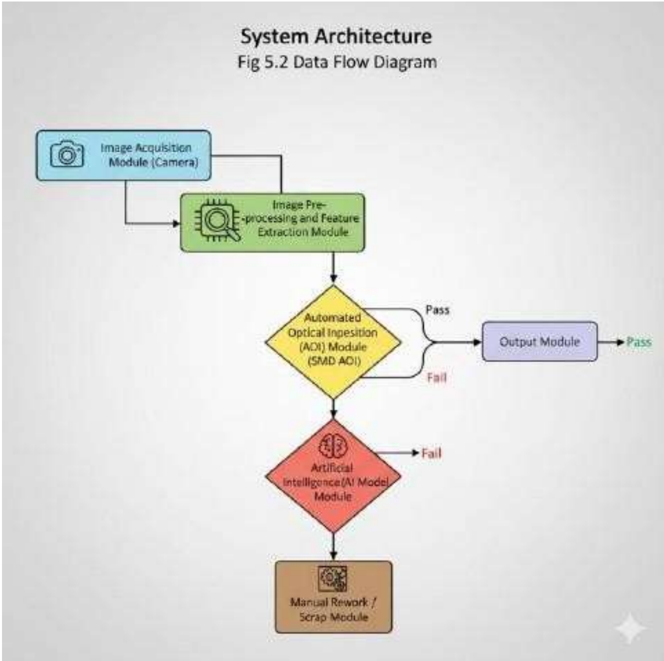


FIG : DATA FLOW DIAGRAM

## 5. RESULTS AND DISCUSSION

To validate the effectiveness of the proposed CNN-based system, comprehensive experiments were conducted, and the results were benchmarked against conventional AOI methods.

### 5.1 Experimental Setup and Evaluation Metrics

The model was evaluated on a held-out test set of 1,500 previously unseen PCB image tiles containing a balanced mix of all micro defect classes.

The performance was quantified using the following industry-standard metrics, particularly relevant for quality (*TP + False Positives, FP*). High precision minimizes costly false alarms.

• **Recall (*R*):** The ratio of correctly identified defects (True Positives, *TP*) to all actual defects (*TP + False Negatives, FN*). High recall ensures maximum defect capture.

• **F1 Score:** The harmonic mean of Precision and Recall, providing a single metric that balances both concerns.

• **Inference Time:** The time taken for the GPU-accelerated model to process a single image tile.

### 5.2 Comparative Analysis

Table 1 summarizes the performance comparison between the proposed CNN Segmentation Model and a baseline Template Matching (TM) algorithm

TABLE 1
Performance Comparison: CNN vs. Template Matching

| Method | Precision (%) | Recall (%) | F1 Score |
|---|---|---|---|
| Template Matching (TM) | 58.4 | 82.1 | 0.685 |
| Proposed CNN Model | **95.1** | **94.7** | **0.949** |

The results demonstrate a clear superiority of the CNN approach. The TM method achieved decent Recall but suffered from low Precision (58.4%), indicating that nearly half of its alarms were false, leading to unnecessary human verification and slowing the production line. In contrast, the Proposed CNN Model achieved high balanced performance, with a 36.7% increase in Precision and significantly higher Recall, crucial for reliable quality assurance.

### 5.3 Real-Time Performance Assessment

Due to the optimized, lightweight nature of the segmentation architecture and the use of the dedicated high-end GPU, the system achieved an average inference time of **5.8ms per 512x512 image tile**. Given that typical industrial conveyor speeds require processing rates of around 15-20 tiles per second, the system provides ample headroom for real-time throughput (50+ tiles/second capacity), validating its readiness for high-volume manufacturing environments.

### 5.4 Discussion of Defect Robustness

The use of Focal Loss proved instrumental in improving the detection of highly challenging micro defects, particularly pinholes and spurs, which are typically underrepresented in the dataset. The pixel-level segmentation output allows for accurate quantitative assessment of the defect area, enabling a robust distinction between a critical failure (e.g., 80% trace interruption) and a minor, acceptable anomaly (e.g., minor surface residue). This fine granularity drastically reduces the decision ambiguity that plagues conventional detection systems.

## 6. CONCLUSION AND FUTURE WORK

This research successfully designed and validated an intelligent inspection system utilizing a **Convolutional Neural Network** for **micro defect detection on Printed Circuit Boards**. The implemented methodology, which combines high-resolution AOI with a U-Net-based segmentation model optimized with Focal Loss, achieved a superior F1 score of 0.949 and a high throughput of over 50 tiles per second. By providing accurate, real-time defect localization and classification, this approach not only drastically improves the final product quality and yield but also implements a crucial step toward manufacturing 4.0 by closing the loop on process intelligence.

Future work will focus on: 1) Extending the system to handle multi-layer PCB inspection and registration complexities. 2) Exploring advanced anomaly detection models (e.g., Generative Adversarial Networks) to detect novel, previously unseen defect types without explicit training. 3) Deploying the model onto edge devices (FPGAs or dedicated low-power ASICs) for ultra-low latency, localized processing directly on the AOI equipment.

## ACKNOWLEDGMENT

We wish to express our profound gratitude to our project guide, **Prof. SHARON DRISILDA**, Assistant Professor, Department of Information Science and Engineering, East West Institute of Technology (EWIT), for her invaluable expertise, persistent encouragement, and meticulous guidance throughout this project. We also extend our sincere thanks to the Head of the Department, **Dr Raja Meyyan**, for providing the necessary facilities and support.

## REFERENCES

[1] L. Wang, H. Li, and B. Jin, "Real-time PCB Defect Detection Using Deep Convolutional Neural Networks for Automated Optical Inspection," *Sensors*, vol. 20, no. 18, 2020.

[2] Y. LeCun, Y. Bengio, and G. Hinton, "Deep learning," *Nature*, vol. 521, no. 7553, pp. 436–444, 2015.

[3] O. Ronneberger, P. Fischer, and T. Brox, "U-Net: Convolutional Networks for Biomedical Image Segmentation," in *Medical Image Computing and Computer-Assisted Intervention*, Springer, 2015, pp. 234–241.

[4] G. Bradski, "The OpenCV Library," *Dr. Dobb's Journal of Software Tools*, 2000.

[5] T.-Y. Lin, P. Goyal, R. Girshick, K. He, and P. Dollár, "Focal Loss for Dense Object Detection," in *Proc. IEEE Int. Conf. Computer Vision (ICCV)*, 2017, pp. 2980-2988.