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# Minimizing Output Ripple in Satellite BDRs Using Fuzzy Logic Control

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## ABSTRACT:

The conventional Weinberg converter is commonly employed in battery discharge regulators (BDRs) within the electrical power systems of geostationary satellites due to its high efficiency, continuous input and output currents, and the soft switching characteristics of both switches and diodes. However, a major limitation of this topology is the significant output current ripple that occurs during diode commutation. This ripple leads to increased output voltage fluctuations and higher root mean square (RMS) currents, which can degrade the lifespan of the bus capacitors and necessitate larger capacitance values—ultimately impacting the size, reliability, and operational lifespan of the satellite. Therefore, minimizing output current ripple in the BDR is essential for enhancing the overall performance of the satellite's power system. To overcome this challenge, this study introduces an improved Weinberg converter designed to reduce both output current and voltage ripple, while also minimizing magnetizing current offset in the coupled inductor. The proposed topology retains the advantages of the conventional design, including high efficiency and soft switching for all switching devices, and effectively eliminates diode reverse recovery issues. Simulation results for a 750 W prototype validate the improved converter's performance and demonstrate its suitability for advanced satellite power systems.

## INTRODUCTION:

The satellite data services market has expanded rapidly in recent years, prompting a transition from government-led initiatives to private-sector-driven satellite development [1], [2]. This shift has fueled demand for satellites supporting a wide range of missions—including communications, navigation, and weather monitoring. As mission complexity increases, satellites require more advanced and higher-capacity power systems, often resulting in greater overall mass [3–10]. To address rising launch costs while meeting escalating power demands, geostationary satellites increasingly depend on lightweight, high-power-density systems [11]. Consequently, significant research efforts have been directed toward achieving miniaturization, higher power density, and overall weight reduction in satellite systems [12–18]. Among all subsystems, the electrical power system plays a pivotal role in enabling compact, lightweight satellite designs suitable for modern mission profiles.

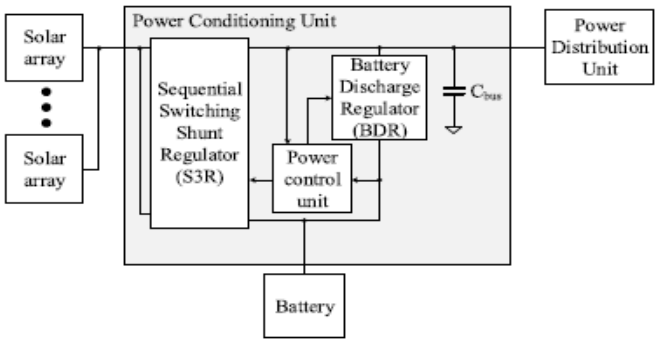
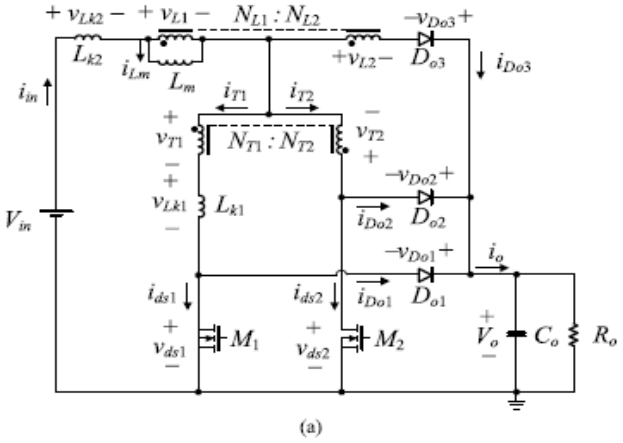



FIGURE 1. The sequential switching shunt regulator (S3R) & battery

A critical element of the electrical power system (EPS) in geostationary satellites is a regulated bus that maintains a constant voltage to ensure reliable power delivery [19], [20]. Central to this function is the power-conditioning unit (PCU), which precisely regulates the bus voltage to meet operational requirements. As illustrated in Fig. 1, the PCU architecture typically includes a battery discharge regulator (BDR), a sequential switching shunt regulator (S3R), a power control unit, and bus capacitors [21–23]. During sunlight periods, the PCU distributes power generated by the solar array, supplies the satellite's electrical load, and charges the battery. However, during eclipse periods—when the solar array is inactive—the BDR draws stored energy from the battery to maintain bus power. To minimize voltage ripple and maintain a stable supply, multiple bus capacitors are employed, ensuring consistent voltage levels across varying load conditions.



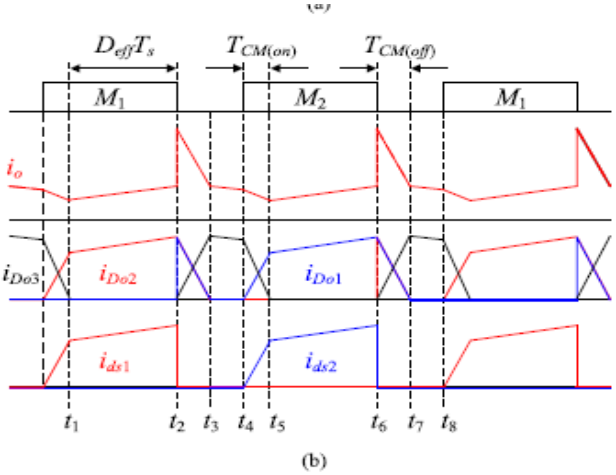



FIGURE 2. The circuit diagram and key operation waveforms of the conventional Weinberg converter (a) Conventional Weinberg converter circuit diagram, (b) The key waveforms of the current.

To enable miniaturization of the electrical power system in geostationary satellites, the volume of bus capacitors within the power-conditioning unit (PCU) must be minimized. In the typical configuration, the bus capacitor is connected to the output of the battery discharge regulator (BDR), where the bus voltage exceeds the battery voltage—necessitating a step-up conversion topology. Among various step-up converters, the conventional Weinberg converter is widely adopted for BDRs in geostationary satellite applications due to its multiple advantages, as shown in Fig. 2(a) [24–27]. These advantages include: Continuous input and output currents, which reduce stress on both the battery and the bus capacitor.Soft switching operation enabled by leakage inductance, improving overall efficiency. A working frequency that is double the switching frequency, allowing for smaller magnetic components. Voltage clamping of all switches to the output voltage, which limits voltage stress and eliminates the need for snubber circuits. Despite these benefits, the traditional Weinberg converter also has notable drawbacks, as illustrated in Fig. 2(b). When all switches are turned off, the output current rises rapidly, leading to significant current ripple. This elevated ripple increases both the output voltage ripple and the RMS current through the output capacitor, which can compromise performance and reliability. These effects are further exacerbated under higher load conditions, necessitating the use of numerous output capacitors. Consequently, the increased number and size of capacitors negatively impact the satellite's overall weight and volume, contradicting the goal of system miniaturization.

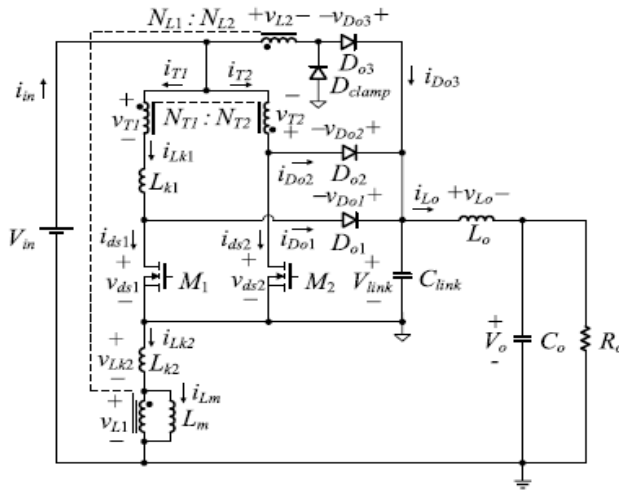



FIGURE 3. The circuit diagram of the proposed converter.

To address the limitations of the conventional Weinberg converter, an enhanced topology is proposed, as illustrated in Fig. 3. The improved converter retains the general structural framework of the standard design but introduces two key modifications: a small link capacitor (ClinkC_{link}Clink) and a small output inductor (LoL_oLo). These additions effectively mitigate the high output current ripple typically observed when all switches are turned off in the traditional configuration. Specifically, the output inductor LoL_oLo smooths the output current, ensuring minimal ripple regardless of the load current. As a result, the proposed converter significantly reduces the required number and size of output capacitors, contributing to a more compact and lightweight design. Moreover, the current in the magnetizing inductor of the coupled inductor decreases proportionally with the load current, allowing for a reduction in the magnetic core size of the coupled inductor. This contributes to both improved efficiency and reduced component bulk. Additionally, the converter's leakage inductors facilitate soft switching, minimizing turn-on losses for all switches and eliminating reverse recovery problems in the diodes. These characteristics collectively result in lower electromagnetic interference (EMI) and higher overall efficiency. To suppress voltage ringing, the output voltage is clamped using a DC lamp across diode Do3D_{o3}Do3, as depicted in Fig. 3. However, since this element has minimal impact on the overall operation of the converter, it is omitted from the mode and detailed operational analyses.

OPERATIONAL PRINCIPLES: the proposed converter operates using two switches, m1 and m2, with identical duty cycles (d) in an alternating manner, and its functional analysis is based on the following assumptions: the transformer has a sufficiently large magnetizing inductance to be neglected and a 1:1 turn ratio (nt1:nt2 = 1:1); the coupled inductor also has a 1:1 turn ratio (nl1:nl2 = 1:1) with its magnetizing inductance represented by lm; lk1 denotes the lumped leakage inductance reflected to the primary side of the transformer, while lk2 represents the leakage inductance of the coupled inductor reflected to the nl1 side; all switches (m1, m2) and output diodes (do1, do2, do3) are considered ideal; at steady state, the average voltage across all inductors is zero, implying vink=vov_{ink} = v_ovink=vo; and both the link capacitor clinkc_{link}clink and output capacitor coc_oco are sufficiently large to be modeled as constant voltage sources vinkv_{ink}vink and vov_ovo, respectively.

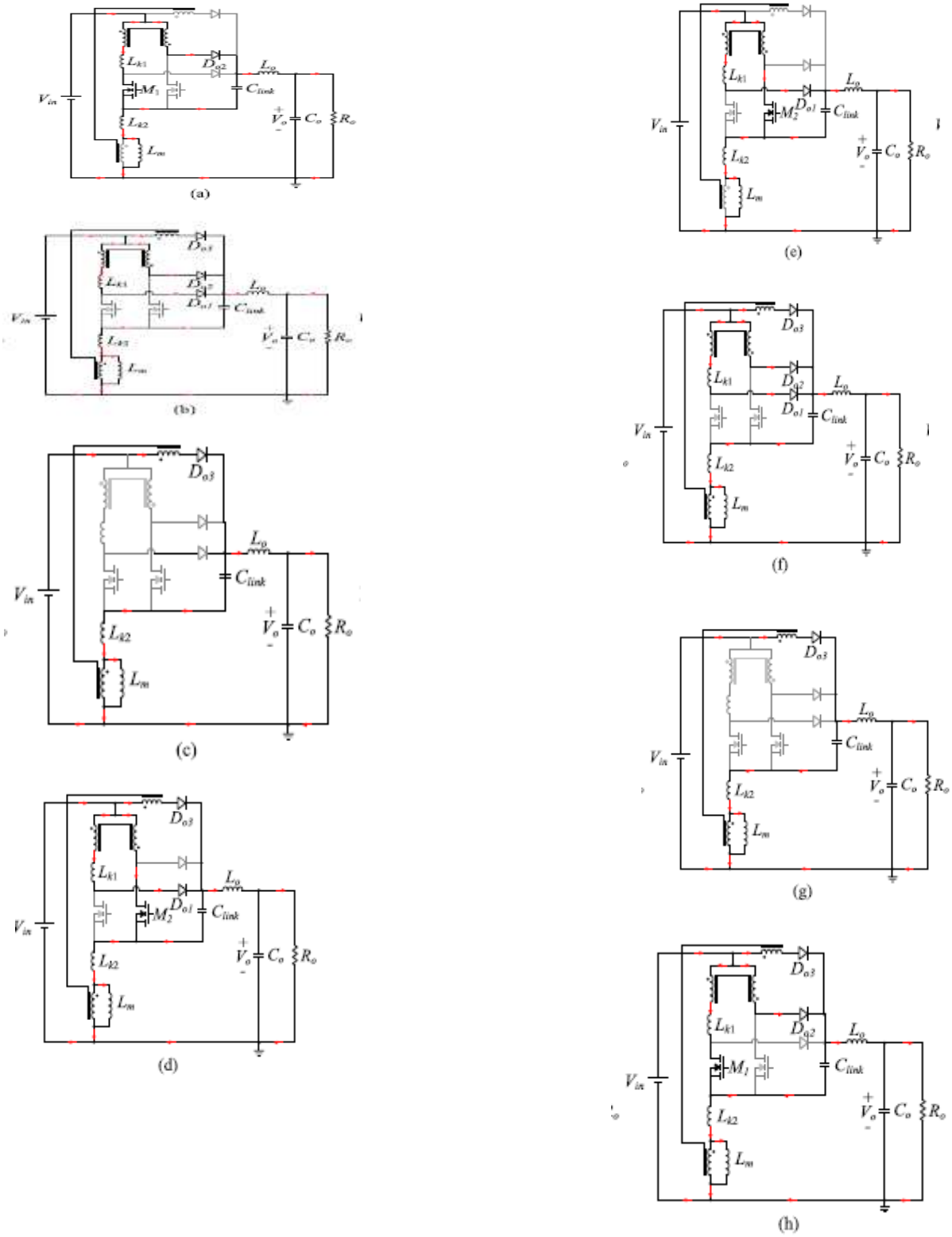



FIGURE 4. The circuit operation of the proposed converter during one period (a) Mode 1 (t1-t2), (b) Mode 2 (t2-t3), (c) Mode 3 (t3-t4), (d) Mode 4 (t4-t5),(e) Mode 5 (t5-t6), (f) Mode 6 (t6-t7), (g) Mode 7 (t7-t8), (h) Mode 8 (t8-t9).

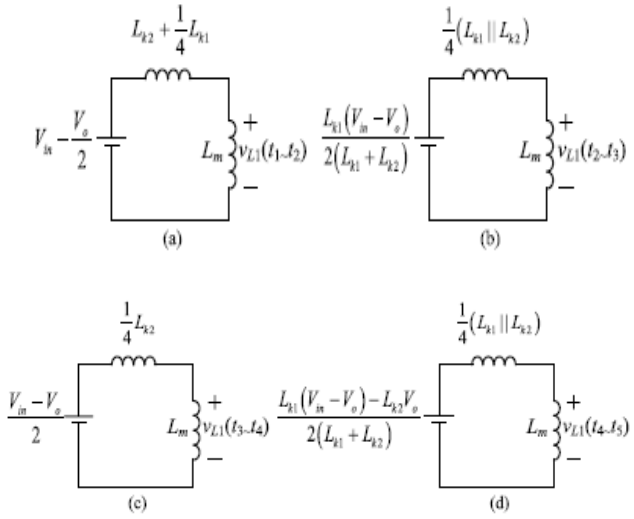



FIGURE 5. The equivalent circuits for each operation mode of the proposed converter (a) Mode 1 (t1-t2), (b) Mode 2 (t2-t3), (c) Mode 3 (t3-t4), (d) Mode 4 (t4-t5).

The proposed converter operates through eight distinct modes, as illustrated in Fig. 4, based on the switching states of the transistors and conduction states of the diodes. The equivalent circuits corresponding to Modes 1 through 4 are shown in Fig. 5, under the assumption that the output inductor LoL_oLo is significantly larger than Lk1/4L_{k1}/4Lk1/4 and Lk2/2L_{k2}/2Lk2/2. The key operational waveforms of the converter across these modes are presented in Fig. 6. Additionally, Fig. 3 provides a detailed representation of the voltage applied to each circuit component and the corresponding current flow through them.

**Mode 1 [t1-t2]:** This mode begins when the commutation between Do2 and Do3 ends at t1, and Do3 is turned off. In this mode, vL1 (= vL2) applied to the coupled inductor can be derived as follows from Fig. 5(a).

$$v_{L1}(t) = \frac{L_m(4V_{in}-2V_o)}{4L_m+4L_{k2}+Lk1} \quad (1)$$

$$v_{Lk1}(t) = \frac{L_{k1}(2V_{in}-Vo)}{4L_m+4L_{k2}+L_{k1}} \quad (2)$$

$$v_{Lk2}(t) = \frac{L_{k2}(4V_{in}-V_o)}{4L_m+4L_{k2}+L_{k1}} \quad (3)$$

$$vL_o(t) = \frac{(L_m+L_{k2})(4V_{in}-2V_o)}{4L_m+4L_{k2}+L_{k1}} \quad (4)$$

$$v_{D_o}3(t) = \frac{2L_mV_{in}+L_{k2}V_o}{4(L_m+L_{k2})} \quad (5)$$

Using (1) – (4), the currents flowing through Lm, Lk1, and Lo can be determined as follows:

$$i_{Lm}(t) = \frac{4V_{in}-2V_o}{4L_m+4L_{k2}+L_{k1}}(t-t1) + i_{Lm}(t1) \quad (6)$$

$$i_{Lk}(t) = \frac{2Vin-Vo}{4L_m+4L_{k2}+L_{k1}}(t-t1) + i_{Lk1}(t1) \quad (7)$$

$$i_{Lo}(t) = \frac{(L_m+L_{k2})(4V_{in}-2V_o)}{L_o(4L_m+4L_{k2}+L_{k1})}(t-t1) + i_{Lo}(t1) \quad (8)$$

In this mode, since Do3 is blocked, iLk2 is equal to iLm.

**Mode 2 [t2-t3]:**

vds1 rises from zero to V link = Vo when M1 is turned off at t2. Do1 is turned on and commutation between Do1, Do2, and Do3 occurs when vds1 approaches V link = Vo begins. Furthermore, the following can be used to get vL1 (= vL2) from Fig. 5(b).

$$v_{L1}(t) = \frac{2L_mL_{k1}(V_{in}-V_o)}{4L_m(L_{k1}+L_{k2})+L_{k1}L_{k2}} \quad (9)$$

If 4Lm in (9) is big enough compared to Lk1||Lk2, then vL1 can be expressed as Lk1(Vin-Vo)/(2Lk1+2Lk2). Furthermore, according to KVL, vLo = Vin-Vo-vL2; vT 1 (= vT 2) = -vL2; vLk1 = 2vL2; and vLk2 = Vin-Vo-vL1-vL2 since Do1 and Do2 are conducting. As a result, the following is how vLk1, vLk2, and vLo are derived:

$$v_{Lk1}(t) = \frac{L_{k1}(V_{in}-V_o)}{(L_{k1}+L_{k2})} \quad (10)$$

$$v_{Lk2}(t) = \frac{L_{k2}(V_{in}-V_o)}{(L_{k1}+L_{k2})} \quad (11)$$

$$v_{Lo}(t) = \frac{(L_{k1}+L_{k2})(V_{in}-V_o)}{2(L_{k1}+L_{k2})} \quad (12)$$

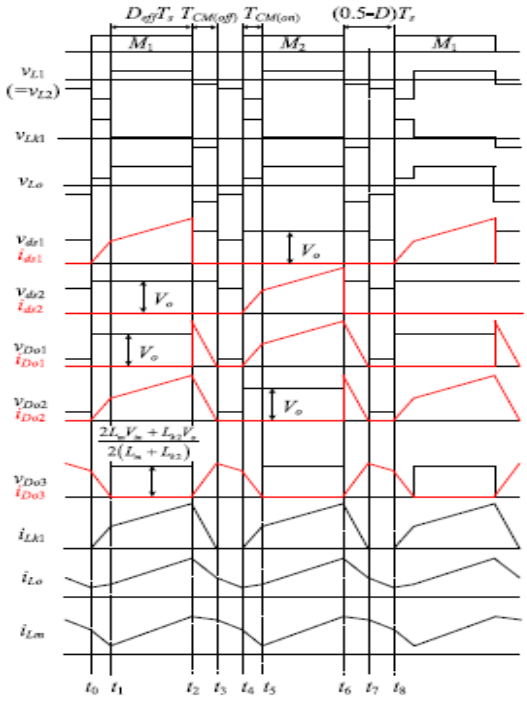


FIGURE 6. The key operation waveforms of the proposed converter.

It is possible to express the currents passing through Lm, Lk1, Lk2, and Lo using the voltages (9) through (12) that were previously determined as follows:

$$i_{Lm}(t) = \frac{L_{k1}(V_{in}-V_o)}{2L_m(L_{k1}+L_{k2})}(t-t2) + i_{Lm}(t2) \quad (13)$$

$$i_{Lk1}(t) = \frac{(V_{in}-V_o)}{(L_{k1}+L_{k2})}(t-t2) + i_{Lk1}(t2) \quad (14)$$

$$i_{Lk2}(t) = \frac{(V_{in}-V_o)}{(L_{k1}+L_{k2})}(t-t2) + i_{Lk2}(t2) \quad (15)$$

$$i_{Lo}(t) = \frac{(L_{k1}+2L_{k2})(V_{in}-V_o)}{2Lo(L_{k1}+L_{k2})}(t-t2) + iLo(t2) \quad (16)$$

Additionally, since in the prior mode iLm = iLk2, iLm(t2) = iLk2(t2). Additionally, Kirchhoff's current law states that iDo3 = iLm-iLk2. (KCL). Consequently, iDo3 steadily rises. Based on (9) and (12). In the meantime, according to (11) iLk1 (= iDo1 = iDo2) steadily declines. The commutation between Do1, Do2, and Do3 so begins. The diode commutation procedure stops and Do1 and Do2 are stopped when iDo1 and iDo2 reach zero. Furthermore, there is no issue with Do1 and Do2's reverse recovery because they are softly switched off. Unlike the typical converter, the suggested converter does not appreciably enhance the output current ripple because of the output inductor Lo, especially in this mode.

**Mode 3 [t3–t4]:** In this mode, iLk1 is zero and the input current passes through Do3, as Do1 and Do2 are blocked. Furthermore, the energy that has been stored in Lm is moved to the output. vL1 (= vL2) can be obtained as follows from Fig. 5(c).

$$V_{L1}(t) = \frac{2L_m(V_{in}-V_o)}{4L_m+L_{k2}} \quad (17)$$

By KVL, vLo = Vin-Vo-vL2 and vLk2 = Vin-Vo-vL1-vL2. Therefore, according to (17), vLk2 and vLo can be expressed as follows V.

$$VLk2(t) = \frac{L_{k2}(V_{in}-V_o)}{4L_m+L_{k2}} \quad (18)$$

$$VLo(t) = \frac{(L_m+L_{k2})(4V_{in}-2V_o)}{4L_m+L_{k2}+L_{k1}} \quad (19)$$

Here is an expression for the current passing through Lm, Lk2, and Lo based on the previously derived (17)–(19):

$$iL_m(t) = \frac{2(V_{in}-V_o)}{4L_m+L_{k2}}(t-t3) + iL_m(t3) \quad (20)$$

$$iL_{k2}(t) = \frac{(V_{in}-V_o)}{4L_m+L_{k2}}(t-t3) + iL_{k2}(t3) \quad (21)$$

$$iLo(t) = \frac{(2L_m+L_{k2})(V_{in}-V_o)}{L_o(4L_m+L_{k2})}(t-t3) + iL_o(t3) \quad (22)$$

Similar to the preceding mode, mode 3 terminates upon turning on M2. iDo3 = iLm-iLk2.

**Mode 4 [t4–t5]:** The transformer conducts current when M2 is activated at t4. As a result, vds1 and vDo2 are clamped to Vlink = Vo and Do1 conducts. vL1 (= vL2) can be obtained as follows from Fig. 5(d)

$$VL_1(t) = \frac{L_{k1}(V_{in}-V_o)-L_{k2}V_o}{2(L_{k1}+L_{k2})} \quad (23)$$

KVL states that vT 1 (= vT 2) = -Vo-vL1, vLk1 = -Vo-vT 1-vT 2, and vLk2 = Vin +vT 2-vL1. vLo = Vin-Vo-vL1. Consequently, the following voltages are across Lk1, Lk2, and Lo.

$$V_{Lk1}(t) = \frac{Lk1Vin}{(L_{k1}+L_{k2})} \quad (24)$$

$$V_{Lk2}(t) = \frac{L_{k2}V_{in}}{(L_{k1}+L_{k2})} \quad (25)$$

$$V_{Lo}(t) = \frac{L_{k1}(V_{in}-V_o)+L_{k2}(2V_{in}-V_o)}{2(L_{k1}+L_{k2})} \quad (26)$$

(**Vin** = 36 V, V**o** = 50 V, P**o** = 750 W).

The currents flowing through Lm, Lk1, Lk2, and Lo are as follows, deduced from previously

(23) – (26):

$$iL_m(t) = \frac{L_{k1}(V_{in}-V_o)-L_{k2}V_o)}{2L_m(L_{k1}+L_{k2})}(t-t3) + \text{iLm(t4)} \quad (27)$$

$$iL_{k1}(t) = \frac{V_{in}}{(L_{k1}+L_{k2})}(t-t4) + iL_{k1}(t4) \quad (28)$$

$$iL_{k2}(t) = \frac{V_{in}}{(L_{k1}+L_{k2})}(t-t4) + il_{k2}(t4) \quad (29)$$

$$i_{Lo}(t) = \frac{L_{k1}(V_{in}-V_o)+L_{k2}(2V_{in}-V_o)}{2L_o(L_{k1}+L_{k2})}(t-t4) + i_{Lo}(t4) \quad (30)$$

According to KCL, iDo1 in this mode equals iLk1, and iDo3 = iLm-iLk2. As a result, the commutation between Do1 and Do3 begins since iDo1 progressively grows and iDo3 gradually drops in accordance with (27), (29), and (30). Furthermore, since iLk1 was zero in the previous mode and ids2 equals iLk1 in this mode. As a result, as illustrated in (28), ids2 progressively rises from zero as a result of Lk1 and Lk2. As a result, M2 can operate through gentle switching, which significantly lowers the turn-on loss. Similar to how M2 functions, M1 can be turned on in mode 8 by using the gentle switching technique. As a result, M1's turn-on loss can be significantly decreased. Additionally, because this mode terminates when iDo3 drops to zero, there Do3 does not have a reverse recovery issue.

A thorough operation analysis is not included here because the operations of modes 5 through 8 are comparable to those of modes 1 through 4. The suggested converter repeats one switching cycle, going from mode 1 to mode 8.

1. ANALYSIS OF THE PROPOSED CONVERTER:

A. VOLTAGE CONVERSION RATIO:

By applying KVL to the outermost loop in Fig. 7, one can determine the voltage conversion ratio of the proposed converter: vDo3 = vLo+Vo-Vin+vL2. The average voltage < vDo3 > of Do3 is as follows since, at steady-state, the average voltage across the resistor is zero

$$\langle V_{Do}3\rangle = V_o - V_{in} \quad (31)$$

Do3 conducts for (1-2D) Ts+2TCM(on) during a single switching cycle, as seen in Fig. 6. Consequently, < vDo3 > is ascertained as follows from (5):

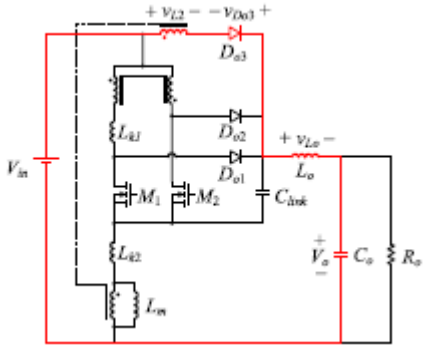


FIGURE 7. The KVL loop of the outermost path in the proposed converter.

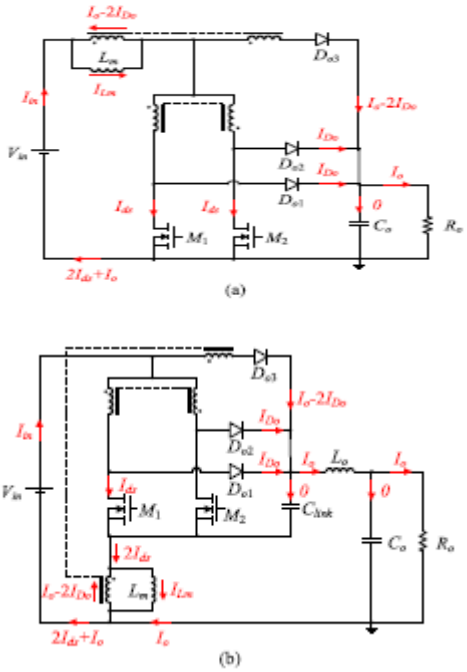


FIGURE 8. The average currents through the circuit components

(a) Conventional converter, (b) Proposed converter.

$$\langle V_{Do}3\rangle = D_{eff}\left\{\frac{2L_mV_{in}+L_{k2}V_o}{L_m+L_{k2}}\right\} \quad (32)$$

The voltage conversion ratio and the effective duty ratio, Deff, can be calculated as follows from equations (31) and (32):

$$D_{eff} = \frac{(L_m+L_{k2})(V_o-V_{in})}{2L_mV_{in}+L_{k2}V_o} \quad (33)$$

$$\frac{V_o}{V_{in}} = \frac{L_m+L_{k2}}{L_m+(1-D_{eff})L_{k2}}\left(1+\frac{2L_mD_{eff}}{L_m+L_{k2}}\right) \quad (34)$$

For comparison, the voltage conversion ratio and effective duty cycle of the conventional converter are the same as those of the proposed converter because they both function in the same way.

B. COMMUTATION TIME:

As Fig. 6 illustrates, during TCM(off), the currents via Do1 and Do2 gradually drop while the current through Do3 steadily increases. Furthermore, during TCM(on), the current passing through Do1 steadily increases while the current passing through Do3 gradually drops.
From Fig. 6's iLk1 waveform, TCM(off) can be expressed as follows.

$$T_{CM(off)} = \frac{i_{Lk1}(t_2)L_{k1}}{V_{Lk1}(t_2-t_3)} \quad (35)$$

where the voltage delivered to Lk1 during mode 2 is denoted by vLk1(t2-t3). For the time interval t1–t2, iLk1 equals ids1, as Fig. 4(a) illustrates. The average current Ids1 passing through M1, assuming an ideal circuit, is 0.5Io(Vo/Vin-1) by KCL.

Furthermore, as illustrated in Fig. 6, ids1(t2) can be obtained as follows, presuming that the average current component of ids1 during TCM(on) is insignificant because TCM(on) is significantly smaller than Deff Ts.

$$i_{ds1}(t_2) = \frac{1}{2Deff}\left(\frac{V_o}{V_{in}}-1\right)I_o + \frac{v_{Lk1}(t1-t2)}{2L_{k1}}D_{eff}T_s. \quad (36)$$

where the voltage delivered to Lk1 during mode 1 is denoted by vLk1(t1-t2). TCM(off) can be ascertained from (35) and (36) since iLk1(t2) = ids1(t2).

$$T_{CM(off)} = \frac{L_{k1}+L_{k2}}{(V_o-V_{in})} \times \left[\frac{1}{2D_{eff}}\left(\frac{V_o}{V_{in}}-1\right)I_o + \frac{(2V_{in}-V_o)D_{eff}T_s}{8L_m+8L_{k2}+2L_{k1}}\right] \quad (37)$$

Furthermore, TCM(on) can be calculated as follows using the iLk1 waveform displayed in Fig. 6.

$$T_{CM(on)} = \frac{-vLK1(t2-t3)T_{CM(off)}-vLK1(t1-t2)D_{eff}T_s}{vLK1(t4-t5)} \quad (38)$$

where the voltage delivered to Lk1 during mode 4 is denoted by vLk1(t4-t5). The following expression for TCM(on) can be derived from (2), (10), and (38):

$$T_{CM(ON)} = \left(\frac{V_o}{V_{in}} - 1\right) T_{CM(off)} - \frac{(L_{k1}+L_{k2})(2V_{in}-V_o)}{(4L_m+4L_{k1}+L_{k2})V_{in}} D_{eff} T_s. \quad (39)$$

For comparison, the TCM(off) and TCM(on) of the two converters are the same when the leakage and magnetizing inductances are the same, as the proposed converter and the conventional converter operate similarly.

**T1** (= N**T2**).

C. PROPOSED CONTROL TECHNIQUES FUZZY LOGIC:

Fuzzy Logic is a form of many-valued logic that allows for reasoning with imprecise or uncertain information, making it especially useful in real-world scenarios where conditions cannot always be classified as simply true or false. Unlike classical binary logic, fuzzy logic assigns truth values anywhere between 0 and 1, enabling the representation of partial truths. This approach reflects the natural ambiguity found in human reasoning and decision-making. At its core lies the **membership function**, which quantifies the degree to which a particular input belongs to a defined set, with values ranging from 0 (non-membership) to 1 (full membership). Fuzzy logic systems rely on **fuzzy rules**—"if-then" statements—that define relationships between input and output variables in a gradual, human-like manner. The result is a **fuzzy set** representing a spectrum of possible output values, each with its associated degree of membership. Because of this flexibility, fuzzy logic has been widely adopted in applications such as control systems, image and natural language processing, medical diagnosis, and artificial intelligence, where crisp, binary decisions are often insufficient.

2. SIMULATION RESULTS:

This section presents the experimental validation of the conventional and proposed converters based on the specifications outlined in Table 1. The key waveforms obtained during testing are illustrated in Figs. 9 and 21. Specifically, Figs. 9(a) and 9(b) highlight the output capacitor current ripple of both converters at an input voltage of 36 V, under varying load conditions. As shown in Fig. 9(a), the proposed converter achieves an output current ripple of just 4.2 A. In contrast, Fig. 9(b) reveals that under a 15 A load, the conventional converter exhibits a ripple of 9.2 A, whereas the proposed design maintains a significantly lower ripple of only 4.21 A. Notably, as the load current increases from 10 A to 15 A, the conventional converter's output current ripple increases by 4.8 A, while the proposed converter sustains an almost constant ripple, highlighting its superior performance. Additionally, Fig. 9(b) shows that the RMS current through the output capacitor in the conventional converter reaches 4.65 Arms at a 15 A load, while the proposed converter achieves a substantially lower RMS current of 1.05 Arms—approximately 4.4 times smaller. This reduced RMS current alleviates stress on the bus capacitor, potentially extending its operational lifespan and making the proposed design more suitable for high-power applications. Fig. 9(c) illustrates the magnetizing current waveforms of the coupled inductors in both converters. The proposed converter demonstrates a peak magnetizing current of 18.5 A, which is 13.5 A lower than the 32 A observed in the conventional converter. As a result, the proposed design can utilize a smaller OD234 magnetic core, unlike the conventional design, which requires a larger OD270 core. Furthermore, Fig. 9(d) shows that the output inductor in the proposed converter carries a peak current of 17.11 A, closely matching the peak current of its coupled inductor, allowing both to share the same OD234 core size. These findings confirm the efficiency, compactness, and improved performance of the proposed converter design over the traditional approach.

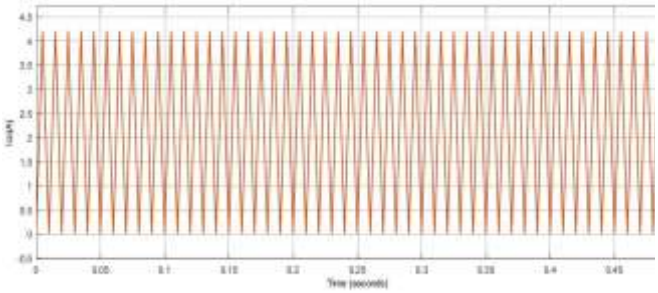
| Parameter | Conventional converter | Proposed converter | Unit |
|---|---|---|---|
| Input voltage $V_{in}$ | 30 - 42 | | V |
| Output voltage $V_o$ | 50 | | V |
| Rated power $P_o$ | 750 | | W |
| Switching frequency $f_{sw}$ | 100 | | kHz |
| Transformer core | PQ2625 | | |
| Number of turns | $N_{T1} = 5$<br>$N_{T2} = 5$ | | |
| Leakage inductance $L_{k1}$ | 0.3 | | uH |
| Coupled inductor core | CH270125 | CH234125 | |
| Number of turns | $N_{L1} = 4$<br>$N_{L2} = 4$ | $N_{L1} = 5$<br>$N_{L2} = 5$ | |
| Magnetizing inductance $L_m$ | 2.7 | 2.73 | uH |
| Leakage inductance $L_{k2}$ | 0.24 | 0.29 | uH |
| Output inductor core | - | CH234125 | |
| Output inductance $L_o$ | - | 5.36 | uH |
| Output capacitor | MKT1820522015 (2.2uF) | | |
| Output capacitance $C_o$ | 24.2 | 6.6 | uF |
| Link capacitor | RA4405K100-FA (4uF) | | |
| Link capacitance $C_{link}$ | - | 8 | uF |

TABLE 1. Parameters used in the experiment.

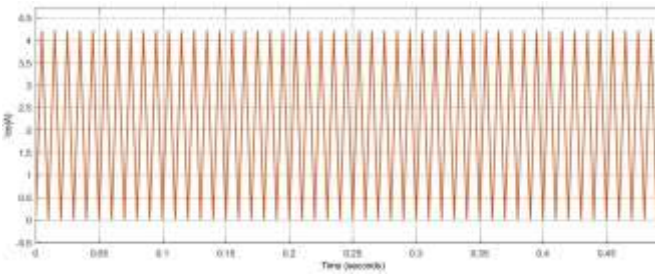
The maximum magnetic flux density (Bmax) values for the magnetic cores used in the converters are as follows: 0.317 T for the coupled inductor in the conventional converter, 0.247 T for the coupled inductor in the proposed converter, and 0.32 T for the output inductor in the proposed converter. These values indicate that, while the conventional converter relies on a single large magnetic core, the proposed converter requires two smaller magnetic cores—for the coupled and output inductors. Additionally, Fig. 9(e) shows the output voltage ripple of both converters at an input voltage of 36 V and a full load of 15 A. Notably, the proposed converter maintains an output voltage ripple of approximately 0.45 V using only two link capacitors (Clink = 8 µF) and three output capacitors (Co = 6.6 µF). In contrast, the conventional converter requires a significantly larger total capacitance—eleven output capacitors totaling 24.2 µF—to achieve a similar ripple level.

Although the proposed converter includes an additional magnetic component (the output inductor), the overall

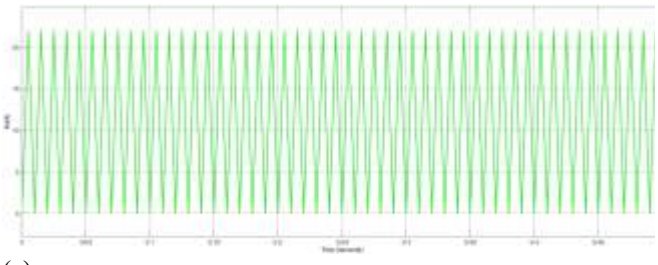
capacitor requirement is drastically reduced compared to the conventional design. Moreover, due to the lower peak magnetizing currents in all inductors of the proposed converter, smaller magnetic cores can be employed. This allows for a significant reduction in both the total volume and weight of the converter. Considering that electrical power systems in geostationary satellites often utilize multiple BDRs in parallel to ensure reliability and high performance [28], the reduced size and weight of the proposed converter make it especially advantageous for such applications, contributing to a more compact and efficient satellite power system.



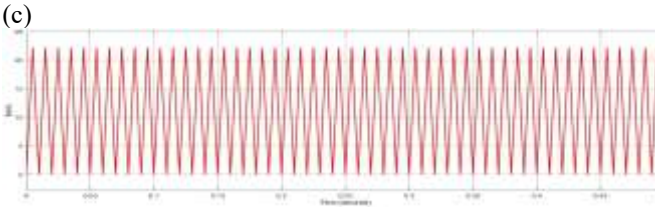
(a)



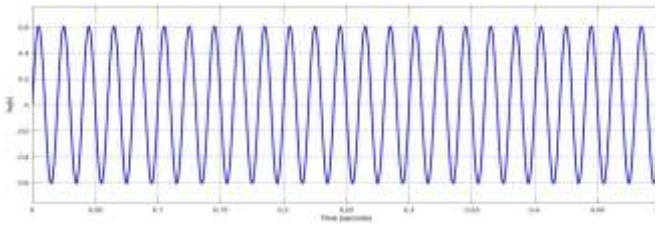
(b)



(c)



(d)



(e)

FIGURE 9. The experimental key waveforms (a) Output capacitor current ripple at 10 A load, (b) Output capacitor current ripple at 15 A load, (c) Magnetizing current of the coupled inductor

## VI. CONCLUSION:

This study presents an improved Weinberg converter that significantly reduces output current ripple and RMS current compared to the conventional design, thanks to the inclusion of an output inductor. As a result, fewer output capacitors are needed to achieve similar voltage ripple, reducing size and component stress. Unlike the traditional converter—where ripple increases with load—the proposed design maintains a nearly constant output ripple across varying loads, making it ideal for high-power applications. Though it introduces an additional magnetic component, the proposed converter operates with a much lower peak magnetizing current, allowing for smaller magnetic cores and avoiding core saturation. A 750 W prototype confirms its high efficiency (≥92.9% across 30 V–42 V inputs) due to soft-switching, optimized magnetic design, and minimal diode losses. Overall, the converter reduces system weight from 404 g to 392 g, and its benefits scale with parallel BDR use, making it suitable for reducing the size, weight, and cost of geostationary satellite power systems.

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