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Mitigation of Critical Delay in Carry Skip Adders Using Finfet 18nm Technology

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Abstract:

The full adder is the basic building block of every arithmetic circuit, and its delay and power decide how fast and how efficiently a processor can compute. As planar CMOS is scaled down, short channel effects and leakage current make it difficult to keep both under control. This paper presents a carry skip adder built from a 10-transistor FinFET full adder cell realised in 18 nm technology. The cell uses XNOR gates and a multiplexer to produce the sum and the carry, so the slow AND-OR-Invert stage normally used for the carry is avoided.

Four such cells are joined with a skip path to form a 4-bit carry skip adder, and a pipelined arrangement is used to shorten the longest carry path. The circuits are designed in Cadence Virtuoso using an 18 nm FinFET design kit, and the adder is also described in Verilog HDL and simulated in the Xilinx Vivado Design Suite for FPGA implementation. Simulation of the 8-bit carry skip adder confirms correct generation of the sum and the carry output. The proposed cell needs fewer transistors than the CMOS, pass-transistor, transmission-gate and GDI full adders reviewed in this paper, which makes it suitable for low power and high speed arithmetic units.

Keywords: *FinFET, Full Adder, Carry Skip Adder, Gate Diffusion Input, Critical Delay, FPGA.*

I . INTRODUCTION

Addition is the most frequently used operation in digital systems. It sits inside arithmetic logic units, multipliers, digital filters and signal processors, so the speed of the adder often sets the clock rate of the whole system. At the same time, many present-day applications are portable and battery operated, which means that low power consumption is just as important as speed.

For decades the answer to these demands was to shrink planar CMOS transistors. At nanometre dimensions, however, short channel effects, leakage current and device variability become serious limits on this approach [8], [12]. The FinFET was introduced to overcome these limits. As shown in Fig. 1, the gate wraps around a thin vertical silicon fin on more than one side, which gives much better control over the channel, lower leakage and better scalability than a planar device [12], [13].

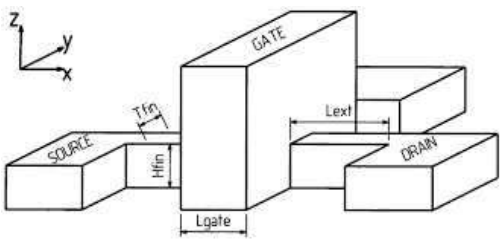


Figure 1: Three-dimensional FinFET structure on silicon-on-insulator substrate

In a ripple carry adder the carry has to travel through every stage, so the delay grows with the word length. A carry skip adder reduces this delay by letting the carry bypass a block of bits whenever all the propagate signals of that block are high. It achieves this with only a small increase in area, and the longest path through the adder, the critical path, becomes much shorter [9], [10].

The objective of this work is to design a carry skip adder around a compact 10-transistor FinFET full adder in 18 nm technology, to reduce the critical delay, and to verify the design by simulation and FPGA implementation. The rest of the paper is organised as follows. Section II reviews related work, Section III describes the proposed method, Section IV presents the simulation results and Section V concludes the paper.

II . LITERATURE REVIEW

A large number of full adder topologies and carry skip adder designs have been reported. The designs that were studied for this work are summarised in Table I and discussed below.

Table I: Summary of full adder designs from the literature

S.No	Method	No. of transistors	Technology	Reference
1	CMOS	28	45 nm	Ibrahim et al. [16], 2011
2	GDI	16	0.18 µm	Agrawal et al. [17], 2010
3	TGL	28	32 nm, 20 nm	Rajesh Babu et al. [7], 2018
4	GDI multiplexer	12	250 nm	Mukherjee et al. [18], 2015
5	FinFET	14	33 nm	Basireddy et al. [19]
6	CMOS & TG	16	90 nm	Bhattacharyya et al. [20], 2015
7	**FinFET GDI (proposed)**	**10**	**18 nm**	**This work**

The conventional CMOS full adder uses 28 transistors arranged as two complementary networks [16]. The large transistor count increases input loading, power consumption and chip area. The four-stage ripple arrangement built from such cells is shown in Fig. 2. Pass-transistor and transmission-gate designs reduce the transistor count, and a hybrid CMOS and transmission-gate cell with 16 transistors has been reported in 90 nm technology [20]. Gate diffusion input (GDI) cells with 16 transistors in 0.18 µm technology [17] and 12 transistors in a multiplexer based form in 250 nm technology [18] reduce the count further. A transmission gate full adder has been implemented with FinFETs at 32 nm and 20 nm [7], and a 14-transistor FinFET cell has been reported at 33 nm [19].

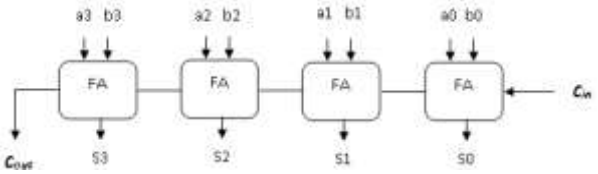


Figure 2: Conventional 4-bit adder

Several carry skip adders have also been proposed. De Rose et al. analysed dynamic carry skip adders based on a Manchester carry chain with domino logic in 45 nm technology, and noted that they need extra input buffers and a complex clock distribution tree [10]. Bahadori et al. presented a high speed, energy efficient carry skip adder that works over a wide range of supply voltages [9]. Lin and Radhakrishnan used OAI logic to generate the propagate and generate signals of a 32-bit carry skip adder in a single stage [11]. Bagyalakshmi and Karpagam proposed a carry skip adder for IoT applications [1], and Tari et al. designed a CNTFET based full adder for carry ripple, carry select and carry skip adders [3].

Other work looked at the full adder cell itself. Radhakrishnan and Themozhi used an XOR-MUX full adder for a wavelet transform on FPGA [4], Kamlapurkar and Lalitha built a 32 nm FinFET based 4-bit ALU, carry save adder and multiplier [2], and Bin Talib et al. studied fault tolerant adders, which need extra circuitry [6]. Canan et al. showed that ambipolar FinFETs can give ultra-compact logic below 10 nm [5].

It can be seen from this survey that most existing designs either use many transistors or depend on extra buffers and complex clocking. This motivates a compact FinFET full adder that avoids the slow AOI stage in the carry path.

III.PROPOSED METHOD

Full adder cell: A full adder has three inputs, a, b and c_{in}, and two outputs, sum and c_{out}. In the proposed cell two XNOR gates in series produce the sum, because the XNOR of an XNOR output with a third input gives a $\oplus$ b $\oplus$ c_{in}. The carry is produced by a 2:1 multiplexer whose select line is driven by the first XNOR gate. When a and b are equal the carry equals a, and otherwise the carry equals c_{in}. Using a multiplexer for the carry removes the AND-OR-Invert logic of the conventional adder and the delay it adds to c_{out}. The gate level model is shown in Fig. 3 and the FinFET implementation in Fig. 4. The complete cell uses only 10 FinFETs.

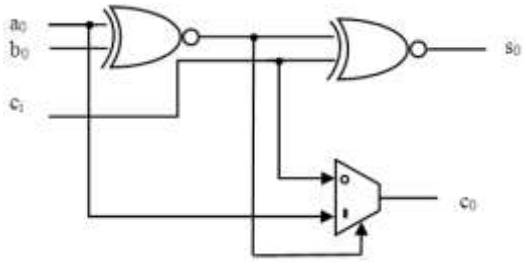
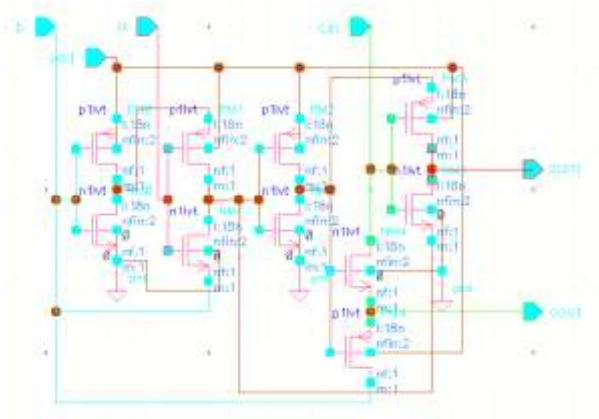
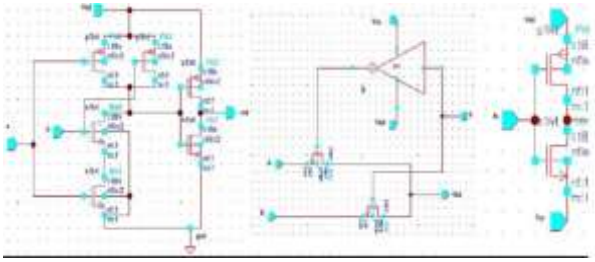


Figure 3: Gate level model of the full adder


Figure 4: Implementation of the full adder using FinFET 18nm technology


Figure 5: Schematic of AND gate and multiplexer using FinFET 18nm technology

Carry skip adder: Four full adder cells are cascaded to form a 4-bit block, as shown in Fig. 6. The propagate signals of the four bits are combined by an AND gate to give a group propagate signal. When this signal is high, the carry entering the block skips the ripple chain and is passed directly to the output through a 2:1 multiplexer. Otherwise the carry produced by the last full adder is selected. The schematic of the 4-bit carry skip adder is given in Fig. 7. A pipelined organisation is also used so that the longest carry path is divided into shorter stages. This is useful in FIR filters, where the full adder is the basic element.

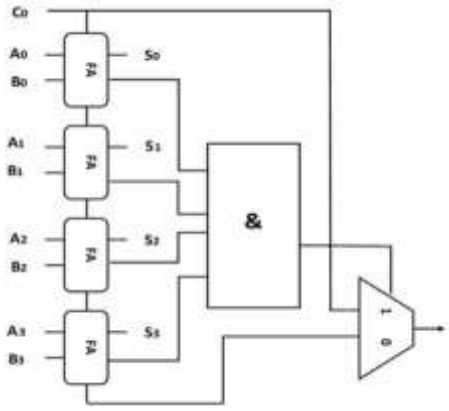


Figure 6: Block diagram of 4-bit carry skip adder

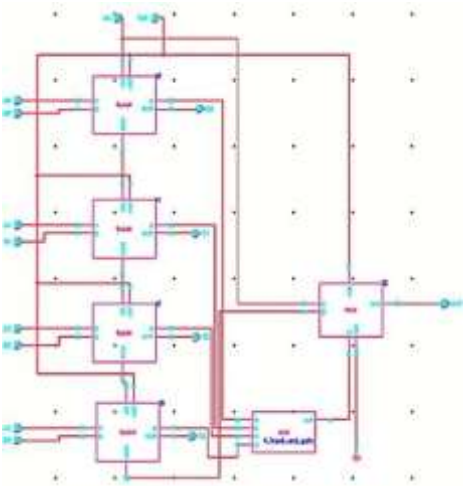


Figure 7: Schematic design of 4-bit carry skip adder

Device sizing: The transistors operate in the weak inversion region, and their dimensions are obtained from the EKV charge-based model [14]. The inversion coefficient, the transconductance and the normalisation current are given by

$$I_C = I_D / I_S \quad (1)$$

$$g_m = (I_D / \eta\varphi_t) \cdot (1 - \exp(-\sqrt{I_C})) / \sqrt{I_C} \quad (2)$$

$$I_S = 2\eta\mu C_{ox}(W/L)\varphi_t^2 \quad (3)$$

where I_D is the drain current, I_S the normalisation current, η the slope factor (taken as 1), μ the carrier mobility, φ_t the thermal voltage (about 26 mV at room temperature) and I_C the inversion coefficient. The oxide capacitance is $C_{ox} = \varepsilon_0\varepsilon_{ox}/t_{ox}$, where ε_0 is the permittivity of free space, ε_{ox} the relative permittivity of the oxide and t_{ox} the oxide thickness. The channel length is chosen by the designer from the design requirements.

Design flow: The design starts with the literature survey and the adder specifications. The HDL, the technology and the topology are then selected, suitable parameter values are derived, and the circuit is designed and simulated. If the specifications are not met, optimisation techniques are applied and the circuit is simulated again; otherwise the design is taken forward to implementation.

IV . SIMULATION RESULTS

The 8-bit carry skip adder was described in Verilog HDL and simulated with the Xilinx Vivado Design Suite, targeting a Xilinx 7-series device. The simulation window is 20 ns long, and the waveform is shown in Fig. 8.

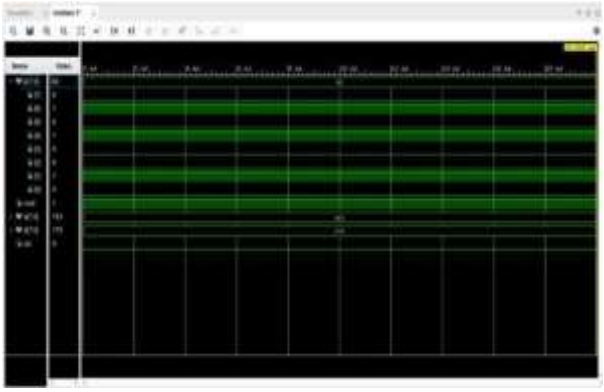


Figure 8: Simulation of 8-bit carry skip adder

Functional Verification: For the test vector shown, input a is 163 (10100011), input b is 175 (10101111) and the carry input is 0. The adder produces the sum s[7:0] = 82 (01010010) and a carry output $c_{out} = 1$. Together the carry and the sum form the 9-bit result 101010010, which is 338 in decimal and equals 163 + 175. The outputs settle to the correct values and stay stable for the rest of the window, so the adder performs the addition correctly.

Transistor Count: As Table I shows, the existing full adders need between 12 and 28 transistors. The proposed FinFET cell needs only 10, which lowers the silicon area and the input loading, and since the carry is taken from a multiplexer, the carry path contains fewer logic levels than in AOI based adders.

FPGA Implementation: The adder is written in Verilog HDL and synthesised in the Vivado Design Suite. Vivado gives a complete platform for design entry, synthesis, simulation and debugging, and the successful synthesis and simulation show that the carry skip adder is suitable for FPGA implementation.

V . CONCLUSION

This paper presented a carry skip adder based on a 10-transistor FinFET full adder in 18 nm technology. The full adder generates the sum with two XNOR gates and the carry with a multiplexer, which removes the AOI stage from the carry path and reduces the critical delay. The cell uses fewer transistors than the CMOS, pass-transistor, transmission-gate and GDI adders reviewed here. Simulation of the 8-bit carry skip adder in Vivado confirmed correct sum and carry generation, and the design is suitable for FPGA implementation. Future work will report post-layout power, delay and area figures, and will study the effect of process variation using Monte Carlo analysis. The adder can then be applied in FIR filters and other arithmetic units where low power and high speed are required.

VI . REFERENCES

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