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Modelling and Simulation of Crisscross Switched Multilevel Inverter Using Cascaded Semi-Half-Bridge Cells

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Abstract: ***A new cascaded multilevel inverter (MLI) is presented. This MLI aims to use a lesser number of switches, achieve better modularity, and reduce voltage stress. The new structure can operate in symmetric and asymmetric modes, producing all odd and even voltage levels. It comprises semi-half-bridge cells connected in series with crisscross switches to generate target voltage levels for synthesizing the sinusoidal output waveform. An extended version of the proposed MLI topology cascades sub-inverters to generate more voltage levels with reduced standing voltage. Compared to the cascading H-bridge topology, the proposed MLI and its extended version use fewer semiconductor switches. The MATLAB R2013b-based simulation results, confirm the efficacy of the proposed MLI topology.***

I. INTRODUCTION

The notion of multilevel power conversion aims to synthesize a stepped waveform from multiple sources to obtain an output voltage closer to a sinusoidal shape. This approach offers several advantages, including the ability to operate at higher power and voltages using fewer series-connected switches, reduced voltage stress, lower electromagnetic interference (EMI), and improved modularity. Major applications of this technology include industrial drives, FACTS devices, electric vehicles, and renewable energy sources [1–5].Cascaded multilevel inverters (MLIs) have three classical topologies: cascaded H-bridge inverters (CHBMLI), MLIs with clamping diodes, and MLIs with flying capacitors [6–10]. The CHBMLI is more reliable for high-voltage applications due to its isolated voltage sources, which are free from voltage-balancing issues. However, the number of components increases as the number of levels increases. In diode-clamped and flying-capacitor inverters, the use of more series-connected clamping diodes and flying capacitors for higher-level operation can cause voltage-balancing problems.

To address these issues, researchers have explored developing either hybrid topologies from the classical benchmarked topologies or novel topologies. Additionally, several novel switching mechanisms have been extended from three-level modulations to MLIs. The focus of research in this area has been on developing novel topologies rather than modulation strategies, with the goal of achieving the desired number of levels using the minimum number of power components.

Among the various topologies, MLIs derived from CHBMLI have attracted significant interest due to their modular structure, ability to operate at higher voltages, and the flexibility to choose different voltage magnitudes for the input sources. Based on the selection of source voltage magnitudes, CHBMLI topologies are further classified into symmetric structures with equal magnitudes and asymmetric structures with unequal source voltage magnitudes. Compared to symmetric topologies, asymmetric topologies can achieve the same number of levels using fewer power components, and they can also reach higher numbers of levels.

Several novel symmetric and asymmetric MLI configurations have been proposed in the literature. These include structures using non-insulated DC sources with fewer switches, series combinations of basic cells and H-bridge inverters, and semi-half-bridge modules with an additional single DC source and an H-bridge inverter. While these topologies offer various advantages, they also introduce increased control circuit cost, complexity, and size due to the larger number of bidirectional switches and gate drivers required.

In recent years, more innovations have emerged in MLI topologies, focusing on the relocation of DC sources, the introduction of modular-based level generation cells, and the reconfiguration of classical topologies with innovative circuits. However, there is still a need for further innovation in the MLI family to address the challenges of extracting sinusoidal voltage/current waveforms using a minimal number of power components. This paper presents the generalized structure of a proposed MLI, along with a multicarrier phase disposition (PD) PWM technique, to generate any desired number of voltage levels.

II.PROPOSED TOPOLOGY

The development of new MLI topology allows sharing the voltage stress among the switches through a series connection of semi-half bridge cells intertwined with crisscross switches. Fig. 1a portrays the general structure of the novel MLI topology constituted by a string of voltage sources (Va1–Van) and (Vb1 – Vbn) connected in crisscross fashion through switches Sc1–Sc2. The switches (Sa1–San) and (Sb1–Sbn) connect the voltage sources in series, while the diodes (Da1–Dan) and (Db1–Dbn) bypass the voltage sources from the load. The switches (S1, S2) complementary to the switches (S′1, S′2) are arranged like H-bridge inverter. In the proposed topology, the required number of levels in the output voltage and the corresponding switches is given by the expression $((4 \times n) + 1)$ and $((2 \times n) + 6)$, respectively, where 'n' is the number of voltage sources per string. Voltage sharing is achieved in every conduction path due to the switching sequence and thus the blocking voltage is reduced. Fig. 1b depicts the structure of a nine-level inverter using four semi-half-bridge cells: two in upper and lower strings, respectively. By connecting only a few basic cells in series, this methodology can generate a minimum step voltage required for any given level. The structure of the DC-link can be obtained from a fixed DC source or from any other renewable energy sources such as solar cells, fuel cells, etc. The level 1 (±Va1) and level 3 (±(Va1 + Va2 + Vb1)) operating modes for each half-cycle with equal voltage sources for symmetrical configuration are illustrated in Figs. 2a and b. In Figs. 2a and b, the switches (Sa1 , Da2 , S′1 , S′2 , Sc2) and (Sa1 , Da2 , Sc1 , S2 , S1), (Sa1 , Sa2 , S′1 , S2 , Sb1 , Db2 , Sc2) and (Sa1 , Sa2 , Sc1 , Sb1 , Db2 , S′2 , S1) are switched to produce (±Va1 and ±(Va1 + Va2 + Vb1)), respectively. The procedure follows a similar switching sequence to extract other voltage levels. The number of switching devices in the conduction path determines the efficiency of the proposed topology. The conventional nine-level CHBMLI topology requires 16 switches and at any point of time, with half of the switches conducting, whereas in the presented topology the number of switches is always less for any level. Table 1 shows the power components comparison of the proposed and classical topologies in terms of 'm', where, 'm' is the number of output levels. The proposed MLI in the asymmetrical configuration is realized by choosing the voltage ratio either in a binary ratio or factor of 2. The structure is shown in Fig. 1b is configured to operate at 15 levels in binary ratio. The number of voltage sources and switches required is four and ten. The corresponding magnitudes of voltage sources are Va1 = Vdc and Va2 = Vb1 = Vb2 = 2 Vdc. The level ±(Va1 + Va2) is observed by switching the devices (Sa1, Sa2, S′1, S′2, Sc2) and (Sa1, Sa2, Sc1, S2, S1). The logical operation tabulated in Table 4 follows a similar pattern as used in symmetrical configuration with seven carriers and two reference signals for positive/negative pulse generation. An extended basic sub-MLI topology in Fig. 3 from proposed MLI of Fig. 1a is composed of three voltage sources (Va1,1, Va2,1and Va3,1) with eight switches. This innovative structure allows producing any possible values of minimum step voltage by using fewer number of basic sub inverter cells. The main advantage of this topology is minimum number of switching devices with reduced blocking voltage for a given number of levels. For the extended topology, the relation between the DC sources (n) and the sub inverters (k) required for any number of levels is shown in Table 2. The proposed topology illustrated in Fig. 1b utilizes PD-PWM for producing nine-level output in symmetrical configuration due to its simplicity. It involves four triangular carriers and two reference signals (sine wave) for PWM generation and the corresponding analog circuitry for base PWM generation for each level as portrayed in Fig. 4. Table 3 details the logical operation for PWM generation to extract various levels of output voltage. Similarly the same concept is extended for asymmetrical configuration.

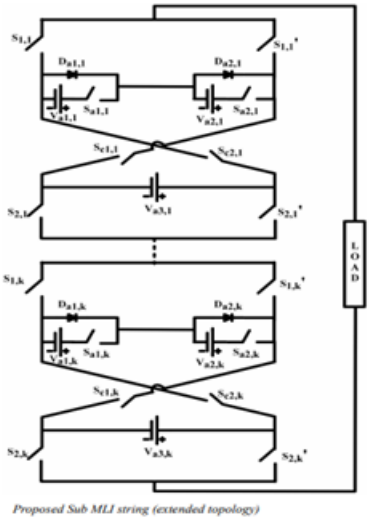

FIG1: PROPOSED MLI TOPOLOGY

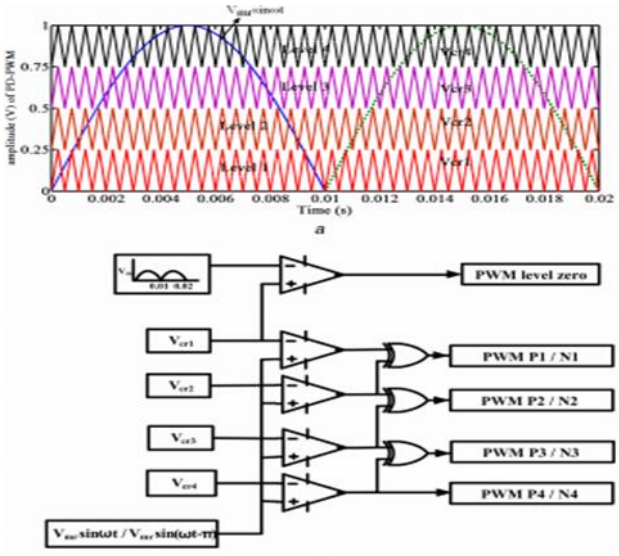

FIG2: Modulation schematic for the 9-level inverter

III. SIMULINK MODEL OF PROPOSED TECHNIQUE:

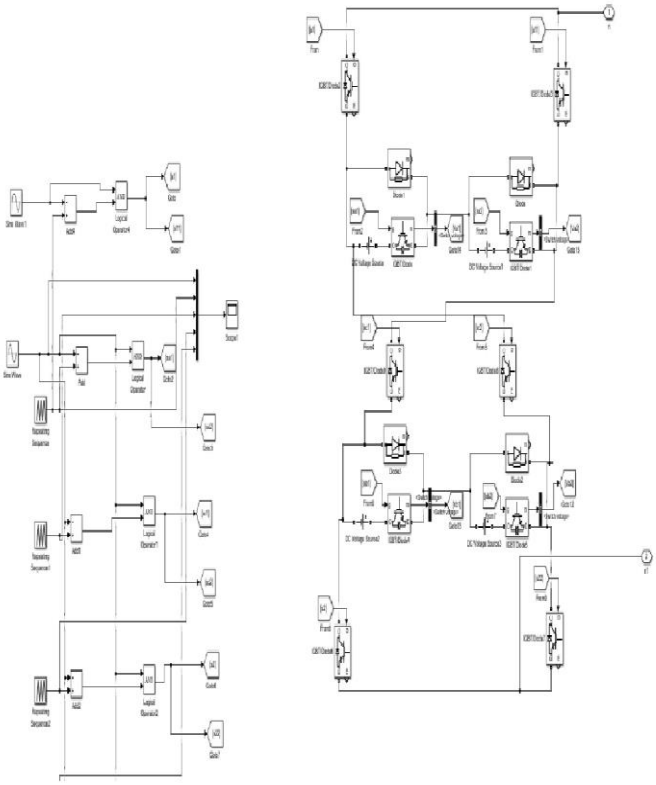

FIG3: SIMULATION BLOCK DIAGRAM

3.1. OUTPUT OF 21 LEVEL:

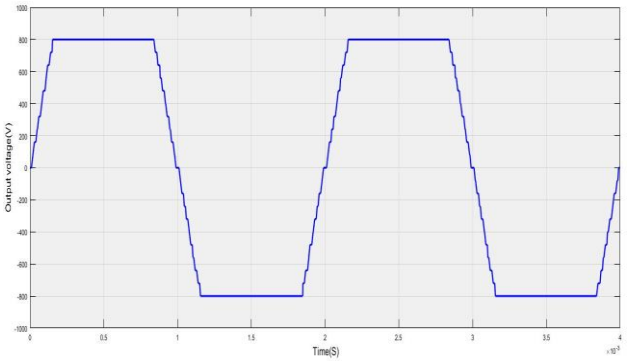

Fig4:-21 level inverter output voltage

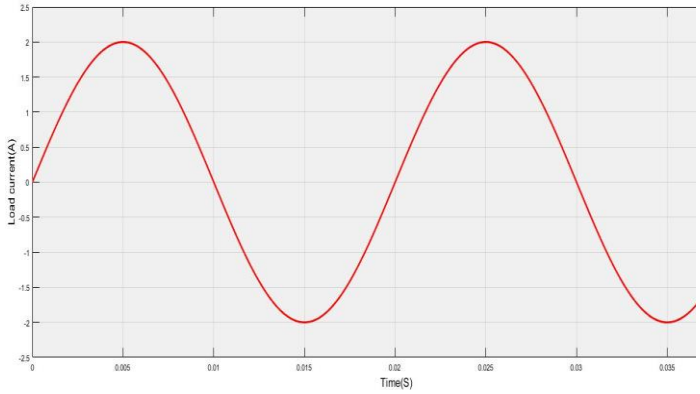

Fig5:-21 level inverter output current

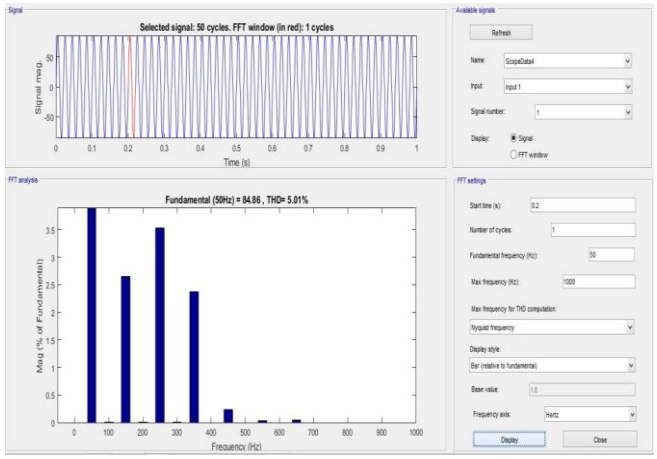

Fig6: Symmetric 21-level inverter Harmonic spectrum

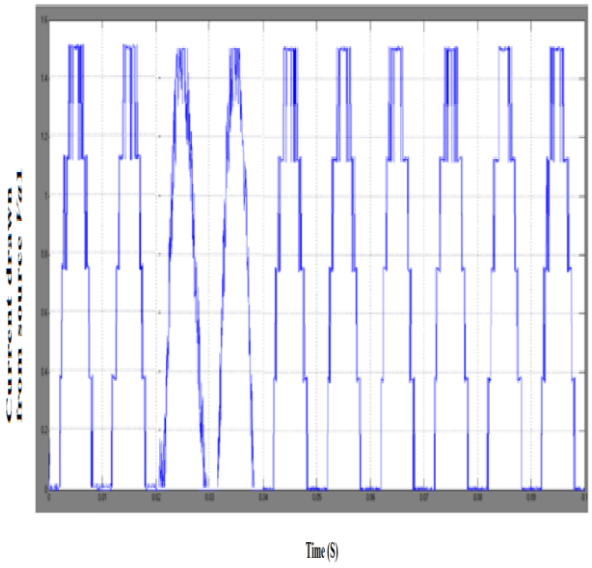

Fig:Current drawn from source *Va*1

CONCLUSION

A new MLI (Multilevel Inverter) topology with symmetric and asymmetric configurations is presented. The modular design allows the topology to achieve any desired voltage level using fewer power components and reduced blocking voltage compared to conventional converters. As a result, the control circuit complexity is lowered, and the derived PWM (Pulse-Width Modulation) scheme utilizing logic gates was easily implemented. The proposed MLI topology was fabricated and tested, with hardware simulation results for 9-level, 13-level, 15-level, and 21-level inverters meeting the target output and validated through simulation. The presented findings demonstrate the practical viability of the proposed MLI topology for renewable energy applications.

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