Modified High Speed 32 Bit Vedic Multiplier Design and Implementation

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Abstract:

Multipliers are essential components in digital signal processing, image processing, and communication systems where high-speed arithmetic operations are required. Conventional multipliers suffer from increased propagation delay and hardware complexity as operand size increases. This paper presents a modified 32-bit Vedic multiplier based on the Urdhva-Tiryakbhyam algorithm of Vedic mathematics. The proposed architecture divides operands into smaller sub-blocks to enable parallel generation of partial products, thereby reducing computation delay. An optimized adder structure is used to combine intermediate results efficiently. The design is implemented using Verilog HDL and simulated using Xilinx tools. Simulation results demonstrate improved speed, reduced delay, and efficient hardware utilization suitable for high-performance VLSI applications.

Keywords — Vedic Multiplier, Urdhva-Tiryakbhyam, VLSI, Verilog HDL, High Speed Multiplier.

I. Introduction:

Multiplication is a fundamental arithmetic operation used extensively in digital signal processing, image processing, communication systems, and microprocessor design. The performance of these systems largely depends on the speed and efficiency of the multiplier unit. As operand size increases, conventional multiplication techniques such as array multipliers and Booth multipliers introduce significant propagation delay and require larger hardware resources. These limitations reduce system performance, particularly in high-speed and low-power VLSI applications.

Vedic mathematics offers efficient algorithms that simplify complex arithmetic operations. Among these techniques, the Urdhva-Tiryakbhyam (vertical and crosswise) method enables parallel generation of partial products, thereby reducing computation time. This paper proposes a modified 32-bit Vedic multiplier that uses hierarchical decomposition of operands into smaller modules. The proposed architecture improves speed by reducing critical path delay and enhancing parallelism. The design is implemented using Verilog HDL and evaluated using simulation tools to verify functional correctness and performance improvements. The proposed system demonstrates better efficiency compared to conventional multiplier architectures in terms of delay and hardware utilization.

II. Proposed System

The proposed system implements a 32-bit Vedic multiplier using a hierarchical and modular architecture. The multiplier is constructed using smaller multiplier blocks such as 4-bit, 8-bit, and 16-bit modules. These smaller modules operate simultaneously to generate partial products. The outputs of these modules are combined using optimized adder structures to produce the final multiplication result.

The hierarchical design reduces design complexity and improves scalability. Parallel processing of partial products minimizes propagation delay and increases computational speed. Additionally, the architecture incorporates efficient carry propagation mechanisms to reduce overall latency. The modular structure also allows easy extension of the design for higher bit-width multipliers. This approach enhances performance and ensures efficient utilization of hardware resources in VLSI implementations.

III. Design Methodology

The proposed system implements a high-speed 32-bit Vedic multiplier based on the Urdhva Tiryakbhyam algorithm. The design follows a modular and hierarchical approach to improve computational speed and reduce propagation delay. Two 32-bit input operands are divided into smaller segments to enable parallel processing. Using vertical and crosswise multiplication, partial products are generated simultaneously, which reduces computation time compared to conventional multiplier architectures. This parallel generation of partial products forms the basis of the proposed high-speed multiplier design.

The generated partial products are accumulated using a Carry Save Adder (CSA) network, which reduces carry propagation delay by producing intermediate sum and carry outputs. These outputs are then processed by a Kogge Stone Adder (KSA), which performs fast parallel carry computation to obtain the final result. The integration of CSA and KSA enhances the speed and efficiency of the multiplier. The complete architecture is implemented using Verilog HDL and verified through simulation to ensure correct functionality and improved performance.

IV. Operation

The proposed 32-bit Vedic multiplier operates based on the Urdhva Tiryakbhyam algorithm combined with optimized adder structures. Initially, two 32-bit binary inputs are provided to the multiplier. These inputs are decomposed into smaller segments to enable parallel generation of partial products. Using the vertical and crosswise multiplication technique, multiple partial products are generated simultaneously, which reduces computation time.

The generated partial products are then forwarded to the Carry Save Adder (CSA) network. The CSA accumulates multiple operands without immediate carry propagation, producing intermediate sum and carry outputs. This approach significantly minimizes propagation delay during intermediate addition stages.

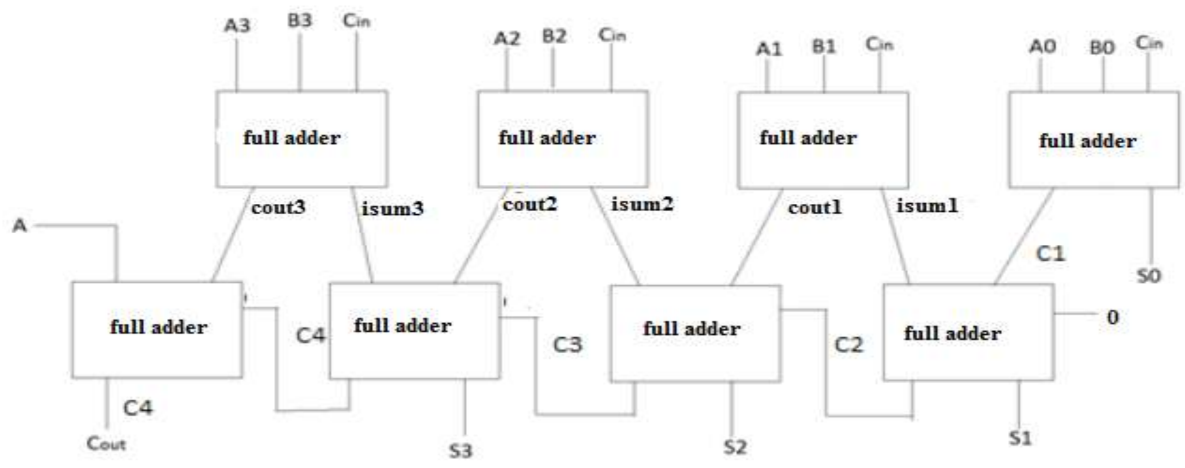

Fig6: 4bit carry save adder

The intermediate outputs from the CSA are then processed by the Kogge Stone Adder (KSA). The KSA performs parallel prefix carry computation, enabling fast final addition. This stage generates the final multiplication result efficiently with reduced delay.

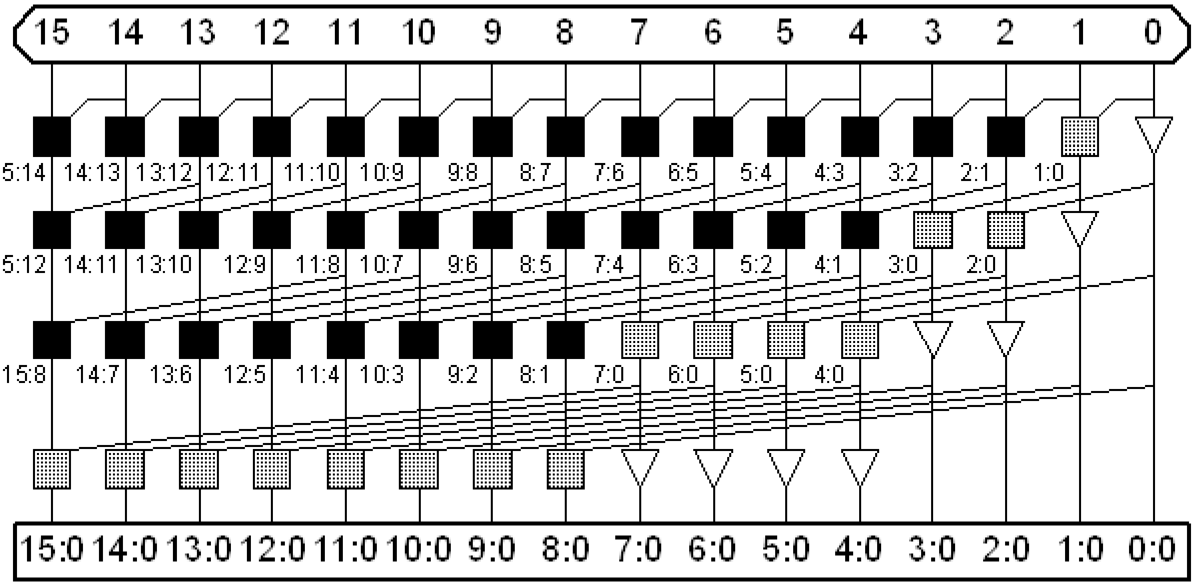

Fig : 16 bit kogge stone adder

Finally, the output generation unit produces a 64-bit result corresponding to the multiplication of two 32-bit inputs. The overall operation ensures high-speed computation, reduced propagation delay, and improved performance compared to conventional multiplier architectures.

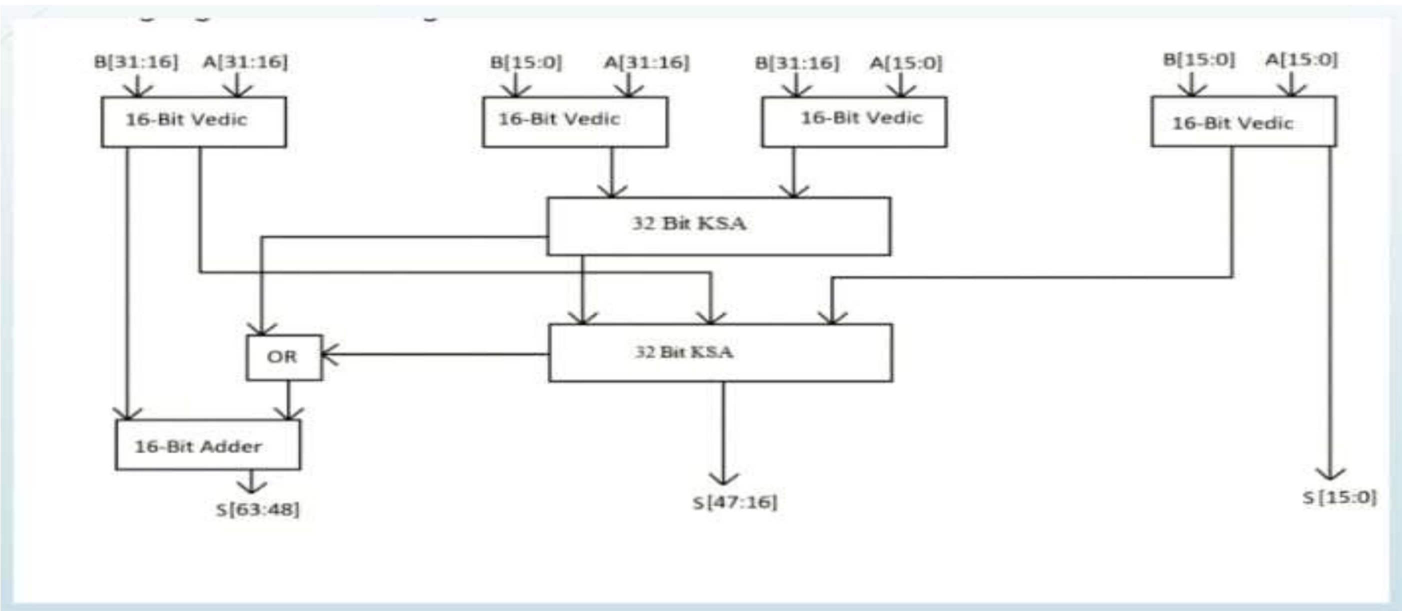

Fig: 32 Bit vedic multiplier using KSA

V. Tools and Technologies Used

- Verilog HDL
- Xilinx Vivado
- FPGA-based simulation environment
- VLSI design methodology

These tools are used for implementation, simulation, and verification of the proposed multiplier design.

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VI. Implementation

The implementation of the proposed 32-bit Vedic multiplier is carried out using Verilog HDL. Initially, small multiplier modules are developed and tested individually. These modules are integrated hierarchically to construct the complete multiplier architecture. The design is simulated using Xilinx tools to verify functionality.

After simulation, synthesis is performed to analyze delay and hardware utilization. The modular implementation simplifies debugging and improves scalability. The design is tested with multiple input combinations to ensure correctness. The implementation demonstrates improved speed and reduced propagation delay compared to conventional multiplier designs.

VII. Testing and Validation

Testing is performed by applying various input combinations to verify functional correctness. Simulation waveforms are analyzed to confirm accurate multiplication results. The delay and performance parameters are measured using synthesis reports. The proposed multiplier is compared with conventional multiplier designs to evaluate performance improvements.

The validation process confirms that the hierarchical Vedic multiplier reduces computation time due to parallel processing. The design also shows improved hardware utilization. These results demonstrate the effectiveness of the proposed architecture for high-speed applications.

VIII. Results and Discussion

Simulation results indicate that the modified Vedic multiplier provides faster computation compared to conventional multiplier architectures. The use of parallel processing reduces propagation delay. The hierarchical structure improves scalability for larger bit-width operations. Efficient adder structures minimize carry propagation delay, enhancing overall performance.

The synthesis results show improved speed and reduced hardware complexity. The architecture demonstrates efficient utilization of logic resources. These improvements make the proposed multiplier suitable for digital signal processing and other high-speed VLSI applications.

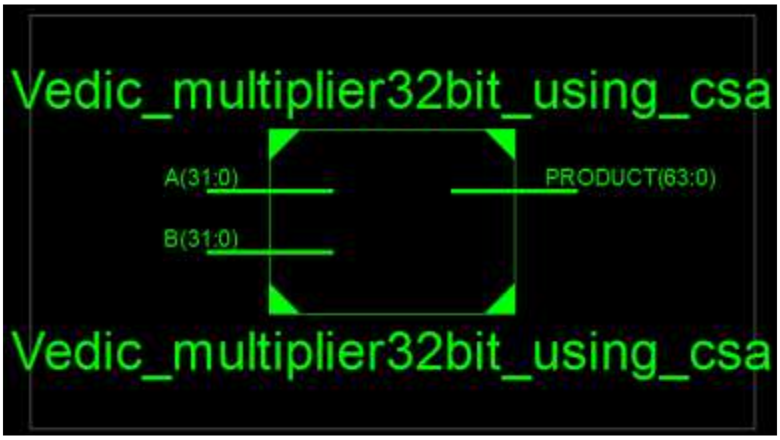

Fig: RTL Schematic of vedic multiplier using CARRY SAVE ADDER

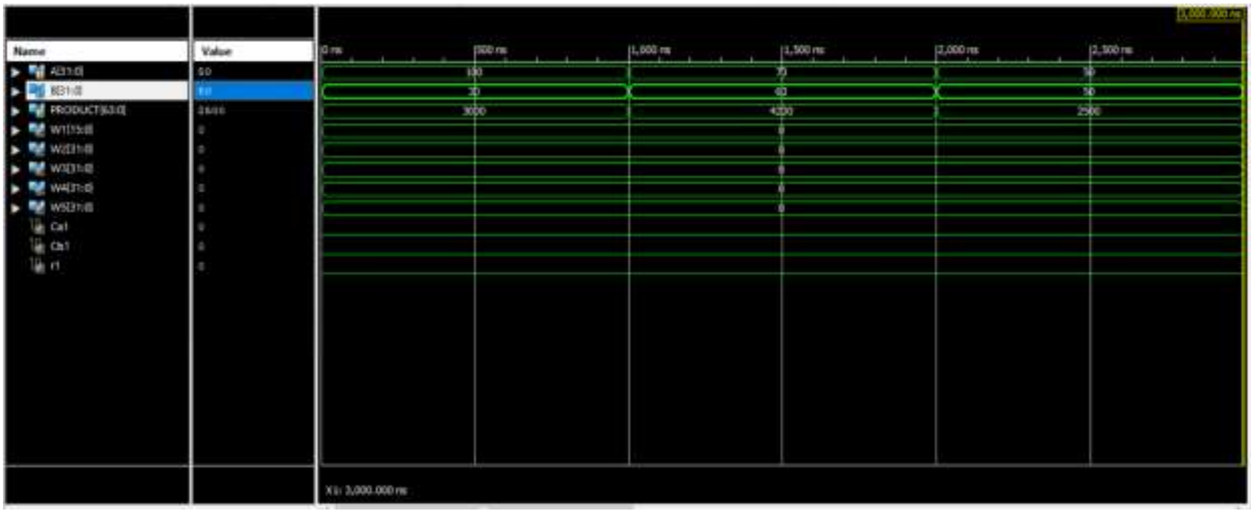

Fig :Simulated Waveforms of vedic multiplier using carry save adder

IX. Conclusion

A modified 32-bit Vedic multiplier based on the Urdhva-Tiryakbhyam technique is presented in this paper. The proposed architecture improves speed through parallel generation of partial products and efficient addition. The hierarchical design reduces propagation delay and enhances scalability. The implementation using Verilog HDL and simulation results confirm improved performance. The proposed multiplier is suitable for high-speed and low-delay VLSI applications.

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