International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 06 Issue: 08 | August - 2022 Impact Factor: 7.185 ISSN: 2582-3930

MODIFIED HIGH SPEED AND LOW POWER 32-BIT VEDIC MULTIPLIER DESIGN AND IMPLEMENTATION

Mrs. CH. Manjusha[1], V. Saideepika[2], R. Lakshmi Surekha[2], V. Yamini[2],N. Revathi[2],

[1]Associate Professor, Department of ECE, Narayana Engineering College, Gudur, AP, 524101.
[2]UG Student, Department of ECE, Narayana Engineering College, Gudur, AP,524101.

[1]manjusha.chinta1@gmail.com, [2]vadhisaideepika@gmail.com

Abstract –The multiplier speed is a significant feature as the multiplier forms an important part of many systems like FIR filters, microprocessors, DSPs etc. The multiplier is slow as compared to other parts of the system hence it is the speed determining factor of the system. An improvement in speed of the multiplier leads to an improvement in speed of the overall speed. The multiplier speed not only depends on the multiplication technique used it is also depends on the type of adder employed for the addition of the partial products. The proposedhigh speed and low power 32-bit Vedic multiplier architectures based on Vedic sutra namely, Urdhva-Triyag using Carry Save Adder(CSA) has been implemented.Among various methods of multiplication, recently Vedic multipliers are being more efficient. These sutras meant for fastercalculation.Urdhva-Triyag is more efficient than other multipliers with respect to speed. The most significant aspect of the Urdhva-Triyag sutra is, the developed multiplier generates allpartial products in one step. High speed adders are used in the architecture instead of conventional Ripple carry adders thereby reducing the delay further.Finally, the results are comparedwith conventional multipliers to show the efficiency in terms of speed.The effectiveness of theproposed method is synthesized and simulated using Xilinx tool using Verilog coding

Software Tools:

- Xilinx ISE 14.7 Tool

Key Words:Vedic Multiplier, Urdhva-Triyagbhyam sutra, Ripple Carry Adder,Carry Save Adder.

1.INTRODUCTION

Multiplier is a major block in designing the digital systems and it plays an important role in digital signal processing and various other applications. The demand of high-speed processing and low power consumption multipliers are increasing day-by-day in digital signal processing and high-speed general purpose processor design.

Two most common multiplication algorithms followed in the digital hardware are array multiplication algorithm and booth multiplication algorithm. Power consumption and delay is more in Array Multiplier and also booth multiplier consumes large power. The mathematical operations using Vedic method are very fast and requires less hardware, this can be used to improve the computational speed of processors. Veda means “knowledge”. Hence Vedic math has a much ancient origin though attributed to the techniques. Main algorithm of Vedic multiplication is Urdhva Triyakbhyam. The multiplication of two operands using Vedic Multiplier is achieved by multiplication by vertically and crosswise and then adding all the results.By usingVedic multiplier the delay, area and power will be efficient.

2.AIM AND OBJECTIVE

The aim of this project is to increase the speed ofmultipliers, reduce the delay of multiplications in systems and reduce the use of power consumption by designing and implementing the modified high speed and low power 32-bit Vedic Multiplier by using carry save adder.

The objective of the implementation is to optimize the performance parameters such as area, delay and power for the 32-bit Vedic Multiplier implementation using carry save adder.

3.LITERATURE SURVEY

“Implementation of an Efficient Multiplier based on Vedic Mathematics Using EDA Tool”, International Journal of Engineering and Advance Technology, Vol.1, no. 5, June, 2012. In this project an optimized area efficient multiplier is designed. This paper deals with design and implementation of efficient high speed 16x16 multiplier using various algorithms like array & booth, and using Vedic operators. Multipliers are compared on the basis of optimized area, speed and memory required. Multipliers are designed with optimized speed and area. Pushpalata Verma, K. K. Mehta,

“Area Efficient Low Power Vedic Multiplier Design Using GDI Technique.” international journal of engineering trends and technology 15 (2014): 196-199. In this paper, transistor level implementation of a Vedic multiplier based on a Vedic sutra, Urdhva Tiryakbhyam, is proposed. Higher order compressors are used in partial product addition stage to get the final result. A power efficient technique, Gate Diffusion input, has been used to design all the leaf cells of the multiplier. Pokhriyal, Nidhi and Neelam Rup Prakash.

"Design and implementation of 8-bit vedic multiplier using mGDI technique," 2017 International Conference on Advances in Computing, Communications and Informatics (ICACCI), 2017, pp. 1923-1927. 8-bit Vedic multiplier is designed using Urdhva Tiryagbhyam sutra with 4 numbers of

4-bit Vedic multiplier and 3 adder circuits. S. S. Meti, C. N. Bharath, Y. G. Praveen Kumar and B. S. Kariyappa.

4. VEDIC MATHEMATICS

Vedic mathematics is a part of four Vedas.The description of severalmathematical terms containing arithmetic, geometric, factorization, trigonometric, quadraticequations, and calculus is given by Vedic Maths.Vedic mathematics manages couple of fundamental and complex numerical tasks. "Vedic" hasbeen gotten from "Veda" which means the storage facility of all learning.

4.1. Urdhva-Triyagbyam sutra

The uniqueness of Vedic mathematics is that it eliminates the lengthy and very simple equations using Urdhva-Triyagbhyam (Vertically and Crosswise) Sutra one of 16 Vedic Triyagbhyam means bothvertically and crosswise.This sutra is a powerful way to multiply and results in a faster multiplication by partialgeneration of the product and a summing up in a single iterative step. This sutra has theadvantage of saving considerable time and effort to solve the problem.

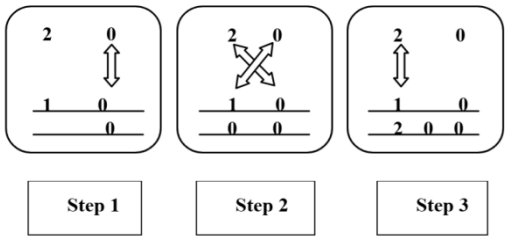

Figure 1: Urdhva-Triyag sutra

This sutra is a powerful way to multiply and results in a faster multiplication by partialgeneration of the product and a summing up in a single iterative step. This sutra has theadvantage of saving considerable time and effort to solve the problem.

5. CARRY SAVE ADDER

Carry Save Adder is also one kind of parallel RCA but it does not calculate the carrythrough the stages rather it stores the carry or save it and later it calculates. Suppose we haveto calculate A, B, C. So Carry Save Adder splits it into A+B+C= S+C. CSA has n numberof full adder which perform the single summation and generates the carry individually. Entire sum can be calculated after we shifted the carry by the left side. The main application ofcarry save algorithm is, well known for multiplier architecture.

5.1. 4-bit Carry Save Adder

Carry Save Adder doesn't transfer the intermediate carries to the next stages, but insteadsaves the carry and addends to the sum of next stage using another full adder. This methodof adding up bits, generally are 3 binary numbers of 4 bits, the time delay of the circuit. Thestage of the addition part includes saving the carries and sum bits and transferring to thestage 2. The stage 2 acts similar to RCA where the stored carry and sum bits are added. Thecircuit diagram of the Carry Save adder is as shown in figure.

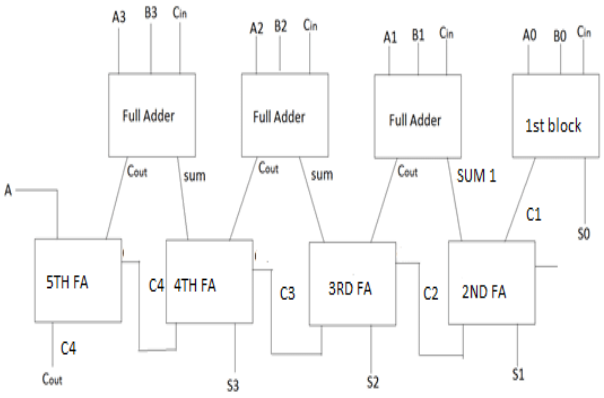

Figure 2: 4-bit Carry Save Adder

The operands used here are three i.e., A, B and Cin where Cin is a 4-bit input carry. Fourfull adders are used for four each bits of A, B and Cin. The sum and carry bits are generatedfor every full adder. The carry bits are not sent to the next full adder but instead, they aresaved and added up to the next sum term using a ripple carry adder.

*Advantages of CSA:*In carry save adder we can operate on 3 different numbers at a time.The carry is not propagated through the stages. Instead, carry is stored in present stage,and updated as addend value in the next stage.For the next level where the final operation is done, use a simple N-bit Ripple CarryAdder.The delay is O (log N) for the tree CSA.

6.EXISTING METHOD

There are many existing methods for design of Vedic Multipliers. The design of Vedic multiplier using Ripple Carry Adder (RCA) is a dependent process because using RCA the full adders in a multiplier arranged in a manner to give a result of an addition operation of n-bit binary sequence. The input of one full adder is depending on output of second full adder and it repeats until it reaches to the last full adder, it leads to increasing of delay and power consumption.

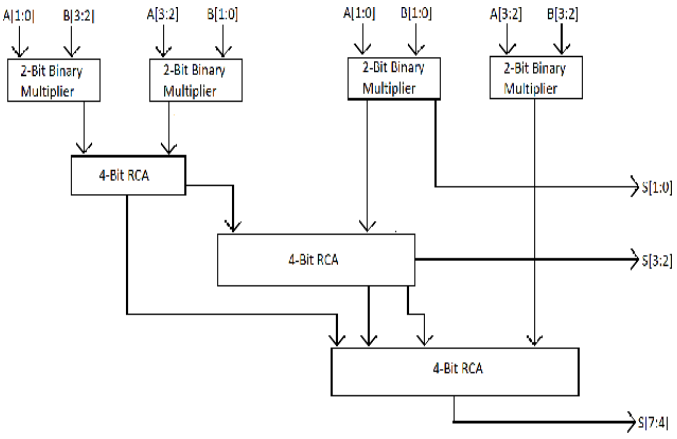

Figure 3: 4-bit Vedic Multiplier

The sutra used by this Vedic Multiplier using RCA is Urdhva-Triyakbhyam which means vertically and cross-wise. The 2 inputs bits are separated into 2 similar parts the vertical and cross-product calculations can be done. Two adders are used

in the design of intermediate stages of the addition. The output carry Cout from these two adders is given as input to another RCA. For 32-bit Vedic Multiplier the outputs of parallel adders are given to OR gate and of the size of last RCA is reduced to half.

*Disadvantages:*Area is increased and hardware complexity increasesas number of computations increases.Computational delay is high and performance of the design is low.

7. PROPOSED METHOD

In the proposed method, the two parallel adders are replaced by Carry Save Adder for the better execution of the multiplier architecture. The carry save adder seems to be the most useful adder for our application. it is simply a parallel ensemble of k full-adders without any horizontal connection.There have been many existing binary multipliers which are efficient. The currentpaper specifies a modification in binary Vedic multiplication technique.

A binary multiplier can be used in digital electronics as a electronic circuit, such as incomputers to find the product of two binary numbers. Carbon-copy of normal multiplicationtechnique is used by binary multiplier, the multiplicand is multiplied with each bit of themultiplier beginning from the least significant bit. Two half adder (HA) modules can be usedin order to implement a 2-bit binary multiplier. A no of computer arithmetic calculations canbe used to appliance digital multiplier. Among these techniques many imply computing a setof partial products, and then summing the generated partial products together.

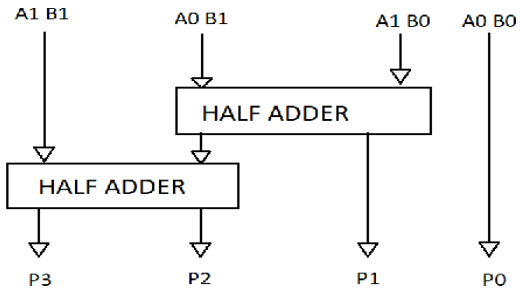

Figure 4: 2 x 2 Binary counter

7.1.Proposed Algorithm

In the proposed paper, the two parallel adders are replaced by Carry Save Adder for the better executionof the multiplier architecture. The recommended modified Vedic multiplicationmethodologyis done in the following for 4-bit inputs, A (A3 -A0) and B (B3 -B0) and 8-bit output S (S7-S0)

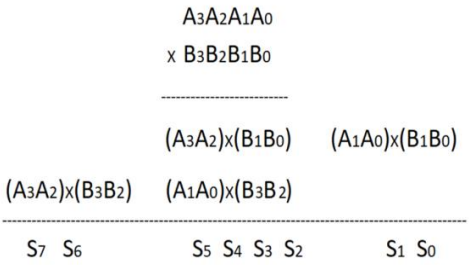

Figure 5: Modified 4-bit Vedic multiplier algorithm

(A3A2) (B3B2) using 2-bit multiplier generates result: S33S32S31S30,(A3A2) (B1B0) using 2-bit multiplier generates result: S23S22S21S20, (A1A0) (B3B2) using 2-bit multiplier generates result: S13S12S11S10, (A1A0) (B1B0) using 2-bit multiplier generates result: S03S02S01S00

7.2. Modified 4-bit Vedic multiplier

The 4-bit CSA Carry Save Adder is used to add three 4-bit data inputs: S23S22S21S20,S13S12S11S10 and S31S30 S03 S02. The proposed 4 bit modified Vedic multiplier is designedand the above Fig shows it. The last two MSBs of CSA outputs are given as inputs to ORgate. In addition, the last stage 4-bit RCA is replaced by 2-bit adder circuit through which the output value of OR gate can be controlled. One of the inputs to last stage 2-bit adder isobtaining from the output of or gate. Similarly, a 4-bit RCA block is a must needed for 8-bitvedic multiplication design.

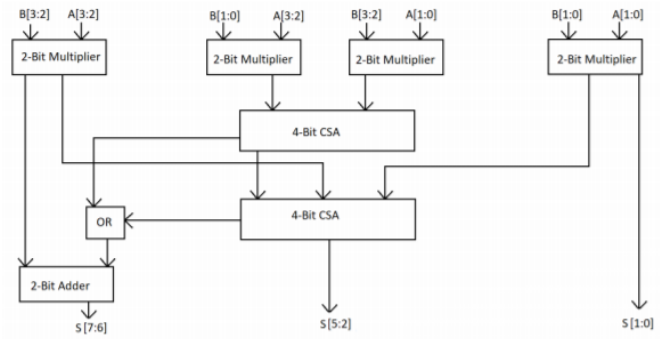

Figure 6: Modified 4-bit Vedic multiplier

7.2. Proposed 32-bit Vedic multiplier

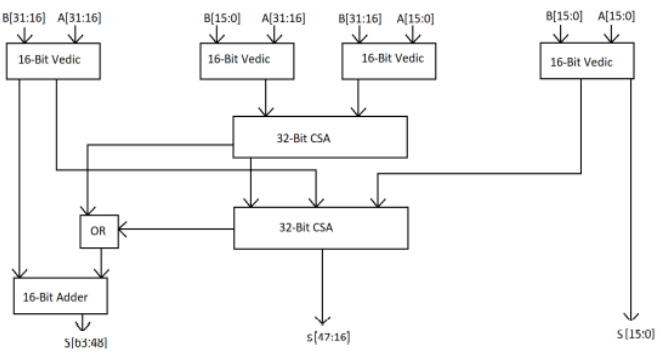

Figure 7: Proposed 32-bit Vedic multiplier

7.3.Methodology

First, a 4-bit Vedic multiplier is designed and in the same manner the size of Vedic multiplier is increased up to 32 bit ie, 8-bit, 16-bit, and then 32-bit using RCA and then by using CSA, the modified 4-bit Vedic multiplier is implemented and in the same way the size of the modified vedic multiplier is increased upto 32-bit i.e, 8, 16, and 32 bit. The final synthesis is done by using XILINX ISE 14.7 DESIGN SUITE. 8.SIMULATION RESULTS AND DISCUSSION

8. SIMULATION AND RESULTS

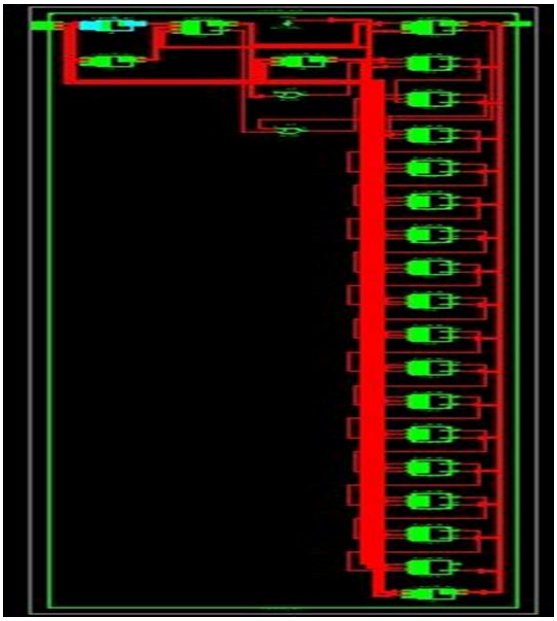

Figure 8: RTL Schematic of proposed 32-bit Vedic multiplier

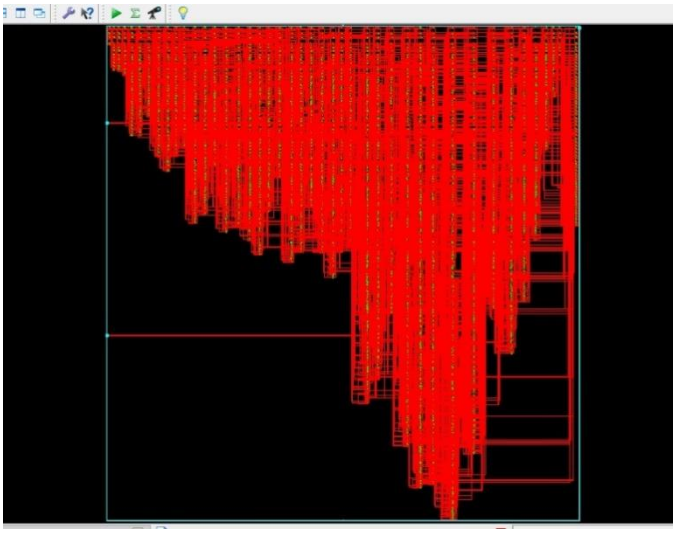

Figure 9: Technology Schematic of Proposed 32-bit Vedic multiplier

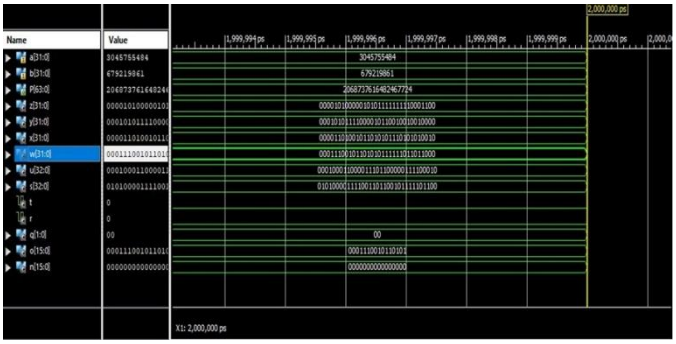

Figure 10: Simulation results of proposed 32-bit Vedic multiplier

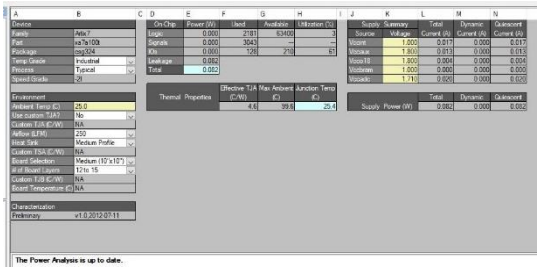

Figure 12: Power Analysis of Proposed 32-bit Vedic multiplier

S. NO	METHOS	DELAY (in ns)	LUT's
1.	16-bit Vedic Multiplier using Ripple Carry Adder [1]	38.040ns	429 out of 4656
2.	16-bit Vedic Multiplier using Carry Select Adder [1]	35.353ns	409 out of 4656
3.	16-bit Vedic Multiplier using Carry Save Adder [2]	20.355ns	708 out of 63400
4.	Proposed 32-bit Vedic multiplier using Carry Save Adder	38.272ns	2979 out of 63400

Table 1: Comparison of delay and area with existing methods

9. CONCLUSIONS

This paper introducethe systematic method for binary multiplier circuits which is based on Vedic mathematics. When it comes to the terms of time delay then the proposed system is more efficient than existing methods. Elongation for a higher bit size can be done with help of proposed technique. Moreover, adders of different architectures can be used in the CSA Carry Save Adder design used in the proposed modified Vedic multiplier. Among many techniques modified architecture is used to increase and speed up the multiplication. In this technique hike in area occurred it is a drawback.

FUTURE SCOPE

In the future the proposed design can be modified in such a way that vedic multiplier can be enhanced by trading off between area and delay or addition operation can be implemented by delay efficient structure and the instructions can be changed such that logical operations can be performed by making modifications in the instruction set.

REFERENCES

[1] Journals: International Journal of Software & Hardware Research in Engineering ISSN-2347-4890 Volume 3 Issue 12 December, 2015 © 2015, I Journals All Rights Reserved www.ijournals.in Page 28 Implementation and Analysis of Vedic Multiplier Using Different Adder. Authors:- Ankita Jain; Atush Jain.

[2] S. Nagaraj, k. Venkataramana Reddy and P. Anil Kumar3i; Analysis of Vedic Multiplier for Conventional CMOS & Complementary Pass Transistor(CPL) Logics SCOPUS Indexed Springer 8th International Conference on Innovations in Electronics and Communication Engineering, (ICIECE)

[3] S. Akhter, "VHDL implementation of fast N x N multiplier based on Vedic mathematics," in Proc. 18th European Conference on Circuit Theory and Design, 2007, pp. 472-475

[4] M.Pushpa, S. Nagaraj, Design and Analysis of 8-bit Array, Carry Save Array, Braun,Wallace Tree and Vedic Multipliers, IEEE Sponsored International Conference On New Trends In Engineering & Technology(ICNTET 2018).

[5] Nagaraj, S; Thyagarajan, K; Srihari, D; Gopi, K; Design and Analysis of Wallace Tree Multiplier for CMOS and CPL Logic2018 International Conference on Computation of Power, Energy, Information and Communication (ICCPEIC)006-0102018IEEE

[6] Josmin Thomas; R. Pushpangadan; S Jinesh Comparative study of performance Vedic multiplier on the Basis of Adders used 2015 IEEE International WIE Conference on Electrical and Computer Engineering (WIECON-ECE) [6] S. Nagaraj, Dr.G.M. Sreerama Reddy and Dr.S. Aruna Mastani; A Survey on Adiabatic Logic International Conference on Communications, Signal Processing and VLSI(IC2SV2019), Springer Conference, National Institute of Technology, Warangal.

[7] S. Nagaraj, K. Venkataramana Reddy and and P.Anil Kumar3i;Analysis of Vedic Multiplier for Conventional CMOS & Complementary Pass Transistor Logic(CPL) Logics SCOPUS Indexed Springer 8th International Conference on Innovations in Electronics and Communication Engineering, (ICIECE-2019) .

[8] Ramesh Pushpangadana, Vineeth Sukumarana, Rino Innocenta, Dinesh Sasikumara & Vaisak Sundara, "High Speed Vedic Multiplier for Digital Signal Processors",IETE JOURNAL OF RESEARCH , Vol 55, ISSUE 6 , NOV-DEC 2009

[9] Nagaraj, S; Reddy, R Mallikarjuna; FPGA Implementation of Modified Booth Multiplier, International Journal of Engineering Research and Applications (IJERA),ISSN: 2248-9622 , Vol. 3, Issue 2, 2013

[10] Sridhar, K; Nagaraj, S; Tech, M; High Speed IEEE-754 Double Precision Floating Point Adder/Subtractor and Multiplier Using Verilog,International Journal and magazine of Engineering, Technology, Management and Research ,ISSN NO.: 2348 -4845 ,Volume 2, Issue 4, 2015

[11] T Prathyusha, P Madhuri, D Pavan Kalyan, R Abhishek, & P Rajasekar(2021), " Implementation Of Efficient Code Convertors Using Reversible Logic Gates" Dogo Rangsang Research Journal, ISSN : 2347-7180

[12] P.Rajasekar,V. Lakshmi Sravani, G. Anjani Priya, V. Thrushitha, P. Bhavana,(2020),Efficient Combinational Logic Circuit Design Using Quantum- Dot Cellular Automata, Juni Khyat - ISSN 2278-4632VOL-10 ISSUE-5 NO. 1 MAY 2020