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# Multi valued logic gates

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***Abstract*— In a run of Typical binary VLSI circuit, interconnect represents 70% of the chip's region while the preparing transistors involve just 10% of the chip. The staying 20% is given to protection. Along these lines the plan of the parallel rationale circuits is constrained by the prerequisite of the interconnections. A more financially savvy method for giving interconnections could accordingly be of incredible advantage. A standout amongst the most encouraging ways to deal with take care of these interconnection issues is the utilization of multi valued logic (MVL) inside the VLSI chip. Various Valued Logic framework is a standout amongst the most encouraging ways to deal with acknowledge future past double hardware and frameworks. One conceivable arrangement can be accomplished by utilizing a bigger arrangement of signs over a comparable chip zone, for example, various smulti valued logice (MVL) gadgets. Numerous esteemed rationale can give improved circuit interconnections, decreased chip region and expanded transport proficiency, since more rationale levels are utilized per line when contrasted with regular twofold.**

***Keywords*— MVL,VLSI,logic level,Interconnections,Binary electronics**.

## 1.INTRODUCTION

The inventions of the transistor brought about a giant technology leap in microelectronics. With the advent of the transistor and, decades later, the arrival of the integrated circuit, power dissipation became a lesser concern. Greater emphasis was placed on performance and miniaturization, yet power dissipation was not entirely ignored. Consequently, ever since then, power requirement reduction has become one of the most critical factors in the evaluation of microelectronics technology, even for desktop applications. To continue to improve the performance of the circuits and to integrate more functions into each chip, feature size had to shrink more and more. The logic circuitry that deals with more than two logic levels is termed as multiple valued logic. This is also called multi value logic system or many valued logic system. The MVL logic system that traces its origins to the Lukasiewicz logic and post algebra. Currently there are ternary logic and quaternary logic.

## SOFTWARE TOOL

*MENTOR GRAPHICS:*

Electronic circuits can be recreated to decide how they perform. To do that the test system has to know the segments in the circuit and how they are associated. This can be given "graphically"in a schematic or as a net rundown "content record. Guide Graphics calls its schematic catch programming "Plan Architect"or "DA"for short. Fundamentally DA enables the architect to put parts on a sheet and after that interconnect them with wires. The

parts can be fundamental, for example, resistors, capacitors, transistors, or further developed segments, for example, rationale entryways (AND, OR, and so forth.). Extra segments such as input ports, control supplies, flag sources are likewise included. At last the product checks the schematic for evident blunders and makes a net rundown to be utilized by the recreation programming..


*eAND 1 GATE:*

eAND1 gate has two inputs VIN1 and VIN2 and contains two output values 0q and 1q.

Vout = 1q if VIN1 = VIN2 = 1q

Vout = 0q otherwise

*Operation of eAND1 gate*:

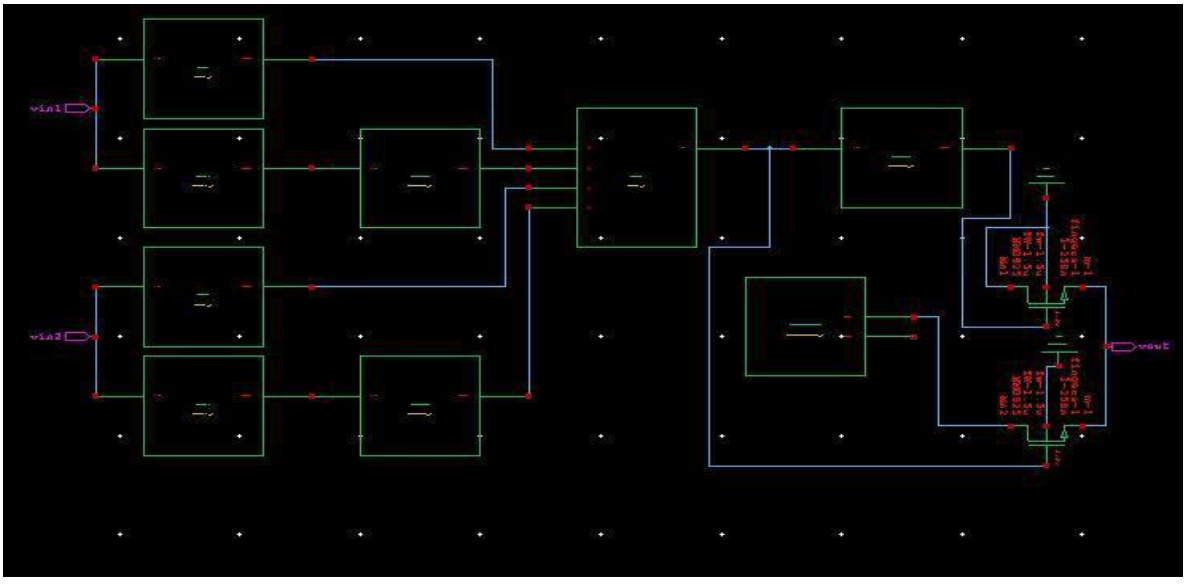
The schematic of the eand1s gate is shown in Fig 1.Two arrangements of inverters with yield Vout1inv07 and Vout1inv14 accepting both, the information 1; and Vout2inv07 and Vout2inv14 getting both, the info 2; the circuit produces E and Eb signals controlling the two changes to set the yield voltage in Vr0 = 0V or Vr1 = 1V. Signs E and Eb set separately 1q and 0q, where:

E = NOT(Vout1inv07 OR NOT(Vout1inv14 ) OR Vout2inv07 OR NOT(Vout2inv14 )

Eb = NOT (E).

NOT stands for the complement binary operator and OR stands for the OR binary operator.

Fig. 1:Schematic of eand1



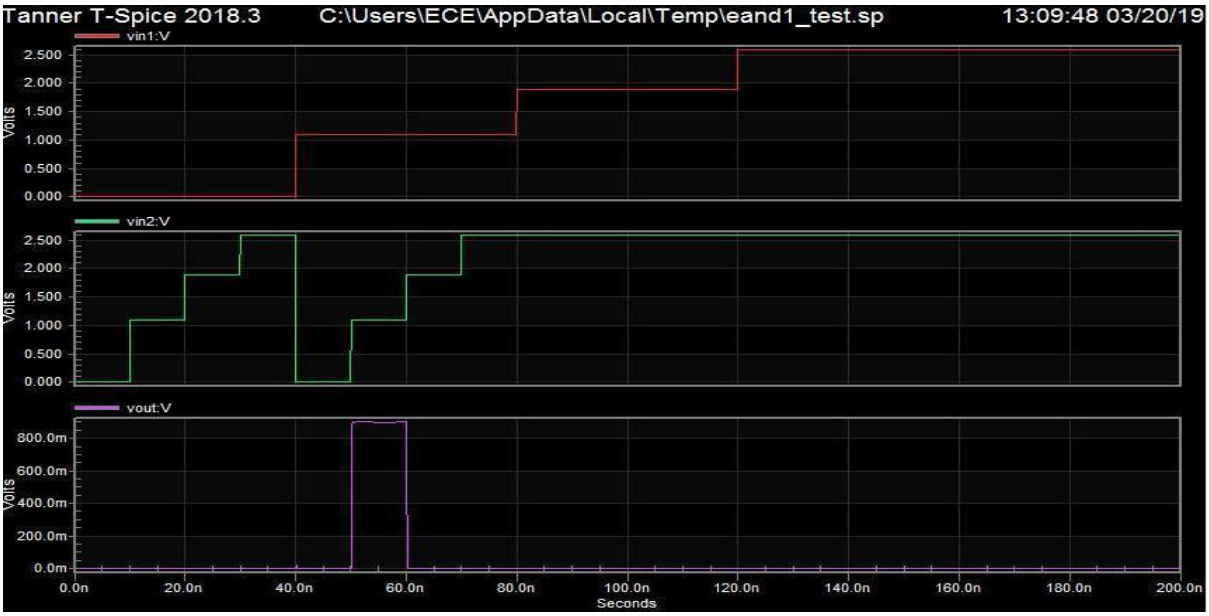



Fig. 2:Waveform of eand1

*eAND2 GATE:*

eAND2 gate has two inputs VIN1 and VIN2 and contains two output values 0q and 2q.

Vout = 2q if VIN1 = VIN2 = 2q

Vout = 0q otherwise

*Operation of eAND2 gate*:

The schematic of the eand2 gate is shown in Fig 3.Two arrangements of inverters with yield Vout1inv14 and Vout1inv22 accepting both, the info 1; and Vout2inv14 and Vout2inv22 getting both, the information 2; the circuit produces E and Eb signals controlling the two changes to set the yield voltage in VR0 = 0V or VR1 = 1.8V. Signs E and Eb set individually 2q and 0q, where:

E = NOT(Vout1inv14 OR NOT(Vout1inv22 ) OR Vout2inv14 OR NOT(Vout2inv22 )

Eb = NOT (E).

NOT stands for the complement binary operator and OR stands for the OR binary operator.

Fig. 3:Schematic of eand2

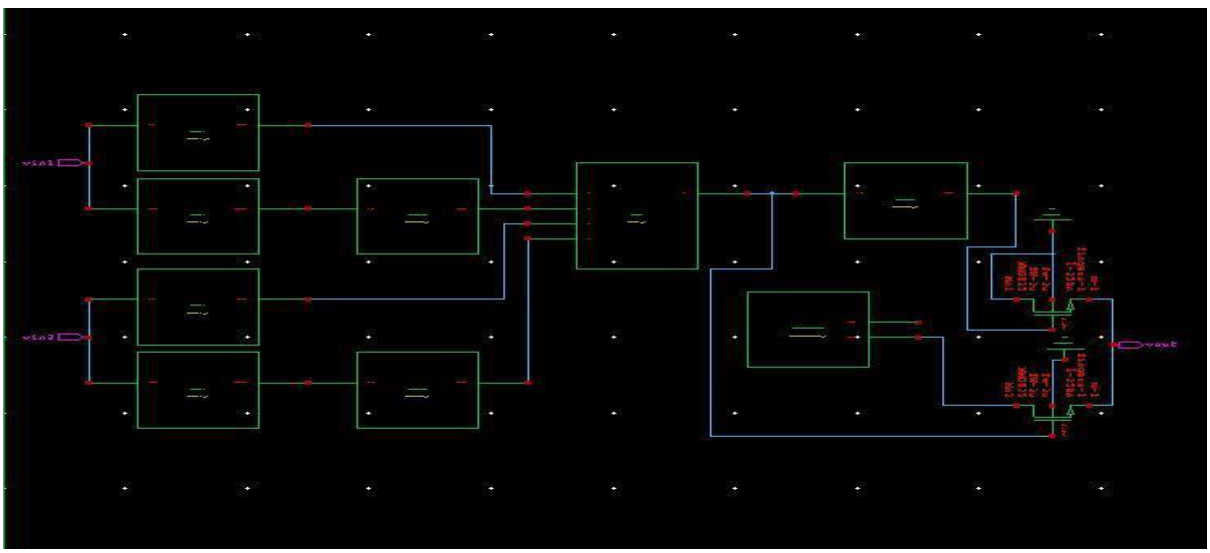



Fig.4:Waveform of eand2

*eAnd3 Gate:*

eAND3 gate has two inputs VIN1 and VIN2 and contains two output values 0q and 3q.

Vout = 3q if VIN1 = VIN2 = 3q

Vout = 0q otherwise

*Operation of eAND3 gate :*

The schematic of the eand3 gate is shown in Fig 5.The two inverters (INV122 and INV222) identify the quaternary digits 3q on its inputs and the binary NOR gate defines the logic operation and interconnects (internally) the gate output with the reference voltage VR0 or VR3 . This simple implementation is possible 111because the voltage values foe 0q and 3q are equal to 0b and 1b respectively.

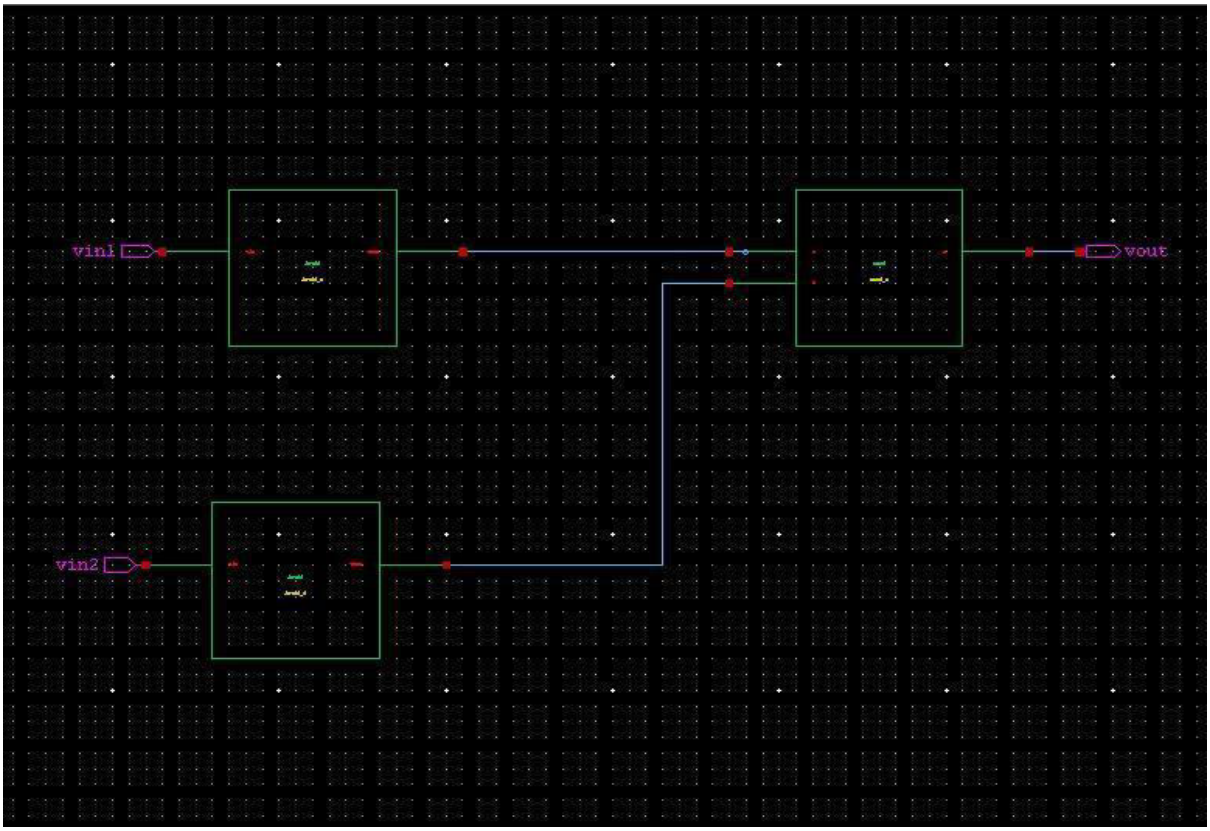



Fig. 5: Schematic of eand3

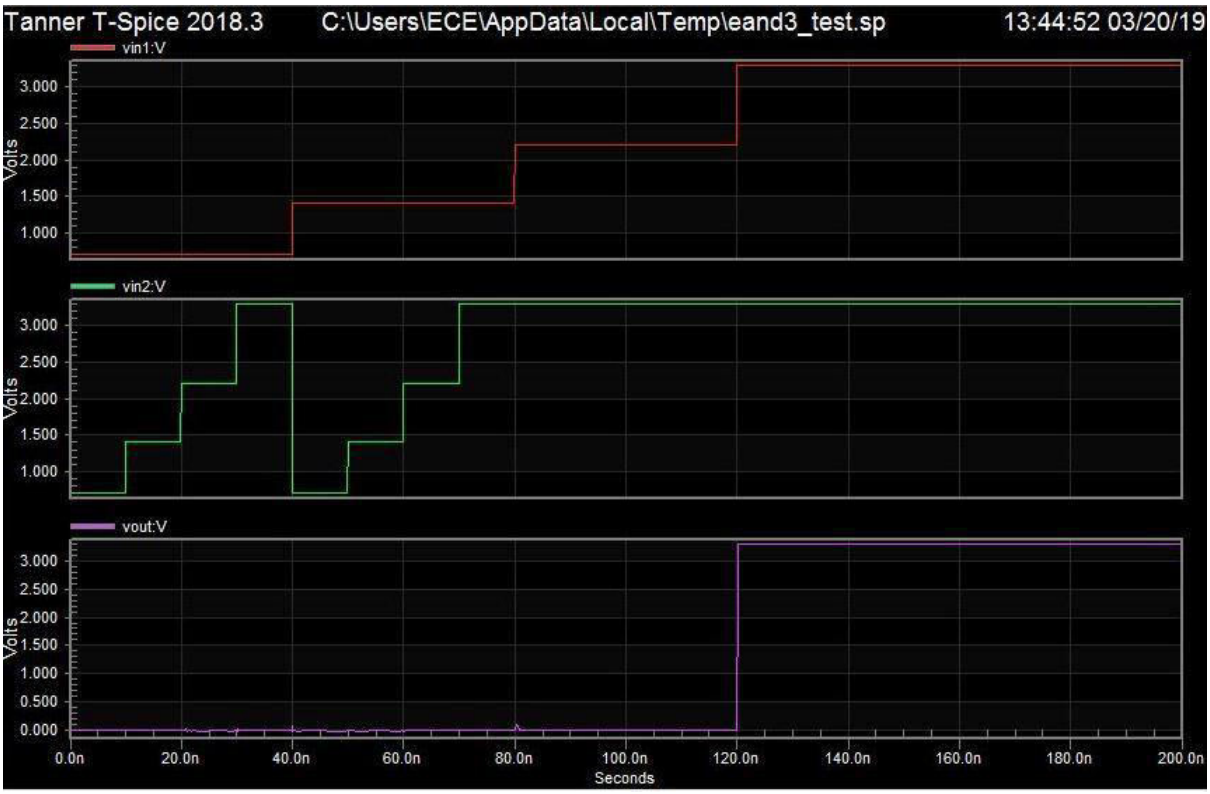



Fig. 6: Waveform of eand3

*SUCCESSOR GATE(SUC):*

Successor operator of (X) denoted by the symbol X1. By definition, X1 = Y; X,Y € Z , where is the next element from the element in the cyclic ordered set.

*Operation of SUC gate:*

The schematic of the SUC gate is shown in Fig 7. The SUC gate has one input VIN and one output VOUT with four possible output values (0q, 1q , 2q, and 3q). The full set of inverters (INV07, INV14, and INV22) and four switches are needed to identify all quaternary digits on its input and to set the output voltage in VR0 or VR1 or VR2 or VR3.

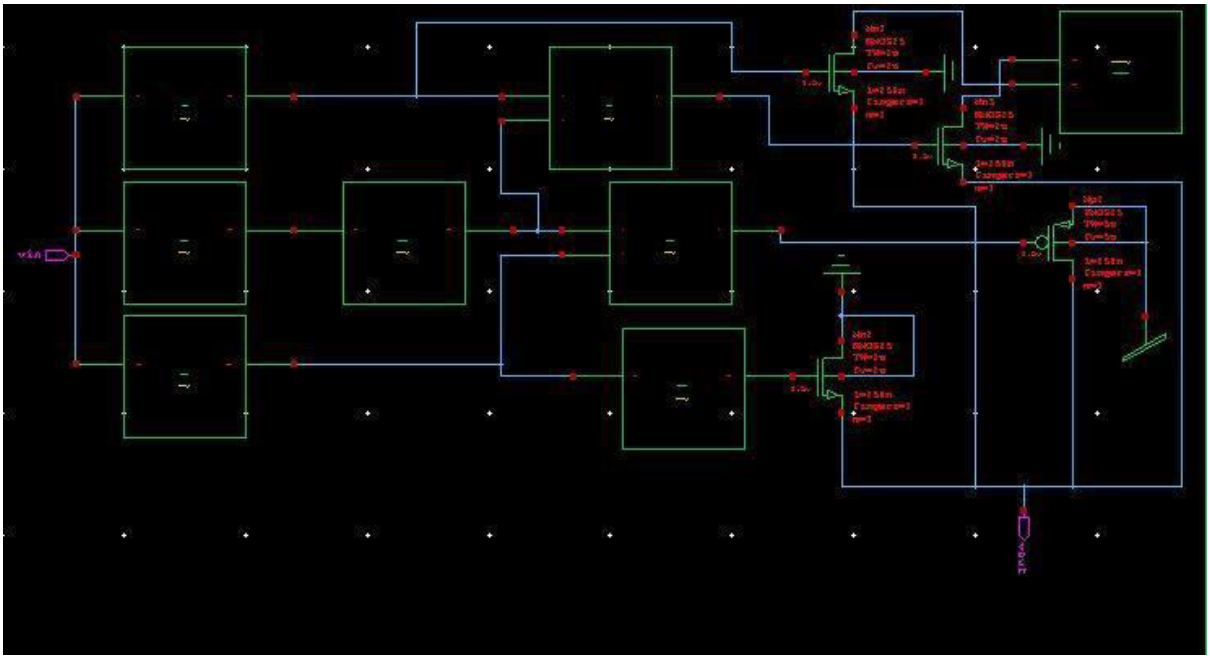


Fig. 7**:** Shematic of SUC gate

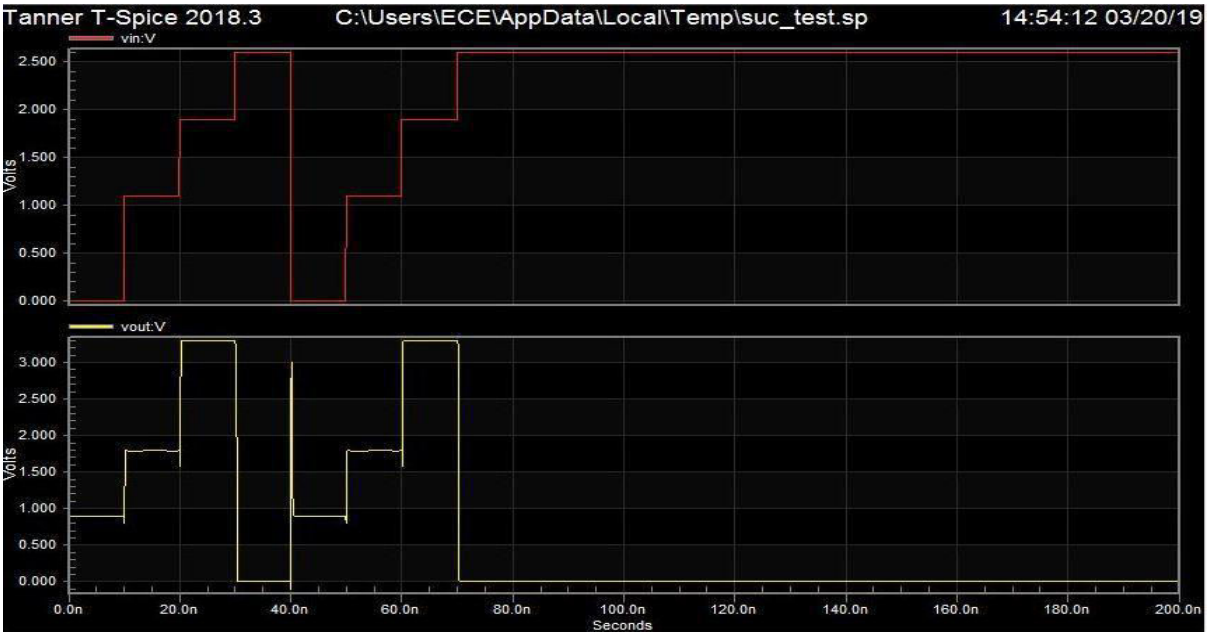



Fig. 7**:** Waveform of SUC gate

## CONCLUSION and FUTURE WORKS:

It explains the problems in the design of binary logic systems and how these drawbacks can be minimised by using MVL systems. It explains the realization of MVL logic functions. Characterisation of MVL gates such as verifying the functionality, calculating the response time by applying different input sequences, Calculation of DC Fan-out for the MVL gates by adding pull-up and pull-down resistors and measuring the maximum output currents of each gate are calculated here. Future work is also related to the design and implementation of (MVL states and gates) software EDA tools with MVL primitive components then there is a possibility to implement MVL based applications with few transistors, lower power dissipation, and using less silicon area than the presented gates.

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