

## NEUROCHIP A POTENTIAL INTERFACE FOR BRAIN CHIP INTERFACES

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ABSTRACT :- A neurochip is a tiny gadget modelled after brain-machine interfaces that simulates the activity of synapses. Its implantation into the human body enables brain and computer communication.(Duranton & Sirat, 1990) Even though they are continually being developed, data processing speed is still slower than that of the human brain. As long as it is utilised to restore damaged or absent brain functioning or for neural rehabilitation, there is no ethical dilemma. Other uses, though, seem contentious.(Blauwendraat et al., 2017) The foundation of the neurochip is a 44 array of metal electrodes, each with a caged well structure that can house a single mature cell body while allowing normal neuronal process proliferation. The expanded and more thorough content of the NeuroChip provides it a dependable, high-throughput, An imitation of the functional synapses, based on brain-machine interfaces, is what makes up a neurochip. Its implantation in the human body enables the brain's communication with low-cost screening tools for genetic studies and molecular diagnosis of neurodegenerative illnesses. Incorporating neural networks with technology, a versatile neurochip (analogue neuroprocessor) has been created.(Masumoto et al., 1993) For tackling issues with pattern recognition, data processing, and control, neural networks provide a variety of potent new solutions. They have a number of distinguishing qualities, including quick processing and the capacity to learn a problem's solution from a series of instances. Currently, two fundamental network models are used in most real-world neural network applications. We thoroughly discuss these models and explain the various methods. For resolving issues with pattern recognition, data analysis, and control. High processing speeds and the capacity to learn a problem's solution from a series of instances are only two of their standout qualities.(Gramowski et al., 2006) Currently, there are two fundamental network models that are used in the bulk of real-world neural network applications. We provide a thorough description of these models as well as an explanation of the various training methods. Chips and nerve cells contact closely physically to enable for the transmission of information in one or both ways at brain-chip interfaces (BCHIs). Multi-site recording chips interfaced to cultured neurons or implanted in the brain to record or induce neuronal excitement serve as typical examples.

• Keywords :- Neurochip, BCI, Neural Networks, Neuroprossers, Neurons, Brain sensors Introduction:- A neurochip, also known as a neuromorphic chip, is a tiny implanted device that can connect with the central nervous system to allow some parts of the brain to communicate with a computer.(Anderson et al., 2001) Although the data processing speed is still slower than that of the human brain, the neurochips include brain-machine interfaces (BMIs) that simulate the working of synapses; nonetheless, they are being developed. We are interested in measuring the electrical activity of every cell in a tiny network of cultured neurons in order to analyse the dynamics of a working neural network. In order to replicate external inputs, map connections, and investigate plasticity (changes in connections between neurons dependent on activity patterns) over periods of days or weeks, targeted and non-invasive stimulation of the neurons is also necessary. We designed and created the neurochip, a silicon micromachined device (M. P. Maher et al., 1999). These chips' purpose is to carry out a concurrent

multiplication of vector and matrices. The ability of neural networks to learn from experience in the actual world is its key characteristic. But in order to make use of the learning capacity, a dynamic connectivity device with adjustable strength is needed. The biggest issue in developing such an optical learning neurochip is a lack of as the dynamic interconnection device, the analogue spatial light modulator (SLM), which is appropriate for three-dimensional (3-D) integration.(1992; Nitta et al.). A neurochip is made up of a column of semiconductor threshold elements and an array of magnetoresistive components (which are comparable to the memory cells of a magnetic RAM). Writing, correction, and replication are the three modes in which the neurochip functions. Parallel data processing is used in the neurochip. Associative memory and image recognition are two potential uses for neurochips. In the last 10 to 15 years, theoretical models of brain networks have been developed, and neurocomputers and neurochips have been made. (Blauwendraat et al., 2017) The capacity for parallel data processing and learning are benefits of neural network devices. One of the fundamental objectives in this area is the development of associative memory (Red'ko & Zvezdin, 1997). The simultaneous recording of the electrical activity of many cultured neural networks has attracted a lot of attention for the research of numerous neurons and researching how the network reacts to different types of stimulation.(David Sánchez et al., 1998) Our research has shown that the neuronal outgrowth from these wells is identical to that on a flat array. However, when a network grows and connects from well neurons, the processes put pressure on the cell bodies that, if the cells weren't confined, would pull them out of the wells. As a result, a well design has been created that retains the cells in the wells successfully.(Maher and others, 1998).

• A novel multielectrode gadget for stimulating and recording from grown neurons is called the "neurochip."

We want to record the electrical activity of every cell in a tiny network of grown neurons to examine the dynamics of a working brain network. We establish two-way, non-invasive connection between external electronics and individual neurons cultivated in the neurochip as a first step towards analysing a whole network. (Gramowski et al., 2006)The usage of analogous devices with individual peripheral mammalian neurons, invertebrate neurons, and mammalian cell networks have all been demonstrated in the past. By connecting individual electrodes to the cell bodies of each neuron in a compact network, the neurochip greatly outperforms these techniques. With the inclusion of a tiny cage surrounding each electrode into which a single cell body can be inserted, the neurochip is basically a planar electrode array. a small cage around each electrode into which a single cell body can be placed. There is a one-to-one correspondence of neurons to electrodes; access to each neuron is unambiguous and well isolated. Recording and stimulating are non-invasive and highly specific, so that the cellular properties are not compromised and individual cells can be studied for as long as the cultures normally live (2–5 (M. P. Maher et al., 1999)directional electrical contact with individual cultured neurons. Neurochip fabrication Electronics , Electrode platinization ,Cell culture.

## • A GENERAL PURPOSE DIGITAL NEUROCHIP FOR LEARNING ON VLSI

For the learning and resolution stages of neural algorithms, we provide a general-purpose digital neurochip. It concurrently updates synaptic coefficients and neuronal states on input neurons. Using a widely used technology (1.6 mm CMOS), a device may construct 32 input and 32 output neurons with 16-bit synaptic coefficients. The usual on-chip working time is 2 s for updating one neuron state or 32 coefficients with 8-bit input neurons. (Blauwendraat et al., 2017) Additionally, many circuits can be combined to depict organised or large-size nets as well as higher-order nets. The majority of learning rules for neural networks

that have been thought of up to this point may be programmed by selecting appropriate parameters.(Duranton & Sirat, 1990) In particular, a straightforward chip configuration that makes optimum use of chip parallelism and requires little interchip connection implements the error backpropagation method. Theoretical justifications and numerical simulations specify the necessary accuracy for synaptic weights: For practically all the instances taken into consideration, 16 bits per synapse should be sufficient. (Blauwendraat et al., 2017)

• NeuroChip, an enhanced version of the NeuroX genotyping technology to quickly test for variations linked to neurological illnesses.

The ageing global population is heavily burdened by neurodegenerative disorders, which are now incurable and irreversible. According to Naj et al. (2017) and Singleton and Hardy (2016), several genes have undergone frequent and uncommon genetic changes that have been identified as diseasecausing or related to the onset of neurodegeneration. There are now four primary applications for genetics: Increasing our understanding of the molecular pathobiology of disease in the hopes of identifying therapeutic targets, 2) identifying risk variants and disease modifiers that influence risk for disease, 3) improving patient selection for pathway-specific clinical trial design, and 4) increasing our knowledge of the molecular pathobiology of disease. Therefore, having a dependable, high-throughput, and affordable platform that can do these tasks quickly might be quite beneficial. (Gabay et al., 2005). A genotyping platform that would enable quick genetic characterization of samples in the context of genetic mutations and risk factors associated with prevalent neurodegenerative diseases was the goal of the collaborative project that produced the NeuroX array, which we previously presented (Nalls et al., 2015). Based on the Infinium HumanExome Beadchip v1.1, this exonic array (also known as an exome chip) contained 242,901 exome-focused variations as well as 24,706 bespoke variants concentrating on neurological illnesses. Numerous research have already employed the NeuroX array with great success (e.g., Barber et al. 2017, Carrasquillo et al. 2016, Ghani et al. 2015, Nalls et al. 2016, Rosenthal et al. 2016). Additionally, there was a constant need to update this helpful platform due to the growing amount of genotype-phenotype relationships and harmful mutations.

- INFORMATION ABOUT ANALOGUE NEUROCHIPS, INCLUDING TYPES AND FUNCTIONS
- Multilayered artificial neural networks' use of analogue neurochips:- A versatile neuro-chip (analogue neuroprocessor) created for real-world uses in which neural networks would be incorporated into machinery. a study describes the multilayered artificial neural networks that operate on an analogue neurochip. (Masumoto et al., 1993)2 m BI-CMOS technology was used to create this new chip. Signals for input and output are analogue, whereas weights are digitally represented. Analogue data can be sampled at intervals of 13 s using an analogue time-sharing bus for input and output. The present chip has issues with digit overflow, considerable weight digit loss, and device characteristic dispersion. A few solutions to these issues were also looked at.Masumoto and others, 1993.
- Neural Competition in Frequency and Time Domains: Analogue Integrate-and-Fire Neurochips This explains an inhibitory neural network that is constructed on an analogue CMOS device and it displays competitive behaviour in the frequency and time domains. Each neuron's circuit was built to generate spikes,(Asai et al., 2002) or timed sequences of pulses with the same form. The results

of the experiment and simulation showed that the network was able to selectively operate upon and deactivate the neuron circuits more effectively on the basis of spiks timing than on the basis of firing rates. According to Asai et al.

- Acoustical mixed analog-digital neurochip Attention:- The technology simulates the human ability to distinguish unfamiliar noises in a natural environment. Interaural time delay is used to differentiate sound sources. The novelty of a sound, learned knowledge, and interaction with other sensorimotor systems all influence acoustical attention. Binary spikes are used to mimic the biology of early receptive signals. At various performing phases, uniform models of pulse propagating cells and synapses are applied. (Zahn et al., 1996)
- Utilising Stochastic Logic to Implement a New Neurochip

Despite extensive research and development into neurochips, the most effective method for application is still unclear. In our method, we use stochastic logic to perform various operations needed for neural functions. Toto et al. (2003) Stochastic logic has the benefit of allowing complicated operations to be accomplished using just a small number of standard logic gates. (Schoenauer et al., 2000) On the other hand, because stochastic logic necessitates a specific accumulation period for averaging, the operating speed is not as quick. However, due to the fact that all operations are carried out on digital circuits, a high level of integration may be obtained. (Sato et al., 2003) Additionally, we suggest a stochastic logic-based nonmonotonic neuron since this trait is effective for boosting association and learning performance. In this study, the circuit design and measurement outcomes of a neurochip with 50 neurons are presented. The benefits of stochasticism and nonmonotonicity are demonstrated clearly. (Sato et al. 2003).

- i. DESIGN OF A STOCHASTIC NEUROCHIP WITH NONMONOTONIC : Nonmonotonic Neurons, Learning Circuit
- ii. HARDWARE IMPLEMENTATION : Learning Outcomes, Application to an Optimisation Problem
- A digital neurochip that can be customised to handle several networks

Here, we'll talk about a self-configurable digital neurochip with a multi-network architecture that can handle a lot of characters or an image recognition system. Recent advancements in multiprocessor design [I] and the reduction strategy [31 of the amount of calculations have led to the development of neurochips that function at high speeds.(Zahn et al., 1996) However, such neuro chips are quite pricey due to the requirement for a huge memory for synaptic weights and their unsuitability for recognition with several categories. in order to conduct recognition more effectively while using less memory. Up until recently, the best network size and smne parameters had to be determined by trial and error. In order to do this, we created two new schemes: "DSP architecture suitable for a proliferating neuron" and "method of ad- dressing to multi-network"; both of which were then implemented in a 0.5 um CMOS process. The outcome was a sharp drop in overall memory to just 9%. This chip has a performance of 1.75 msec/chwicter and can categorise



up to 16.384 categories at once. It can reduce the price and make the identification system more compact (Maruyama et al., 1996).

• Using RBF networks to build a real-time neurocomputer

An RBF network-based real-time neurocomputer is discussed along with its architecture. For purposes of targeting and surveillance, the subsystem is incorporated into an avionics system.(David Sánchez et al., 1998) The architecture of an RBF network-supporting hardware module built on neurochips is provided, together with information on how it may be used to identify signal peaks and create an integrated training and testing environment for RBF networks. The construction of a neurocomputer that realises real-time signal processing for surveillance and targeting operations in an avionics system is the main subject of this article.David Sánchez and other authors, 1998 The design of the neurocomputer makes use of RBF network-supporting neurochip technologies available commercially. Only unclassified subjects are discussed, but the writers are certain that this does not alter how the main principles are explained.(David Sánchez et al., 1998) A signal processor, a system controller, a signal pre-processing subsystem, an antenna and communication subsystem, and enhanced display and control are among the primary subsystems. The description of how to use a neurocomputer to enable real-time capabilities in a signal processor is the focus of this study.

• Developing, Recording, and Stimulating Cultured Networks Using a Neuron-Based on Carbon Nanotube

Using a unique smart multi-electrode array arrangement, high-resolution and high-fidelity extracellular recording and stimulation are made possible by the electrodes' ability to engineer the network architecture to adapt to their array shape. The novel electrode configuration comprises of molybdenum wires that have active carbon nanotube mats at their ends. Compared to their low affinity for the passivated substrate, cells have a high affinity for the carbon nanotube sites, which creates an effective cell patterning process.(Gabay et al., 2005) Although no sticky chemicals (such Poly-L-Lysine) were applied, cells plated on these electrodes show a preference for accumulating on the active areas. Neurite linkages between the active sites were created after several days in culture, with the majority of these links being directed inward towards the closest neighbours Additionally, the impact of cell desity on the linkages' morphology was investigated. The success of the manufacturing strategy to make electrical contact with the CNT mats was validated by cyclic voltammetry measurements, which also showed improved interface resistance compared to ordinary electrodes. For the first time, our innovative method makes it possible to accurately construct the architecture and connection characteristics of genuine neural networks in coordination with superior recording components.(2005) (Gabay et al.).

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• The Neurochip-2, a self-contained head-mounted computer, is used to observe and influence monkeys acting freely.

The Neurochip-2 is a battery-powered, second-generation device that can fit within a chamber on a monkey's skull that records and stimulates brain activity. It has three recording channels that may be modified to capture arm acceleration, electrocorticography, local field potentials, single unit activity, and more. (Zahn et al., 1996)The gains, filters, and sample rates for these channels may all be changed by the user. The captured data is stored on a portable flash memory card. The Neurochip-2 likewise has three different stimulation channels.(Blauwendraat et al., 2017) Two "programmable-system-on-chips" (PSoCs) control the data acquisition and stimulation output. The PSoCs may be used to handle the recorded data in real-time in a number of ways, such as time-amplitude window discrimination and digital filtering. The PSoCs can be made to deliver preprogrammed stimuli or to respond to brain activity by stimulating the recipient. Through access pins on the microcontroller, other devices, including accelerometers, may also be attached. The capacity of the Neurochip-2 to record and stimulate monkeys with free movement for up to several days at a time enables a range of state-of-the-art neurophysiological and neuroengineering experiments.



A) Block diagram of the major Neurochip-2 components and signal routing. G: gain, LF: low-pass fi lter cutoff (Hz), PSoC: programmable system-on-chip, SPI: serial peripheral interface, AVR: Atmel AVR microcontroller, DAC: digital-to-analog converter. Connections between the battery and active components are not shown. (B) Circuit diagram of one of the "V to I converter" blocks(Zanos et al., 2011)

## • FUTURE DIRECTIONS OF NEUROCHIPS APPLICATIONS

The neuromorphic chip-based BMI is kept at an experimental level; although the technology is still in its early stages, it is developing. Based on the outcomes of the invasive non-DBS implants, transcranial magnetic stimulation (TMS), and DBS, which are all well-known technical techniques, future paths of neurochip applications will be determined. (Red'ko & Zvezdin, 1997)DBS has historically been used to treat a wide range of neurological symptoms that are resistant to conventional medical therapy (pain, tremor, severe depression, obsessive compulsive disorder,



anorexia, disorders of consciousness, use of brain signals to control a prosthetic arm for motor assistance in quadriplegia, terminal phase of lateral amyotrophic sclerosis, or locked-in syndrome). (Asai et al., 2002)The experience with noninvasive TMS is the other technical development that has given a foundation for potential uses of neurochips in the future. It is now used to address some learning challenges; in other circumstances, it is only used to experiment with new things or even for pleasure, such boosting sensual experiences.

• Brain-Chip Interfaces: The Present and The Future

Chips and nerve cells connect closely physically at brain-chip interfaces (BCHIs), which enables the flow of information in one or both ways. Multi-site recording chips interfaced to cultured neurons or implanted in the brain to record or induce neuronal excitement serve as common examples.(Zanos et al., 2011) We give an overview of recent developments in BCHIs that improve the signal-to-noise ratio or the spatiotemporal resolution of signals sent from nerve cells to chips or from chips to nerve cells. High signal-to-noise ratio recording is made possible by micro-nail sized microelectrodes that are absorbed by neurons in culture and provide a close electrical link with the cells. As recently demonstrated by recordings from hippocampal slices and brain cortex in implanted animals, oxide-insulated chips with large-scale and high-resolution arrays of stimulation and recording elements represent a promising technology for high spatiotemporal resolution interfacing. Although chemical signalling must also be taken into account and there have been recent advancements in this area, most BCHIs deal with electrical signals.(Maher et al., 1998) Finally, we outline and talk about significant difficulties in creating future generations of BCHIs.

DISCUSSION:- We want to record the electrical activity of every cell in a tiny network of grown neurons to examine the dynamics of a working brain network. To replicate external inputs, map connections, and research plasticity-changes in connections between neurons dependent on activity patterns—neuron stimulation that is non-invasive and focused is also necessary.(Gramowski et al., 2006) We want to measure all of the electrical activity in a tiny network of cultivated neurons in order to analyse the dynamics of a working neural network. In order to map connections, replicate external inputs, and research plasticity-changes in connections between neurons dependent on activity patterns-neuron stimulation that is non-invasive and targeted is also necessary. The Neurochip array platform for high throughput genotyping has been created, put into use, and verified by us. It's crucial to understand this strategy's limits, though.(Zoladz et al., 2011) In recent years, the application of on-chip MEMS in the biomedical industry has drawn more and more attention. New generations of MEMS functioning as scientific, diagnostic, and therapeutic instruments are being developed as a result of the continual advancement of micromachining and microelectronics technologies and concurrent expanding understanding of cellular and molecular mechanisms in life sciences.(Masumoto et al., 1993) Discussions regarding neurotechnology are mostly restricted to a small group of academics, including bioethicists, science fiction fans, artists, and neurotechnological engineers.

- CONCLUSION :- A neurochip, also known as a neuromorphic chip, is a tiny implanted device that can potentially connect specific parts of the brain to a computer. Although the data processing speed is still slower than that of the human brain, the neurochips have brain-machine interfaces (BMIs) that simulate the functioning of synapses.(Sato et al., 2003) The design and implementation of the Neurochip array, which has a more complete and improved content than NeuroX, is currently being worked on. The community is given a fresh tool by this adaptable genotyping platform, which may be utilised in clinical and research contexts.(Blauwendraat et al., 2017) It has been created and experimentally tested to produce neurochip logic components with acceptable operation margins. To simulate the human brain digitally, artificial neural networks are developed. They may be used to create the future generation of computers. Currently, they are utilised for complicated analysis in a variety of disciplines, from engineering to medical. The gaming industry and other sectors depend heavily on artificial neural networks already.
- REFERNCES:- Anderson, P. G., Klein, G., Oja, E., Steele, N. C., Antoniou, G., Mladenov, V., & Paprzycki, M. (2001). Neural networks and their applications: Introduction. *Informatica (Ljubljana)*, 25(1), 1.
- Asai, T., Hayashi, H., & Amemiya, Y. (2002). Analog integrate-and-fire neurochips: Neural competition in frequency and time domains. *Multimedia, Image Processing and Soft Computing: Trends, Principles* and Applications - Proceedings of the 5th Biannual World Automation Congress, WAC 2002, ISSCI 2002 and IFMIP 2002, 13, 129–134. https://doi.org/10.1109/wac.2002.1049533
- Blauwendraat, C., Faghri, F., Pihlstrom, L., Geiger, J. T., Elbaz, A., Lesage, S., Corvol, J. C., May, P., Nicolas, A., Abramzon, Y., Murphy, N. A., Gibbs, J. R., Ryten, M., Ferrari, R., Bras, J., Guerreiro, R., Williams, J., Sims, R., Lubbe, S., ... Heutink, P. (2017). NeuroChip, an updated version of the NeuroX genotyping platform to rapidly screen for variants associated with neurological diseases. *Neurobiology of Aging*, 57, 247.e9-247.e13. https://doi.org/10.1016/j.neurobiolaging.2017.05.009
- David Sánchez, V. A., Sloat, S., Guerrero, J., Shullo, D., & Lefebvre, M. (1998). The design of a real-time neurocomputer based on RBF networks. *Neurocomputing*, 20(1–3), 111–114. https://doi.org/10.1016/S0925-2312(98)00023-X
- Duranton, M., & Sirat, J. A. (1990). Learning on VLSI: A general-purpose digital neurochip. *Philips Journal of Research*, 45(1), 1–17. https://doi.org/10.1109/ijcnn.1989.118451
- Gabay, T., Kalifa, I., Ezra, L., Jakobs, E., Ben-Jacob, E., & Hanein, Y. (2005). Carbon nanotube based neuro-chip for engineering, recording and stimulation of cultured networks. *Digest of Technical Papers - International Conference on Solid State Sensors and Actuators and Microsystems*, *TRANSDUCERS '05*, 2, 1226–1229. https://doi.org/10.1109/SENSOR.2005.1497300
- Gramowski, A., Jügelt, K., Stüwe, S., Schulze, R., McGregor, G. P., Wartenberg-Demand, A., Loock, J., Schröder, O., & Weiss, D. G. (2006). Functional screening of traditional antidepressants with primary cortical neuronal networks grown on multielectrode neurochips. *European Journal of Neuroscience*, 24(2), 455–465. https://doi.org/10.1111/j.1460-9568.2006.04892.x
- Maher, M., Wright, J., Pine, J., & Tai, Y. C. (1998). Microstructure for interfacing with neurons: The neurochip. Annual International Conference of the IEEE Engineering in Medicine and Biology -Proceedings, 4(4), 1698–1702. https://doi.org/10.1109/iembs.1998.746911

Masumoto, D., Ichiki, H., & Yoshizawa, H. (1993). Analog neurochip and its applications to multilayered

artificial neural networks. Fujitsu Scientific and Technical Journal, 29(3), 234–241.

- Red'ko, V. G., & Zvezdin, K. A. (1997). A magnetoresistive neurochip: Architecture and operation. *Russian Microelectronics*, 26(6), 360–364.
- Sato, S., Nemoto, K., Akimoto, S., Kinjo, M., & Nakajima, K. (2003). Implementation of a New Neurochip Using Stochastic Logic. *IEEE Transactions on Neural Networks*, 14(5), 1122–1127. https://doi.org/10.1109/TNN.2003.816341
- Schoenauer, T., Atasoy, S., Mehrtash, N., & Klar, H. (2000). Simulation of a digital neuro-chip for spiking neural networks. *Proceedings of the International Joint Conference on Neural Networks*, 4, 490–495. https://doi.org/10.1109/ijcnn.2000.860819
- Zahn, T., Izak, R., & Trott, K. (1996). Mixed analog-digital Neurochip for acoustical.
- Zanos, S., Richardson, A. G., Shupe, L., Miles, F. P., & Fetz, E. E. (2011). The neurochip-2: An autonomous head-fixed computer for recording and stimulating in freely behaving monkeys. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 19(4), 427–435. https://doi.org/10.1109/TNSRE.2011.2158007
- Zoladz, M., Kmon, P., Grybos, P., Szczygiel, R., Kleczek, R., & Otfinowski, P. (2011). A bidirectional 64channel neurochip for recording and stimulation neural network activity. 2011 5th International IEEE/EMBS Conference on Neural Engineering, NER 2011, 380–383. https://doi.org/10.1109/NER.2011.5910566
- Anderson, P. G., Klein, G., Oja, E., Steele, N. C., Antoniou, G., Mladenov, V., & Paprzycki, M. (2001). Neural networks and their applications: Introduction. *Informatica (Ljubljana)*, 25(1), 1.
- Asai, T., Hayashi, H., & Amemiya, Y. (2002). Analog integrate-and-fire neurochips: Neural competition in frequency and time domains. *Multimedia, Image Processing and Soft Computing: Trends, Principles* and Applications - Proceedings of the 5th Biannual World Automation Congress, WAC 2002, ISSCI 2002 and IFMIP 2002, 13, 129–134. https://doi.org/10.1109/wac.2002.1049533
- Blauwendraat, C., Faghri, F., Pihlstrom, L., Geiger, J. T., Elbaz, A., Lesage, S., Corvol, J. C., May, P., Nicolas, A., Abramzon, Y., Murphy, N. A., Gibbs, J. R., Ryten, M., Ferrari, R., Bras, J., Guerreiro, R., Williams, J., Sims, R., Lubbe, S., ... Heutink, P. (2017). NeuroChip, an updated version of the NeuroX genotyping platform to rapidly screen for variants associated with neurological diseases. *Neurobiology of Aging*, 57, 247.e9-247.e13. https://doi.org/10.1016/j.neurobiolaging.2017.05.009
- David Sánchez, V. A., Sloat, S., Guerrero, J., Shullo, D., & Lefebvre, M. (1998). The design of a real-time neurocomputer based on RBF networks. *Neurocomputing*, 20(1–3), 111–114. https://doi.org/10.1016/S0925-2312(98)00023-X
- Duranton, M., & Sirat, J. A. (1990). Learning on VLSI: A general-purpose digital neurochip. *Philips Journal of Research*, 45(1), 1–17. https://doi.org/10.1109/ijcnn.1989.118451
- Gabay, T., Kalifa, I., Ezra, L., Jakobs, E., Ben-Jacob, E., & Hanein, Y. (2005). Carbon nanotube based neuro-chip for engineering, recording and stimulation of cultured networks. *Digest of Technical Papers - International Conference on Solid State Sensors and Actuators and Microsystems, TRANSDUCERS '05, 2,* 1226–1229. https://doi.org/10.1109/SENSOR.2005.1497300
- Gramowski, A., Jügelt, K., Stüwe, S., Schulze, R., McGregor, G. P., Wartenberg-Demand, A., Loock, J., Schröder, O., & Weiss, D. G. (2006). Functional screening of traditional antidepressants with primary cortical neuronal networks grown on multielectrode neurochips. *European Journal of Neuroscience*, 24(2), 455–465. https://doi.org/10.1111/j.1460-9568.2006.04892.x

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- Maher, M., Wright, J., Pine, J., & Tai, Y. C. (1998). Microstructure for interfacing with neurons: The neurochip. Annual International Conference of the IEEE Engineering in Medicine and Biology -Proceedings, 4(4), 1698–1702. https://doi.org/10.1109/iembs.1998.746911
- Masumoto, D., Ichiki, H., & Yoshizawa, H. (1993). Analog neurochip and its applications to multilayered artificial neural networks. *Fujitsu Scientific and Technical Journal*, 29(3), 234–241.
- Red'ko, V. G., & Zvezdin, K. A. (1997). A magnetoresistive neurochip: Architecture and operation. *Russian Microelectronics*, 26(6), 360–364.
- Sato, S., Nemoto, K., Akimoto, S., Kinjo, M., & Nakajima, K. (2003). Implementation of a New Neurochip Using Stochastic Logic. *IEEE Transactions on Neural Networks*, 14(5), 1122–1127. https://doi.org/10.1109/TNN.2003.816341
- Schoenauer, T., Atasoy, S., Mehrtash, N., & Klar, H. (2000). Simulation of a digital neuro-chip for spiking neural networks. *Proceedings of the International Joint Conference on Neural Networks*, 4, 490–495. https://doi.org/10.1109/ijcnn.2000.860819

Zahn, T., Izak, R., & Trott, K. (1996). Mixed analog-digital Neurochip for acoustical.

- Zanos, S., Richardson, A. G., Shupe, L., Miles, F. P., & Fetz, E. E. (2011). The neurochip-2: An autonomous head-fixed computer for recording and stimulating in freely behaving monkeys. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 19(4), 427–435. https://doi.org/10.1109/TNSRE.2011.2158007
- Zoladz, M., Kmon, P., Grybos, P., Szczygiel, R., Kleczek, R., & Otfinowski, P. (2011). A bidirectional 64channel neurochip for recording and stimulation neural network activity. 2011 5th International IEEE/EMBS Conference on Neural Engineering, NER 2011, 380–383. https://doi.org/10.1109/NER.2011.5910566