Next-Generation SRAM: Design and Optimization with Carbon Nanotubes

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Abstract

Static Random Access Memory (SRAM) serves as a critical component in modern electronic devices, offering high-speed access to stored data. As technology continues to advance, there's a growing demand for smaller, faster, and more energy-efficient memory solutions. Carbon nanotubes (CNTs) have emerged as apromising material for pushing the boundaries of conventional silicon-based SRAM designs. This paper presents a comprehensive exploration of the design andoptimization of next- generation SRAM utilizing carbon nanotubes. The unique properties of CNTs, suchas their exceptional electrical conductivity, mechanical strength, and nanoscale dimensions, offer a fertile ground for revolutionizing SRAM architecture.

The study delves into the integration of CNTs intoSRAM cell structures, discussing variousconfigurations and layouts to harness the advantageous characteristics of carbon nanotubes. Emphasis is placed on addressing the challenges associated with CNT-based SRAM, including manufacturing scalability, reliability, and variability. In conclusion, the integration of carbon nanotubesin SRAM design offers a compelling avenue to overcome the limitations of traditional silicon-based memory technologies. This study not only highlights the promising prospects of CNTs in SRAM but also provides insights into the challenges and opportunitiesin harnessing these nanomaterials for advanced memory applications.

Keywords : Static Random Access Memory (SRAM), Carbon Nanotubes (CNTs), Nanotechnology, Memory Design, Optimization, Electronic Devices, Nanomaterial Integration.

Introduction

The evolution of semiconductor technology has been a driving force behind the advancements in modern computing. Among the fundamental components crucial for high-speed and high- density memory in these systems is Static Random Access Memory (SRAM). SRAM has been a cornerstone in various applications, from embedded systems to cache memories in processors, due to its speed, non- volatility, and ease of integration.

However, as demands for faster and more energy-efficient computing systems continue to surge, conventional silicon-based SRAM faces challenges concerning power consumption, leakage currents, andscaling limitations. To overcome these hurdles and usher in the next generation of memory technologies, researchers and engineers have turned their attention to innovative materials and nanoscale designs, particularly exploring the potential of Carbon Nanotubes (CNTs) in SRAM.

Carbon nanotubes, with their exceptional electrical, mechanical, and thermal properties, offer a promising alternative to traditional silicon-basedtransistors. Their high carrier mobility, low powerconsumption, and potential for seamless integration into existing semiconductor

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manufacturing processes make them an intriguing candidate for enhancing SRAM performance.

This exploration delves into the design, optimization, and potential applications of next- generation SRAM using Carbon Nanotubes. It aims toinvestigate the challenges and opportunities in leveraging CNTs for developing high-performance, low-power, and highly scalable SRAM architectures. By understanding the intricacies of CNT-based SRAM design and optimization, this study seeks to contribute to the development of future computing systems that can meet the ever-increasing demands for speed, efficiency, and miniaturization.

METHODOLOGY

The CMOS-based SRAM cells suffered from short channel effects (SCEs), mobility degradation, etc. when considering the channel length of 32 nm. Hence, the CMOS devices did not produce betterperformance in 32 nm channel length. This drawback was overcome by introducing the multi-gate devices such as Fin-FET and CNFET. In recent decades, the CNTs have more attention because of its thermal, electrical and mechanical properties. Based on the ultra long mean-free path, theCNFETs are classified for elastic scattering, which is similar for holes, electrons, easy combination of high-K dielectric materials, and high Fermi velocity characteristics. The fabrication process of the CMOS and CNFET is similar, and the design approaches of CMOS are separated for CNFET based circuit design.Due to the huge current drive capability, less PDP (Power Delay Product), high thermal stability and ballistic transport, the CNFETs have been considered promising devices.

Figure 1 shows the layouts of the CNFET where the channel regions are highly doped and less dopant are added to the CNT channel. These are considered the interconnection between the 2 adjacent devices orS/D extended region. The single intrinsic CNT (inset)model is depicted in Figure 1, which is the origin point of the modeling of complete CNFET devices.

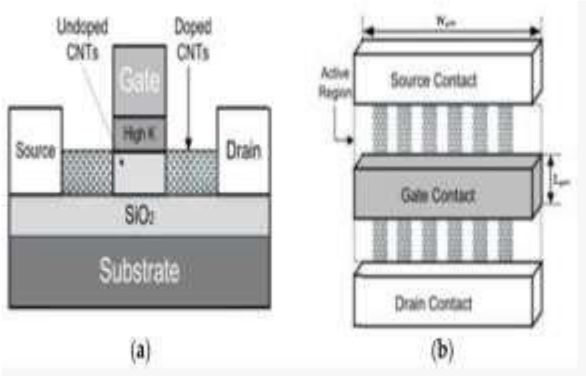


Figure 1. Layout of the CNFET device.

Figure 2 : a,b show the CNFET's side and top view, which consist of 6 single walled CNTs considered asthe channel material. The CNT is either a semiconducting or metallic material based on thechirality factor. The recent CNFETs give considerable percentage for metallic.

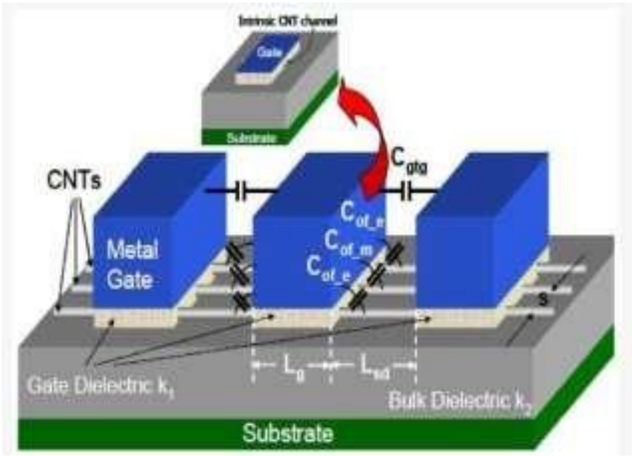


Figure 2. (**a**) Side view of a CNFET, (**b**) Topview of CNFET.

The initial stage of the CNFET fabrication involves the parallel metal strips pre-patterning in SiO2 substrate. Once thepre-patterning process is completed, CNTs are deposited at thetop in a random manner. This CNTs fall around the two metal strips and meet all necessary requirements for basic FET. Here, one metal for the source terminal and another for the drain terminal. The source/drain terminals are made from the chromium/gold materials and SiO2

Parameters	Si-CMOS	CNFET
Vt	0.2–0.5 V	0.293 V, −0.557 V, & −0.293 V
Idlin	$I_D = \mu C_{ox}\frac{W}{L}[(V_{GS}-V_{TH})V_{DS} - \frac{V_{DS}^2}{2}]$	$I_d = K_n[2(V_{gs}-V_T)V_{ds} - V_{ds}^2]$
Idsat	$I_D = \mu C_{ox}\frac{W}{2L}(V_{GS}-V_{TH})^2$	$I_{d(sat)} = K_n(V_{gs}-V_T)^2$
SS	~70 mV/dec (@ Room Temperature)	61.3 mV/dec
DIBL	$DIBL = \frac{V_{Th}^{DD}-V_{Th}^{low}}{V_{DD}-V_D^{low}}$	65.65 mV/V

Table 1. Parameters of Si-CMOS and CNFET.

used as the gate oxide. A collection of 6- transistors, along with a sense amplifier, writecircuitry, and row and column decoders are used to construct the conventional SRAM cell, and itsschematic view is depicted in the Figure 3.

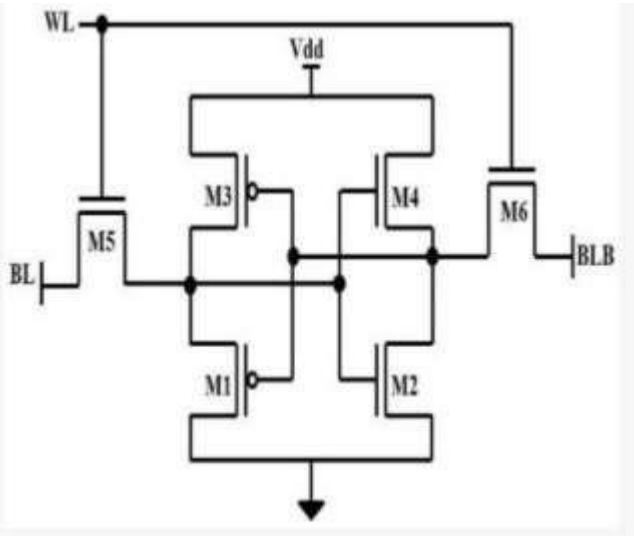
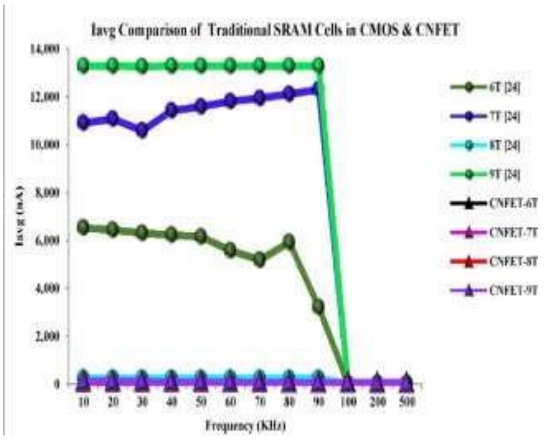
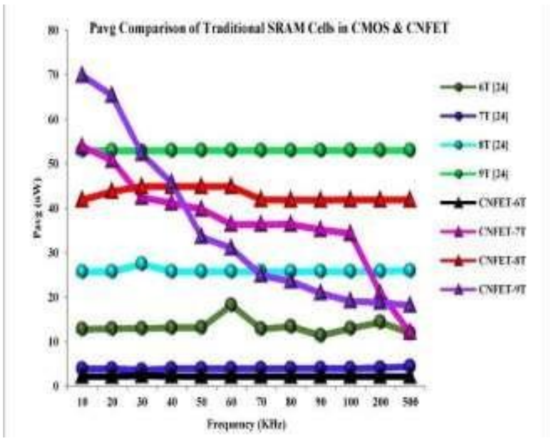


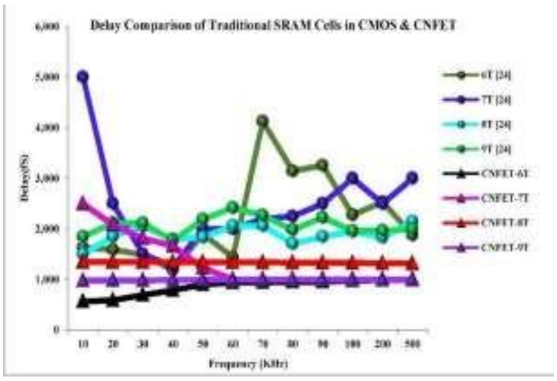
Figure 3. Traditional 6T-SRAM cell

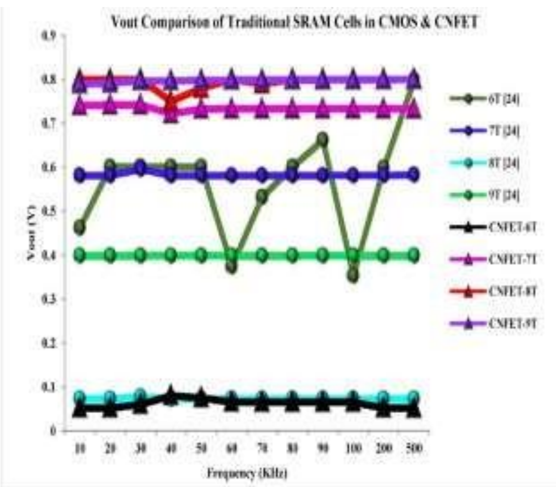
Read Operation: SRAM cell addresses are decoded by the column and row decoders in which thedata has to be read. Initially, the BL is pre-charged to V before the read operation starts. Once the word line (WL) is activated, the B is discharged via the M5 transistor. The voltage variation in the BL is very small due to the limited capability of the cell driving current. The small voltage difference across BLs is sensed by the sense amplifier, and finally, whether thevalue "1" or "0" is stored in the SRAM cell.

Write Operation: with the help of the externaldevices, the









data has to be stored. The column- row decoders are used for providing the address of the cell.When the WL is enabled, the write function is processed to write the data into the cell, which is fully dependent on the column gate condition. The amount of time consumed by the write operation is less when compared with the reading operation time because thewrite buffer has a high capability to drive the huge driving current

RESULTS AND DISCUSSIONS

The overall implementations of the existing and proposed methods are implemented in the twodifferent technologies at 32 nm channel length inLT spice and H Spice simulators. The CNFET device can be realized with the help model files available. Low power consumption is the ultimate aim in VLSI circuits. To achieve this, we have to measurethe power consumption of different SRAM cell and this can be held by parameter P avg. Another important parameter is delay which shows the time taken by the SRAM cells to produce the outputs frominput bit-lines. If we achieved less amount of delay, then the SRAM cells will be operated in high-speed. For proving the SRAM cells performance, wecalculate V out, I avg, P avg , E avg and delay. For detailed comparison, the design approaches implemented in multiple frequencies varies from 10 KHz–500 KHz.

CONCLUSION

The presented paper clearly dealt the lot of designing methods for SRAM design for low power applications. The paper contains both CMOS and CNFET technology-based practical implementations. As a result of this implementation, the CMOS technology does not perform properly when considering the 32 nm channel length. At 32 nm channel length, it produced undesired effects like short channel effect and mobility degradation, etc., This limitation is overcome by CNFET-based SRAMcell design approaches. Hence, the paper proves that CNFET-based Multi-Threshold SRAM design performs better than traditional SRAM cells in CMOS techniques. The proposed design will be further developed by infusing the power reduction techniques.

In many electronic devices and microprocessors, the SRAM (Static Random Access Memory) is commonly used for caches. The SRAM produced better performance compared with the Dynamic Random Access Memory (DRAM). The DRAM capacity is much greater than the static type and it needs more time to refresh itself. This time delaycauses the increment of the latency to access the data. In recent electronic devices that are assigned for particular applications such as multimedia, object tracking, video processing, and medicine, the computation process and complexity have beenincreased and it is also reflected in the power consumption. These devices have unique processors that consumed huge SRAM sub-modules. Hence, the SRAM is one of the much delegated memory modules for power considerations. The limitation of the SRAM power consumption is performed by decreasing Vdd supply voltage or Vth threshold voltage.

The high-low threshold transistor pairs are used to change the channel length by modifying the oxide thickness of the transistors. The overall implementation of the Multi-threshold-based SRAM cells are implemented with the help of CNFET. Carbon Nanotube Field-Effect Transistors (CNFETs) in Static Random Access Memory (SRAM) have shown promising potential due to their ability to offer

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