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Optimization of Efficiency and Parameters of Dc-Dc Converter Using Enhanced Jaya Algorithm

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Abstract - This project presents a comparative efficiency optimization of DC-DC power converters using the Jaya and Enhanced Jaya algorithms. DC-DC converters are essential in power electronics, requiring precise tuning of parameters such as switching frequency, duty cycle, inductance, and capacitance to improve efficiency and reduce losses. Traditional optimization methods often face limitations like slow convergence and entrapment in local optima.

The Enhanced Jaya algorithm addresses these issues through a dynamic, adaptive search mechanism that improves convergence speed and global optimization performance. It is applied to various DC-DC converter topologies, targeting key performance metrics including efficiency, output ripple, and transient response.

Simulation results demonstrate that the Enhanced Jaya algorithm consistently outperforms conventional optimization techniques, achieving better parameter tuning and enhanced overall converter performance. This optimization approach shows strong potential for real-world applications in renewable energy, electric vehicles, and industrial power systems.

***Key Words*:** DC-DC Converters, Enhanced Jaya Algorithm, Efficiency Optimization, Power Electronics, Techniques, Transient Response, Renewable Energy Systems

1. INTRODUCTION

The growing demand for high-efficiency power conversion systems has driven significant advancements in DC-DC converter technology. These converters are vital in applications such as renewable energy systems, electric vehicles, and portable electronics. Their performance is influenced by parameters like switching frequency, duty cycle, and component values, all of which must be optimized to enhance efficiency and minimize power losses.

Traditional optimization techniques often struggle to meet the competing demands of efficiency and performance, particularly in complex, nonlinear systems. In response, metaheuristic algorithms have emerged as effective tools for addressing such challenges. Among them, the Jaya Algorithm has gained attention due to its simplicity, ease of implementation, and independence from problem-specific parameters or gradient information. However, its basic form may exhibit slow convergence and suboptimal performance in complex design spaces.

This project introduces the Enhanced Jaya Algorithm (EJA) to optimize key performance metrics—efficiency, power loss, and transient response—across various DC-DC converter topologies. EJA incorporates adaptive improvements to boost convergence speed and solution accuracy. Through simulation and testing, the study aims to demonstrate EJA's effectiveness in delivering robust, energy-efficient converter designs suitable for real-world applications in advanced power electronics.

2. GENERAL DISCRIPTION

The **Enhanced Jaya Algorithm (EJA)** is an advanced metaheuristic optimization technique designed to improve the performance of **DC-DC converters**. It optimizes key parameters like duty cycle and switching frequency to reduce power loss, minimize voltage ripple, and enhance transient response—all without requiring gradient information. EJA improves upon the basic Jaya algorithm by incorporating better exploration and exploitation strategies, ensuring faster convergence and higher solution accuracy.

The algorithm works by:

1. **Initializing** a population of potential solutions,
2. **Evaluating** their performance based on defined objectives (e.g., efficiency),
3. **Iteratively updating** solutions using improved rules, and
4. **Converging** when optimal or near-optimal performance is achieved.

EJA effectively navigates complex design spaces, making it suitable for real-world converter applications that demand high efficiency, stability, and robustness.

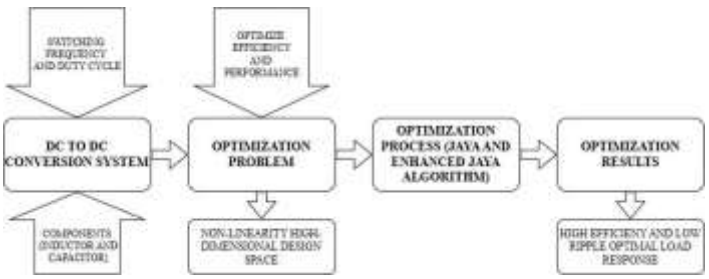
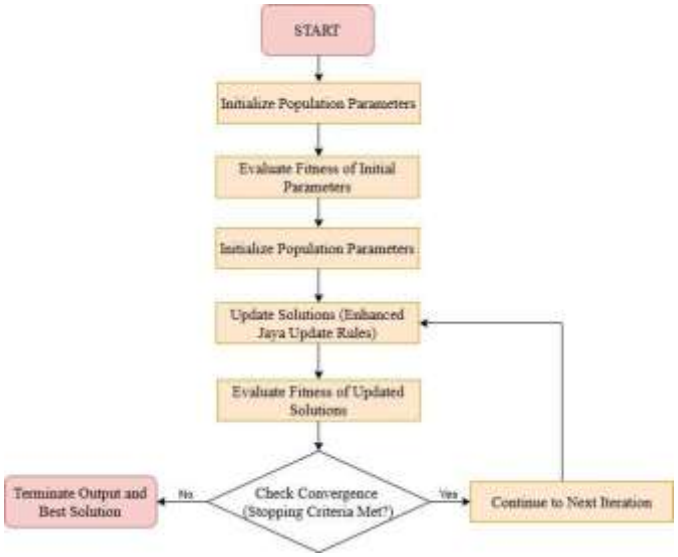


Figure -1: Systematic diagram of DC-DC Converter optimization

3. ALGORITHM AND FLOW CHART



$$Xi(t+1)=Xi(t)+\alpha.r1.(Xbest(t)-Xi(t))-\beta.r2.(Xworst(t)-Xi(t)$$

) Where:

- α and β are adaptive coefficients that influence the update magnitude and allow for more exploration or exploitation based on the current iteration.
- r1, r2: Random numbers in the range [0,1]
- Xi(t): Current solution of i-th individual at iteration t
- Xbest(t): Global best solution at iteration t
- Xworst(t): Worst solution at iteration t

Initialize Population:

Randomly initialize a population of solutions (parameter values for the DC-DC converter).

Evaluate Fitness:

For each solution in the population, evaluate the fitness using the objective function (e.g., converter efficiency, voltage regulation, or ripple minimization.

Find Best and Worst Solutions:

Find the solution with the best fitness value: Xbest Find the solution with the worst fitness value: Xworst **Update**

Solutions:

For each individual Xi in the population, update its position using the Enhanced Jaya update rule:

$$Xi(t+1)=Xi(t)+\alpha.r1.(Xbest(t)-Xi(t))-\beta.r2.(Xworst(t)-Xi(t)$$

)

Termination Condition:

Repeat steps 2-4 until a stopping criterion is met (e.g.,
maximum number of iterations, acceptable performance level, or convergence).

Output:

The algorithm returns the best solution found.

4. OPTIMIZING BUCK-BOOST CONVERTER PARAMETERS USING EJA

I. Design Specifications – Buck Mode (For Example):

- Input Voltage (Vin): 18 V
- Output Voltage (Vout): 12V
- Switching Frequency (fsw): 40 kHz
- Resistance(R):10ohm
- Efficiency (η): 90% (target efficiency)
- Inductor ripple current: 1% of output current (for design purpose)

Manual Calculation Result:

1. Duty Cycle (D)

$$D = \frac{Vo}{Vo + Vin}$$

D = 12/(12+18)
D = 0.4

2. Input Current (Iin)

$$Iin = \frac{Po}{Vs}$$

Iin = 14.4/18
Iin = 0.8 A

3. Output Current (Io)

$$Io = \frac{Vo}{R}$$

Io = 12/10
Io = 1.2 A

4. Inductor (L)

$$Lmin = \frac{R(1-D)^2}{2fs}$$

$Lmin$ = 0.6/80000
$Lmin$ = 0.45µH

5. Inductor Ripple Current

$\Delta IL = Vs.\ D/L.fs$
ΔIL = (18 * 0.4)/(0.0001*40000)
$\Delta IL = 1.8A$

6. Capacitor (C)

$$C = \frac{D}{f_s} . \Delta Vo$$

C = 12 * 0.4/40000 *0.48
C = 20µF

7. Peak Inductor Current ($Ipeak$)

$$I_l\,peak = I_{avg} + \left(\frac{\Delta I_L}{2}\right)$$

$$I_l\,peak = 0.8 + \left(\frac{1.8}{2}\right)$$

$I_l\,peak = 1.7A$

8. Efficiency

$$\eta_{Ideal} = \frac{P_{in}}{P_{out}} = (V_{in} . I_{in})/(V_o . I_o)$$

$$\eta_{Ideal} = \frac{14.4}{15.3}$$

$$\eta_{Ideal} = 94.1\%$$

Enhanced Jaya Algorithm Result:

1. Inductor (L) = 165 µH
2. Capacitor (C) = 40 µF
3. Efficiency = 16%

II. Design Specifications – Boost Mode (For Example):

- Input Voltage (Vin): 18 V
- Output Voltage (Vout): 27V
- Switching Frequency (fsw): 40 kHz
- Resistance(R):10ohm
- Efficiency (η): 90% (target efficiency)
- Inductor ripple current: 1% of output current (for design purpose)

Manual Calculation Result:

1. Duty Cycle (D)

$$D = \frac{Vo}{Vo + Vin}$$

D = 27/(27+18)

D = 0.6

2. Input Current (Iin)

$$Iin = \frac{Po}{Vs}$$

Iin = 72.9/18

Iin = 4.05 A

3. Output Current (Io)

$$Io = \frac{Vo}{R}$$

Io = 27/10

Io = 2.7 A

4. Inductor (L)

$$Lmin = \frac{R(1-D)^2}{2fs}$$

$Lmin$ = 1.6/80000

$Lmin$ = 220 µH

5. Capacitor (C)

$$C = \frac{D}{f} . \Delta Vo$$

C = 2.7 * 0.6/40000 *1.62

C = 47µF

6. Peak Inductor Current ($Ipeak$)

$$I_l\,peak = I_{avg} + \left(\frac{\Delta I_L}{2}\right)$$

$$I_l\,peak = 4.05 + \left(\frac{1.215}{2}\right)$$

$$I_l\,peak = 4.455A$$

7. Efficiency

$$(\eta_{Ideal} = \frac{P_{in}}{P_{out}} = .)/(V . I_{in} I_{in} o o)$$

$$\eta_{Ideal} = \frac{72.9}{74.8}$$

$$\eta_{Ideal} = 97.4\%$$

Enhanced Jaya Algorithm Result:

4. Inductor (L) = 220 µH
5. Capacitor (C) = 67 µF
6. Efficiency = 98.79%

5. CONCLUSIONS

The design of a DC-DC Buck Converter involves selecting the appropriate components based on input/output components specification, optimizing the converter for efficiency, and verifying the design using simulation. You can further optimize the parameters using optimization algorithms lie the Enhanced Jaya Algorithm to improve performance and ensure reliability under varying conditions.

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