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Optimized FIR Filter Architecture Using Vedic Multiplier and Carry Lookahead Adder

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Abstract - The increasing demand for high-performance and low-power digital signal processing (DSP) systems requires efficient arithmetic architectures, particularly in Finite Impulse Response (FIR) filters where multipliers and adders dominate the hardware cost. The existing FIR design utilizes Weinberger adders, composite adders, and Weinberger-based multipliers to achieve improved performance; however, the complex carry-generation structure and multi-stage adder trees lead to higher LUT usage and increased dynamic power. To overcome these limitations, this work proposes an optimized FIR architecture that integrates a Vedic (Urdhva–Tiryagbhyam) 8×8 multiplier and a high-speed Carry Lookahead Adder (CLA). The Vedic multiplier provides fast parallel partial-product generation with reduced logic depth, while the CLA significantly shortens carry propagation delay. The proposed design reduces the number of LUTs, decreases switching activity, and achieves lower dynamic power compared to the existing Weinberger-based structure. Simulation and synthesis results in Vivado confirm that the proposed architecture enhances speed, lowers power consumption, and offers an area-efficient solution suitable for modern low-power DSP applications.

Key Words: Weinberger Multiplier, Weinberger Adder,Vedic algorithm , carry look ahead adder, FIR Filter VLSI architecture and Verilog HDL

1.INTRODUCTION

Finite Impulse Response (FIR) filters are widely used in modern DSP applications where high speed and low power are essential. However, conventional FIR architectures that rely on Weinberger adders and multipliers often suffer from complex carry-generation structures, increased logic depth, and high LUT utilization. These limitations lead to higher delay and dynamic power, making them unsuitable for compact and energy-efficient systems.To address these challenges, recent arithmetic techniques such as Vedic multipliers and fast carry-propagation adders offer promising improvements. The Urdhva–Tiryagbhyam–based Vedic multiplier provides parallel partial-product generation, while the Carry Lookahead Adder (CLA) significantly reduces carry delay. Motivated by these advantages, this work proposes an optimized FIR architecture that integrates an 8×8 Vedic multiplier and a high-speed CLA. The proposed design reduces hardware complexity, lowers dynamic power, and achieves higher speed compared to existing Weinberger-based implementations, making it suitable for modern low-power DSP applications.

2. LITERATURE SURVEY

Vedic Mathematics is an ancient system of mathematics that offers simple and efficient algorithms for various arithmetic operations. The Vedic multiplier is derived from the "Urdhva Tiryakbhyam" sutra, which enables fast multiplication by breaking down complex multiplication into smaller, simpler operations. Vedic multiplication utilizes parallel processing, which allows for faster computation compared to traditional multiplication algorithms.The Carry Look ahead Adder (CLA) is a parallel prefix adder that significantly reduces carry propagation delay by using a tree structure to generate carries in parallel. The CLA operates in logarithmic time with respect to the number of bits, making it much faster than the RCA for large-bit-width addition. The adder has a more complex structure than traditional adders but offers substantial speed improvements, particularly in high-performance computing applications

3. EXISTING DESIGN(FIR Filter using Weinberger Adder Weinberger Multiplier)

Conventional FIR filter architectures rely heavily on arithmetic units such as adders and multipliers, as these blocks dominate the computation of multiply–accumulate (MAC) operations. The existing FIR design under consideration employs **Weinberger adders** and **Weinberger-based multipliers** to perform coefficient multiplication and accumulation

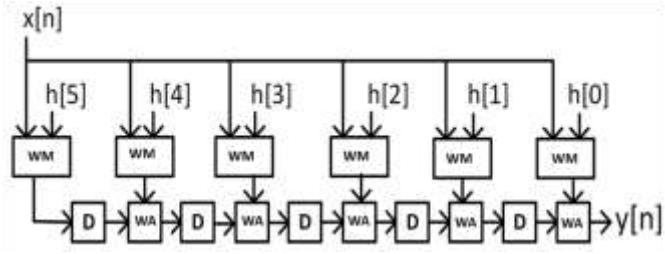

Fig 1: FIR filter using Weinberger Multiplier and Weinberger adder

Weinberger Adder Architecture

The Weinberger adder is a fast carry-propagation adder that uses a hierarchical generate–propagate structure to reduce the overall carry delay. It divides the input operands into smaller groups, computes group generate/propagate signals, and combines them using multi-level carry logic. Although this structure improves theoretical speed compared to ripple-carry adders, it introduces large fan-in gates and complex carry-computation networks. On FPGA implementations, these multi-level logic blocks require additional LUTs, leading to increased area and switching activity.

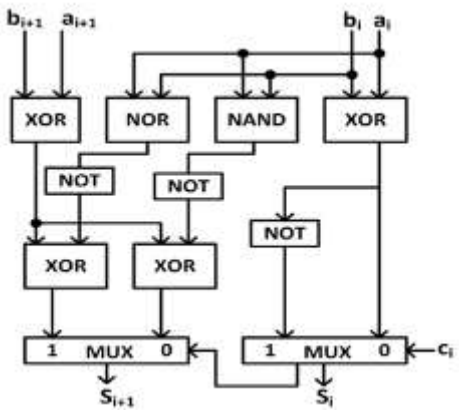

Fig 2: Weinberger Adder

Weinberger-Based Multiplier

The existing multiplier architecture extends the Weinberger addition concept to generate partial products and combine them using composite adder structures. While it maintains uniformity with the adder logic, the multiplier results in:

- Large partial-product adders,
- High carry-generation complexity,
- Multi-stage cascaded logic,
- Increased LUT consumption,
- Higher dynamic power due to extensive switching activity.

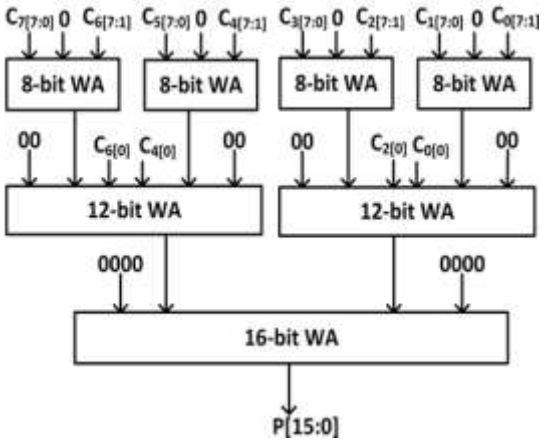

Fig 3: Weinberger Multiplier

Despite achieving functional correctness and reasonable throughput, the existing FIR design suffers from several drawbacks:

- **High LUT utilization** caused by multi-level carry-generation hardware.
- **Longer critical path delay** due to deep, serial adder structures.
- **Increased dynamic power consumption** because of high switching in composite adder trees.
- **Higher routing complexity**, especially on FPGA devices with dedicated carry-chain primitives that are underutilized by Weinberger logic.

These limitations motivate the need for a more power-efficient and area-optimized arithmetic architecture, forming the basis for the proposed Vedic multiplier and Carry Lookahead Adder (CLA) integration

4. PROPOSED DESIGN (FIR Filter using Vedic Multiplier and Carry Look ahead Adder)

The proposed FIR filter implements each multiply–accumulate (MAC) operation using an 8×8 Vedic multiplier followed by a CLA-based adder for accumulation. Partial products for each input–coefficient pair are generated in parallel by the Vedic multiplier; their outputs feed a CLA tree (or a cascaded hierarchy of CLAs) to form the adder-accumulator stage. Where multiple partial products must be summed (e.g., within pipelined MAC stages or across taps), the CLA hierarchy replaces the composite adder tree used in the baseline. The design is modular: an 8×8 Vedic multiplier block, n-bit CLA modules (parameterizable), pipeline registers, and control logic.

To overcome the limitations of the existing design, a Carry Look ahead Adder (CLA) is incorporated into the Vedic multiplier design. The key advantage of the Carry Look ahead Adder is its parallel carry propagation, which significantly reduces the power and area .

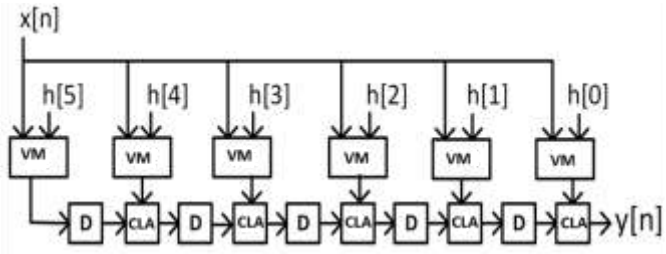

Fig 4: FIR Filter using Vedic Multiplier and Carry Look ahead Adder

Steps involved in the Modified Vedic Multiplier Design:

1. Partial Product Generation:
   - As with the traditional Vedic multiplier, partial products are generated by multiplying each bit of the two operands. The Vedic multiplication method decomposes this into smaller, more manageable parts, making the process faster.
2. Partial Product Addition using Carry Look ahead Adder:
   - Instead of using a Ripple Carry Adder, the partial products are added using the Carry Look ahead Adder .
   - The Carry Look ahead Adder uses a parallel prefix structure to generate carry signals simultaneously, reducing the carry propagation time.
   - The adder employs a series of prefix operations that compute the sum in a logarithmic time complexity, making it much faster than the Ripple Carry Adder for large bit-widths.
3. Final Product Generation:
   - After the addition step is completed using the Carry Look ahead Adder , the final product is generated by combining the sums obtained from the partial product addition.

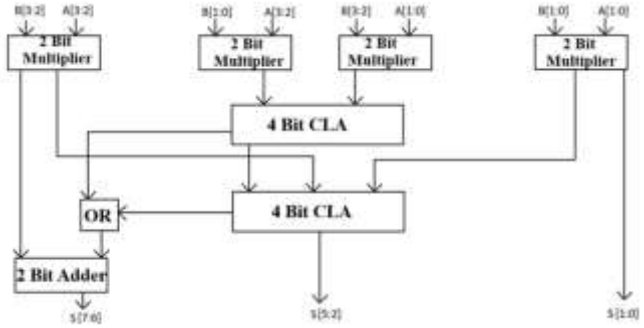

Fig 5: 4 Bit vedic multiplier using CLA

The mode used by Vedic multiplier is Vedic mathematics. By using this technique it will increase, and consumes fewer hardware elements. The sutra used by Vedic multiplier is Urdhva Tiryakbhyam which means Vertically as well as Crosswise. The Fig. shows block diagram of 4 bit vedic multiplier circuit. The2 input bits are separated into 2 similar parts the vertical and cross product calculations can be done as shown in Fig, with inputs A[3:0] and B[3:0].As shown in the Fig. the 2 adders are used in the design of intermediate stages of the addition.The output carry Cout from these two adders is given as input to another CLA. If bits are not of equal sizes concatenate them.For 4-bit Modified Vedic multiplier the outputs of parallel adder is given to OR gate and of the size of last CLA is reduced to half

Carry Lookahead Adder (CLA)

To reduce the computation time, there are faster ways to add two binary numbers by using carry lookahead adders. They work by creating two signals P and G known to be Carry Propagator and Carry Generator. The carry propagator is propagated to the next level whereas the carry generator is used to generate the output carry ,regardless of input carry. The block diagram of a 4-bit Carry Lookahead Adder is shown here below -

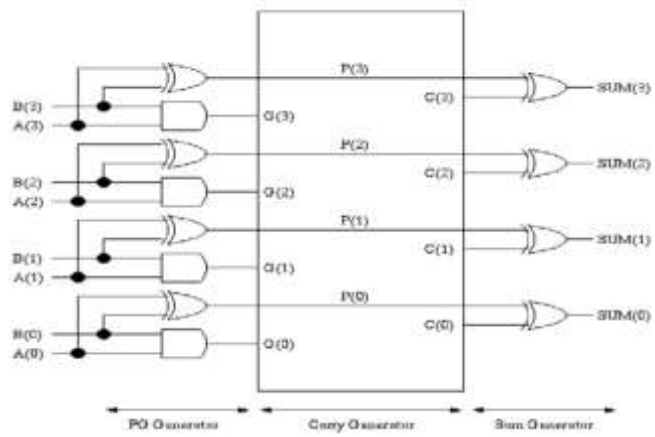

Fig 6: 4bit Carry Lookahead Adder

5. RESULTS

- **RTL SCHEMATIC:-** The RTL schematic is abbreviated as the register transfer level it denotes the blue print of the architecture and is used to verify the designed architecture to the ideal architecture that we are in need of development .The hdl language is used to convert the description or summery of the architecture to the working summery by use of the coding language i.e verilog ,vhdl. The RTL schematic even specifies the internal connection blocks for better analyzing .The figure represented below shows the RTL schematic diagram of the designed architecture.

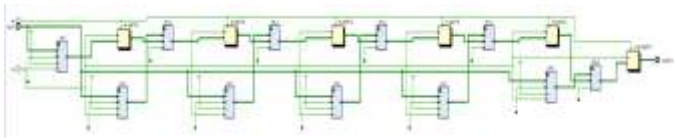

Fig 7: RTL Schematic of existing design

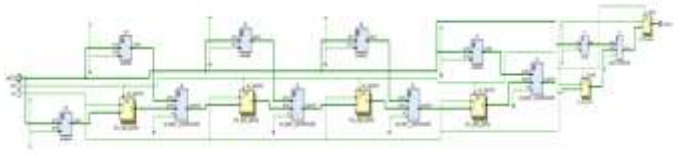

Fig 8: RTL Schematic of proposed design

SIMULATION: -The simulation is the process which is termed as the final verification in respect to its working where as the schematic is the verification of the connections and blocks. The simulation window is launched as shifting from implantation to the simulation on the home screen of the tool ,and the simulation window confines the output in the form of the wave forms. Here it has the flexibility of providing the different radix number systems

Fig 9: Simulated wave form of existing design

Fig 10: Simulated wave form of proposed design

TECHNOLOGY SCHEMATIC:- The technology schematic makes the representation of the architecture in the LUT format ,where the LUT is consider as the parameter of area that is used in VLSI to estimate the architecture design .the LUT is consider as an square unit the memory allocation of the code is represented in there LUT s in FPGA.

Fig 11: Technology schematic of exiting design

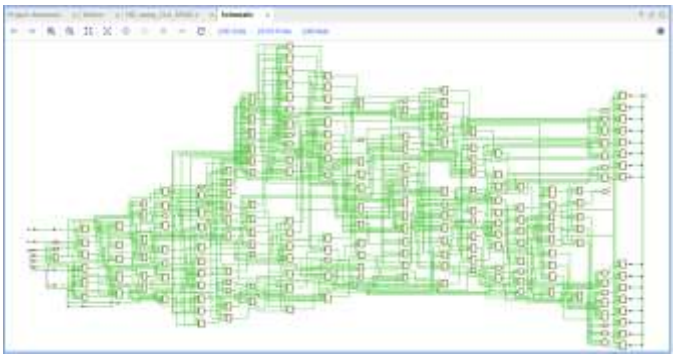

Fig12: Technology schematic of proposed design

PARAMETERS:-Consider in VLSI the parameters treated are area and power ,based on these parameters one can judge the one architecture to other.

Table 1 : Parameter comparison

Parameter	Existing design	Proposed design
No of LUTS	93	86
Power(mW)	16.186	15.912

Fig 13: LUT and Power comparison bargraph

CONCLUSION

The proposed FIR filter architecture using an 8×8 Vedic multiplier and a high-speed Carry Lookahead Adder (CLA) effectively overcomes the limitations of the existing Weinberger-based design. By reducing logic depth and improving carry propagation, the architecture achieves lower LUT usage, reduced dynamic power, and higher computational speed. Vivado results confirm that the optimized design is more efficient and better suited for modern low-power DSP applications.The design can be further enhanced by extending the multiplier to higher bit-widths, incorporating deeper pipelining for high-speed systems, exploring ASIC-based implementation for improved efficiency, and integrating the architecture into adaptive or machine-learning-oriented DSP systems.

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