International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 06 Issue: 06 | June - 2022 Impact Factor: 7.185 ISSN: 2582-3930

OPTIMIZED IMPLEMENTATION OF REVERSIBLE PRIORITY ENCODER USING NANO QCA

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Abstract

Quantum-dot cellular automata (QCA) is a possible replacement for complementary metal–oxide–semiconductor technology (CMOS). With the help of reversible computing, it is possible to attain zero power dissipation. The design of a reversible priority encoder based on QCA is proposed in this work. Peres and BJN gates are the design's foundational elements. The QCA designer simulator verifies the suggested design. The performance analysis is implemented based on the simulation results. The proposed encoder reduces the amount of heat energy dissipation, producing quality data also solving the problem of the jumbled data. The proposed reversible circuit has the potential to be a game changer. Since reversible logic circuit provides zero information loss, it will be a key component in future wireless communication. The estimated energy dissipation of suggested QCA circuits is investigated, implying that QCA could be a suitable platform for implementation of Reversible circuits.

Keywords - *Quantum dot Cellular Automata(QCA), Reversible logic , priority encoder.*

I. INTRODUCTION

In nano scale logic design, power consumption is the most challenging area[5]. Hence, there is a raising requirement for a new technology that can provide nano size circuits having lesser power dissipation. This need is satisfied by QCA Technology[8]. QCA offers high device density, low power consumption and high switching speed[6]. Due to these properties quantum gates have been targeted for their enabling roles towards computational reversibility. Irreversible computing do not conserve information and dissipation of heat is high. This limitation is the main driving force which draws the attention of reversibility.

FUNDAMENTALS OF QCA

A. QCA CELL

In contrast to electronics based on transistors, QCA does not operate by the transport of electrons, but by the adjustment of electrons in a small limited area of only a few square nanometers[26]. QCA is implemented by quadratic cells, the so-called QCA cells. In these squares, exactly four potential wells are located, one in each corner of the QCA cell (see figure 1.1). In the QCA cells, exactly two electrons are locked in. They can only reside in the potential wells.

The potential wells are connected with electron tunnel junctions. They can be opened for the electrons to travel through them under a particular condition, by a clock signal. Without any interaction from outside, the two electrons will try to separate from each other as far as possible, due to the Coulomb force that interacts between them. As a result, they will reside in diagonally located potential wells, because the diagonal is the largest possible distance for them to reside.

A basic QCA cell consists of four quantum dots in a square array.

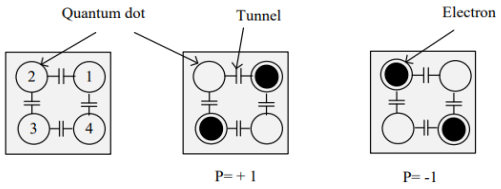

Figure 1.1 QCA cell

Electrons occupy two dots in the furthest site due to mutual electrostatic repulsion. In QCA, logic values are stored based on electron's charge rather than electrical pulse like in CMOS[25].

B. QCA Clocking

The QCA clock has four different phases[27]. In the first phase, known as Switch, the QCA cells start depolarized with the tunnelling potential barriers low. During this phase, the bar lies between the dots are progressively increased and the cells start to polarize according to the state of their drivers. The actual computation is made exactly at this phase. At the end of the first phase, the barriers are high enough to avoid the tunnelling to fix the state of the cells. During the Hold phase, the cells have fixed states as the barriers are kept high. So they can be used as inputs to the next stage. In the Release phase, the barriers are lowered and the cells are allowed to relax to a depolarized state. Finally, Relax phase and the barriers are kept low and the cells remain depolarized.[22]

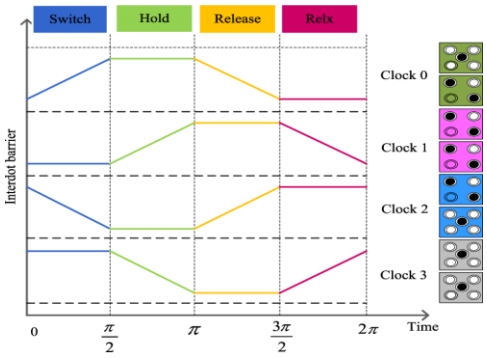

Fig.1.2 Clock Phase shift in QCA

Table 1 Operation of QCA clock phases

Clock pulse	Potential Barrier	Polarization state of the cells
Hold	Held High	Polarized
Switch	Low to High	Polarized
Relax	Low	Polarized
Release	Lowered	Polarized

C. Reversible Computing

Certain amount of energy is wasted when the input bits are destroyed. Reversible logic circuits, avoid energy waste by recovering the energy into the system. Bennet proposed that very low power consumption is possible in logic circuits when it is combined with logic gates.[19]

The list of contribution of Reversible computing is as follows.

- The building blocks of a reversible system should be individually reversible.
- The number of inputs and outputs has to be always equal.

Reversible computation analyze the ratio between consumed energy and logical computation. It can be established at logical level by one to one layout between input and output of the circuits.

To prevent the destruction of data bits during logical operation, they are designed to reduce power consumption. The data bits in reversible computation are preserved that lead to the development of reversible gate.

The reversible gate should have the following characteristics,

• Minimum garbage outputs.

• Minimum input constants.

• Minimum area.

• Minimum number of gates.

Several reversible gates have been developed. Two important types are Toffoli and Fredkin gate.

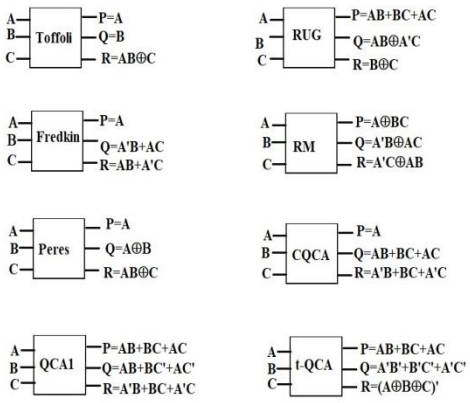

Fig.1.3 Reversible gates

II. REVERSIBLE PRIORITY ENCODER

To date there are many works on priority encoder design in QCA. In [1], a priority encoder is designed using Toffoli and BJN gates with reversible logic. However, this design has 511 cells and area of 0.72μm^2 with Quantum cost of 25.92. Hence an optimized design of the reversible priority encoder is proposed with its QCA layout. The proposed design is performed based on two universal reversible logic gates; those are,

(i) Peres and (ii) BJN gate.

a. Peres gate

Peres gate is a 3x3 reversible gate. This gate is universal in the sense it can synthesize any arbitrary Boolean function. It can thus be used to implement all the basic Boolean functions. The Quantum cost is 4. The gate has three inputs *I(A, B, C)* and three outputs *O*(P = A, Q = A⊕B, R = (AB)⊕C). The Fig. 2.1 represents the logic of Peres gate with its output.

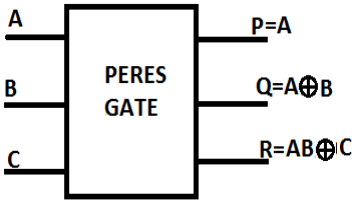

Fig.2.1 Block diagram of Peres Gate

Table 2 Truth Table of Peres Gate

INPUT			OUTPUT		
A	**B**	**C**	**P**	**Q**	**R**
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

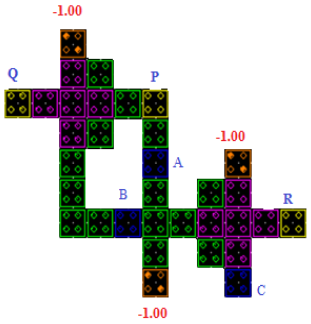

Fig 2.2 QCA Implementation of Peres Gate

b. BJN gate

BJN gate is a 3x3 reversible gate. BJN gate is also known as modified TG. BJN gate consists of three inputs and three outputs. The quantum cost of the BJN gate is 5. The design of the proposed QCA circuit of the BJN gate is given in Fig.4.5 and its block diagram in Fig. 4.5 The inputs are (A,B, C) and outputs are (P = A, Q = B, R = (A + B)⊕C)). Its truth table is given in Table 4.2.

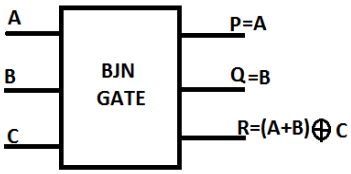

Fig 2.3 Block Diagram of BJN gate

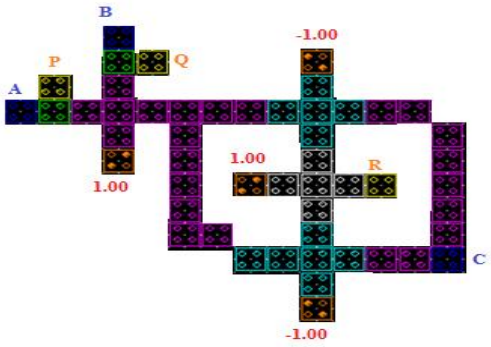

Fig 2.4 QCA Implementation of BJN Gate

Table 3 Truth Table of BJN Gate

INPUT			OUTPUT		
A	**B**	**C**	**P**	**Q**	**R**
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	1	0

A priority encoder is a logic circuit that is able to reduce multiple binary inputs to a smaller number of outputs [4]. All the outputs always should be in the binary representation of given inputs of this circuit. The most significant bit of input acts as the highest priority interrupt request. If two or more inputs are given at a time then the highest priority will take precedence. The input vectors of this circuit are as follows: (*D*0, *D*1, *D*2, and *D*3) and the outputs are:

$$Y1 = (D3 + D1D2')$$

$$Y0 = (D2 + D3)$$

and the output indicator is

$$Z = (D0 + D1 + D2 + D3).$$

Table 4 Truth table of Priority Encoder

D3	D2	D1	D0	Y0	Y1	Z
0	0	0	0	X	X	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

The proposed Reversible Priority Encoder is designed by modifying Peres and BJN gates. There are five functional blocks which include one Peres and four BJN.

Fig. 2.5 and 2.6 represents the Block Diagram and QCA implementation of proposed Reversible Priority Encoder respectively.

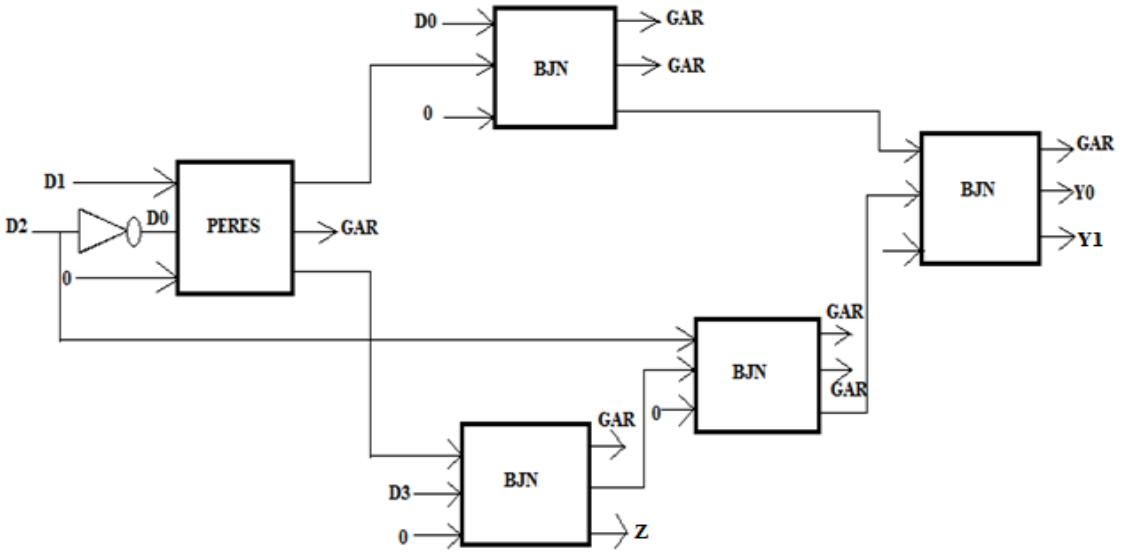

Fig 2.5 Block diagram of Reversible Priority Encoder

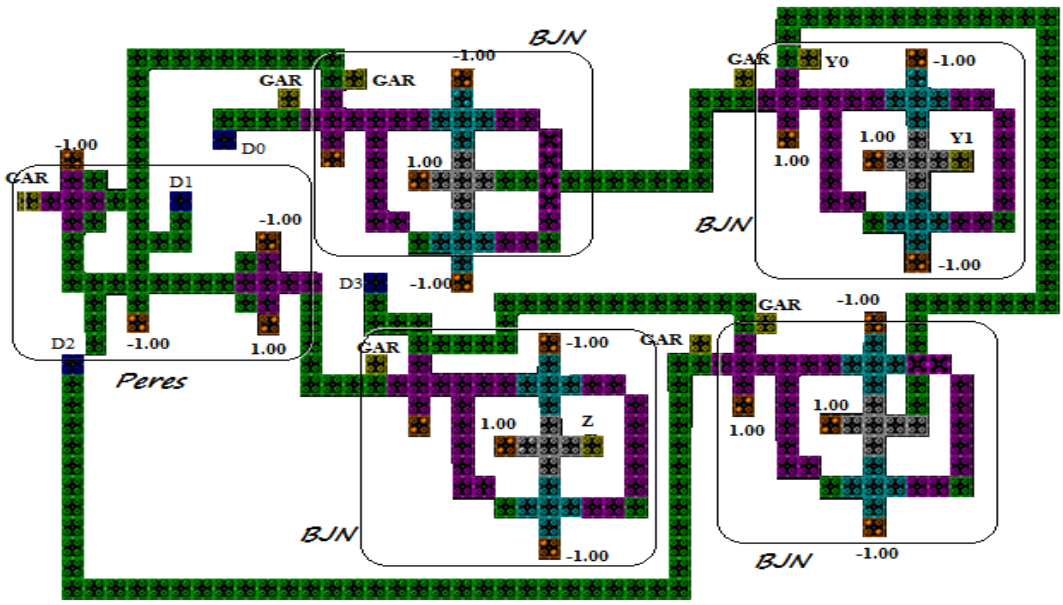

Fig 2.6 QCA Implementation of Reversible Priority Encoder

All the simulations are carried out using QCADesigner software package. QCA designer offers two types of simulations viz. coherence vector and bi-stable approximation. In the proposed design, bistable approximation simulation is used. The cell size used to simulate is 18 × 18 nm. The proposed encoder has four constant inputs, seven numbers of garbage outputs and three constant outputs as in Fig.2.5. The outputs of the QCA layout of Peres and BJN gate including the proposed reversible priority encoder is verified with the truth table by using a bi-stable approximation simulation engine. The QCA implementation of Peres and BJN gate are shown in Figs.2.2 and 2.4, respectively.

III. RESULTS AND DISCUSSION

The proposed Reversible Priority Encoder is implemented using QCADesigner tool as shown in Fig 2.6 and the simulated results are obtained as in Fig 3.1

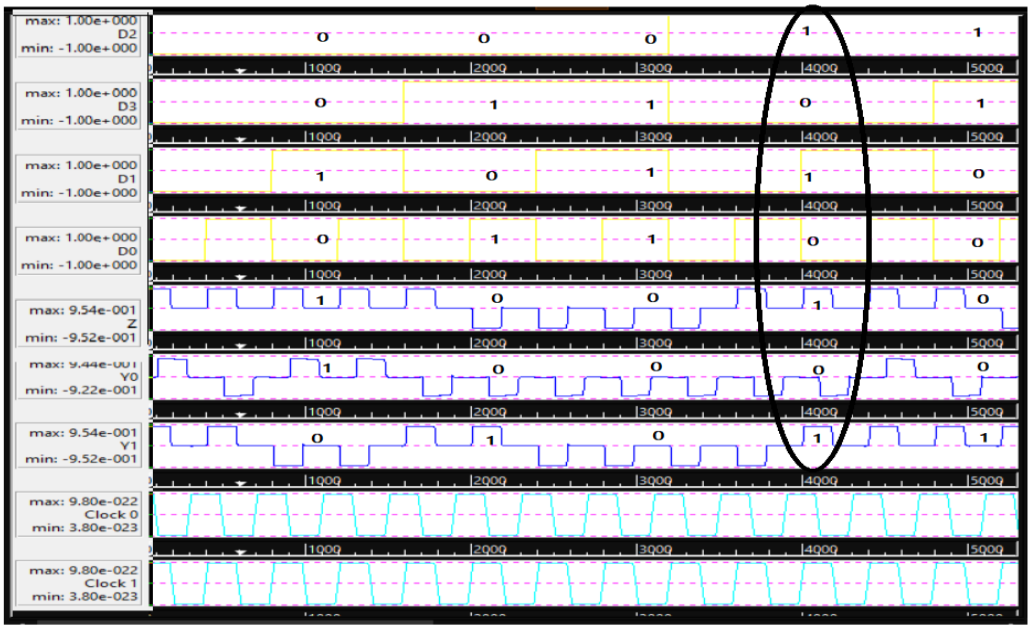

Fig 3.1 Simulation result of proposed reversible priority encoder in QCADesigner

The total energy dissipated and average energy dissipated for the individual gates such as Peres and BJN and also for the proposed Priority Encoder has been calculated and tabulated as shown in table 4.

GATE	Total energy dissipated	Average energy dissipated
Peres gate	3.56 e – 002eV	3.24 e – 003 eV
BJN gate	1.98 e – 002eV	1.80 e – 003 eV
Reversible Priority encoder	1.58 e – 001 eV	1.44 e – 002 eV

Table 4 Energy dissipation of the model

The number of cells required to design the individual gates and the proposed model together are calculated based on the simulation tool and corresponding factors such as Area, Delay and Quantum cost the individual gates and the model are calculated and tabulated as shown in table 5.

Table 5 Circuit complexity of the model

Circuit	No. of cells	Area (μm^2)	Delay	Quantum Cost
Peres	44	0.05	0.5	2.50
BJN	51	0.07	1	1.75
Reversible Priority Encoder	389	0.55	4.5	24.75

Circuit complexity of QCA layout:

The circuit of Peres as well as the BJN gate has 248 cells, 0.33 μm^2 areas, 1.5 clock delay, and quantum cost of 4.25. The priority encoder circuit has 389 cells, 0.55 μm^2 areas, quantum cost of 24.75, and takes 4.5 clock cycle delays to get the output. Table 6 represents the comparison of existing and proposed design.

Table 6 Existing versus proposed

Reversible Priority Encoder	Cell count	Area (μm^2)	Delay	Crossover
Existing [1]	511	0.72	6	Multi layer
Proposed	389	0.55	4.5	Coplanar

IV. CONCLUSION

In this project, the new QCA computation of reversible priority encoder was designed and implemented by using the new QCA implementation of Peres and BJN gates. The functionality of the circuit is tested by QCADesigner software package and the operation of circuit has been verified according to the truth table. All the circuits have lower heat dissipation. The circuit cost has been explored to indicate its design cost. During encoding, loss of information can be prohibited due to the reversible nature of the circuit. So it can be applied to wireless sensors communication, digital signal processing, in various parallel circuits. The reversible logic circuit can be used in application for enabling storage.

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