International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 06 Issue: 09 | September - 2022 Impact Factor: 7.185 ISSN: 2582-3930

PARAMETER ANALYSIS OF SRAM CIRCUIT

Deepti Sagar[1], Er. Thakurendra Singh[2]

Electronic & Communication Engineering, RBS Engineering Technical Campus Agra[1]

Electronic & Communication Engineering, RBS Engineering Technical Campus Agra[2]

Abstract: The study examined the different a number of power-saving strategies, including sleep, stack, sleep stack, transmission gate logic, or self-controllable voltage level-upper (SVL-U). These methods are used with SRAM cells that have 6 transistors (6T), 7 transistors (8T), 8 transistors (9T), and 10 transistors (10T). The SVL-U method and transmission gate logic are used in suggested SRAM cell. According to a comparison of SRAM memory array as well as cells, dynamic power is significantly decreased on average when compared to traditional methods. The 45nm and 90nm software applications from Cadence are also used for simulation. According to a thorough analysis of SRAM memory arrays and cells, PDP and EDP have, on average, been significantly decreased when contrasted the state-of-the-art hybrid VLSI techniques. Therefore, these SRAMs are suitable for extremely low power embedded structural appliances.

Keywords: Semiconductor Memories, Memory organization, SRAM, Write operation, Read Operation.

I.INTRODUCTION

Improving yield is a main objective for semiconductor manufacturers because it defines a new process's readiness for high volume manufacturing [1]. However, these companies are facing significant new challenges in the design and manufacturing of modern integrated circuits as they become denser and smaller sizes as critical measurements continue to shrink with the implementation of novel technology nodes [2]. One of these challenges is the increased complexity of

the conceptual design rules, which makes the cells in an integrated circuit (IC) extremely vulnerable to

physical abnormalities. As a consequence, effective failure investigation is essential.

Embedded memories, particularly SRAM cells, frequently take up a large portion of the area of a typical system-on-chip (SOC) [3]. As a result, the SRAM cell area must meet very strict area specifications, pushing the layout design rules to their boundaries. The output of SRAM cells indicates the dependability of a particular technology node's layout design regulations. It also provides a good indication of the yield of ICs developed at that technology node.

II. Working of 6T SRAM Cell

The 6T SRAM cell consists of a pair of weakly cross coupled inverters that hold the condition as well as a pair of access transistors that read and write the states[3]. The write procedure is carried out by inserting the desired value and its complement into the bit lines bit and bit b, then elevating the word line word. The information is overpowered by using cross coupled inverters. The two bit lines' pre charging is first set to high and then allowed to float. When word is elevated, bit b is pulled down, indicating the data value. The greatest difficulty of SRAM is to guarantee that the circuit holding the state is weak enough even to guarantee the write operation by overwhelming the previously stored value while also being strong enough already to preserve it during the read operation.

Both of these should be guaranteed for proper READ and WRITE processes. The function of SRAM is divided into two phases. Let's call the two phases ϕ1 and ϕ2. These are typically generated by clk (clock) and its supplementary clkb. Allow the circuit illustrated in the figure 1.

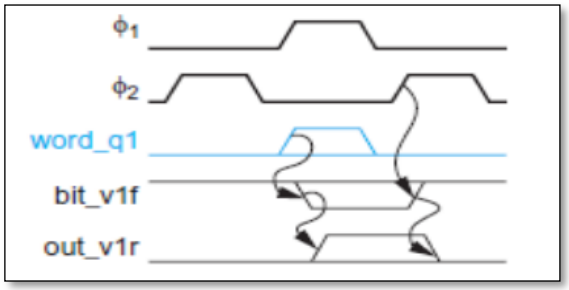

Figure.1 Pre-charge circuit [3]

The read as well as write operations are carried out in Phase 1. Our primary concern here is phase 1 of the SRAM cell. The precise definition of 6T SRAM is depicted in the figure below. 2[3]

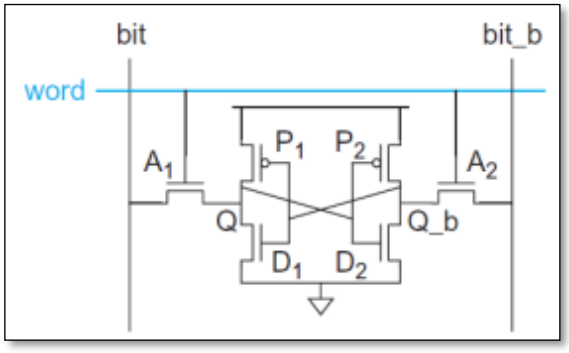

Figure.2 Detailed structure of 6TSRAM cell [4]

Authorization transistors A1 and A2 are linked to bit and bit b, respectively, allowing us to read from or write to the memory. If the word line is set to 1, researchers could indeed access the connect transistors and thus undertake read & write operations. If the word line is equal to zero, transistor access is disabled as well as memory is in the hold state[3]. The access transistors A1 and A2 are turned off in stand by (or) hold mode (i.e., word line=0). As a result, the data will remain unaffected as long as SRAM is in this mode [4]. To write into the memory bit, bit b serves as input, and also to read from the memory bit, bit b serves as output.

This paper describes a method for analyzing power reduction in an SRAM cell. Using 45 nm and 90 nm technology device models and layout rules, a typical 4 and 6-transistor SRAM cell was developed. predict whether a cell is healthy or defective, as well as the type and placement of the deficiency. This paper is organized as follows. Section II describes how the SRAM Functional Mode. In section III gives the literature survey of the proposed work, Section IV explains the objectives and motivation for proposed work. In Section V, simulation results are shown.. Section VI presents the conclusion.

II. BACKGROUND: SRAM FUNCTIONAL MODE

The addressing pattern in random access memories during functional mode is unexpected. As a result, all bit lines must be pre-charged (to VDD) in order for all array rows to be ready for the new operation. When a cell is chosen for a read/write operation, the corresponding pre-charge circuit is normally turned off for the duration of the procedure. The pre-charge circuit is commonly left ON for columns that are not involved in the operation, and the corresponding cells undergo a stress known as RES (Read Equivalent Stress) [5].

- **SRAM trends**

SRAM's limitation is cell size. Because SRAM contains 50-90% of the chip's transistors, area decrease is a significant concern in the design SRAM. Reduced area also allows for the creation of a larger memory. Minimizing standby power consumption (leakage power) is particularly useful for mobile devices, where leakage drains the battery when the circuit is idle for an extended period of time. Future servers will require speed increase. So, a SRAM bit-lines consume a significant amount of power. Another trend to enhance efficiency is charge sharing as well as efficient bit-line pre-charging. Some other trend for enhancing SRAM is the use of dual threshold to reduce leakage. Data stability should be considered during

any advancement. Instruction memory in SRAM is several megabytes in size. A single bit change can affect all success and make the operating system unstable.

- **Read mode**

In SRAM, the word line must be high in order for any operation to be conducted. To conduct a read operation, memory must first contain some value. As an example, suppose memory has Q=1 and Q'=0. Raise the word line to the highest setting to accomplish the read operation. Bit as well as bit b serve as output lines, and are initially pre-charged, with a node voltage Vdd at bit and bit b. There is no discharge in the circuit because Q and bit are both high. Because Q' is 0, there will be a voltage difference between Q' and the node current at bit b, causing the bit b voltage to fall. As a result, the circuit will release as well as current will flow. Bit as well as bit b are linked to a sense amplifier, which acts as a comparator, so when bit' is low, the output is 1. As a result, input Q=1 and output 1, read operation verified. Recognize Q=0 as well as Q'=1 in the memory in the same way. Because there is a reference voltage, there would be a discharge in the circuit at Q and bit. The transistors must have a ratio so that Q is less than the P2/D2 threshold area. This is known as read restriction. The output will be 0 as the bit voltage drops. When the input Q is 0, the output is 0[6]. As a result, the read procedure is validated in both instances. The output waveforms for READ operations are depicted in the figure 3 below.

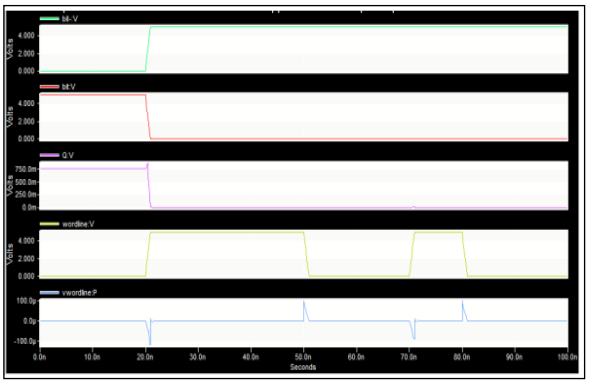

Figure 3: Read operation

- **Write mode**

Recognize the memory bits, which are Q=0 and Q'=1. Because the word line is remarkably high, a write operation could be conducted. Bit and bit' are input lines in the write operation. As we have control over the bit lines, connect bit b to ground at first so that we could measure the voltage difference between Q' as well as bit b. D2 should be greater than P2 in order to write 1 into the SRAM cell; this could be accomplished by changing the aspect ratio of the transistors[7]. As a result, Q would be 1. Originally, Q=0 after the operation, so we effectively write into memory. Figure 4 illustrates the output waveform.

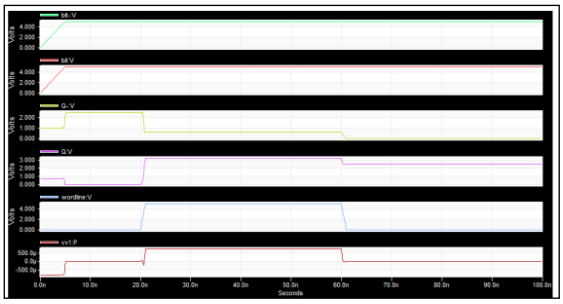

Figure 4: Write operation

III.LITERATURE SURVEY

Chunn et al.,(2020) The efficiency of an SRAM cell based on the Dynamic Threshold Voltage MOSFET method is examined in the sub-threshold zone. The cell uses 8 transistors in total, including access transistors based on transmission gates. The 45nm GPDK is used in simulations on the Cadence Virtuoso tool in the sub-threshold voltage range. The suggested cell has an 80 percent decrease in read access time, a 63.95 percent reduction in write "1" access time, and a 22.7 percentage reduction in write "0" access time when compared to the traditional 6T SRAM cell. Additionally, the suggested cell has a 360% increase in Write Static Noise Margin (WSNM). However, it is seen that the energy consumption rises by 400 percent when the action is read, by 221.4 percent when the operation is write "0," and by 458.4 percent when the operation is write "1."

Sharma et al.,(2021) A new 10T SRAM cell using FinFET is available at various techniques. With a 10T CMOS cell, 45nm and 32nm technologies are thoroughly compared. Various SRAM factors, including power, static noise margin (SNM), and latency, are taken into account for analysis purposes. FinFET-based SRAM cells outperform CMOS-based cells in terms of hold and read static noise margins (HSNM, RSNM) by 31% and 29% at 45nm and 41% and 50% at 32nm, respectively. At a temp of 25°C and a power supply of 0.5v, calculations have been run on the HSPICE tool.

Panguluru et al.,(2020) To increase noise limits, a seven transistor (7T) cell with a 7nm feature size is suggested. The Predictive Technology Model (PTM) 7nm model card is utilized in the suggested design, while Cadence Virtuoso is used for all simulations. The suggested technology's Static Noise Margin (SNM), Read Noise Margin (RNM), and Write Noise Margin (WNM) are each 210mv, 210mv, and 145mv, accordingly. A 1-bit cell with an estimated area of 0.0291 m2 has read and writes times of 5 ps and 17.6 ps, respectively.

Pal et al.,(2021) showed and contrast the efficiency of a binary DNN using high-K and low-K stacked RRAM that is suitable with 32nm technology nodes with CFET-SRAM and MRAM. For use in synaptic memory, researchers have created heterogeneous stacked RRAM using Sidoped Al2O3 and Ta2O5 as stacked layers. The instrument displayed an extreme on/off ratio of 4.2 x 103 and an extremely low variance of 6E-07 S. The NN was trained with a baseline accuracy of 97.11 percent, and the effects of conductance and read noise variation were assessed. Authors also measured the effectiveness of our device to CFET-SRAM and MRAM technologies from previous works and found that our devices performed more accurately and efficiently.

Gauchi et al.,(2019) To tile an SRAM/IMC-based architecture and scale the memory needs in accordance with an application set, put forth a new methodology. We extract the IMC memory needed for a particular class of applications using a high level LLVM-based simulation platform. The physical and performance costs of tiling SRAM instances are then described. Authors examined the performance, energy consumption, and cost of memory interconnects by investigating multi-tile SRAM Place & Route in 28nm FD-SOI. As a consequence, we are able to analyze trade-offs related to memory sizing thanks to a detailed wire costing system. Through dividing the memory into several sub-tiles, we can create an IMC tile with a big capacity while using up to 78% less energy and up to 49% more speed than a single large IMC memory.

Vernekar et al.,(2019) uses the Replica-Bit-Line (RBL) method, a traditional method, to create a self-timed SRAM control circuit that monitors timing changes as well as produced control logic. To guarantee successful read and write operation of SRAM at low voltages, a variable word line system is suggested. The 65 nm UMC-designed 2 Kb (2048 bits) SRAM works at 50 MHz with a supply voltage of 0.58 V as well as at 1 GHz with a nominal supply voltage of 1.2 V. When compared to the traditional RBL method, the variances in the Sense Amplifier Enable (SAE) generation are reduced by up to 92 percent.

Shah et al.,(2018) To counteract the loss caused by NBTI ageing, an on-chip adaptive body bias (O-ABB) circuit is developed. In terms of read current, hold SNM, read SNM, write margin, and word line write margin, the SRAM circuit yield is improved by using the O-ABB. The body bias control circuit, decision circuit, and standby leakage current (Iddq) sensor circuit make up the O-ABB. For pre and post stress of 10 years of NBTI ageing, circuit level simulation for SRAM cell is carried out. The suggested O-ABB lessens NBTI's impact on the stability of the SRAM cell. In the absence of O-ABB, the simulation results show that hold SNM, read SNM, and WLWM decrease by 10.55 percent, 8.55 percent, and 3.25 percent, respectively. However, if O-

ABB is used to mitigate the degradation, hold SNM, read SNM, and WLWM decrease by only 0.47 percent, 1.15 percent, and 0.62 percent, in both.

Surana et al.,(2018) A single ended 6-T (SE6T) SRAM cell with the same bit error rate as a standard 6-T SRAM cell is suggested. It has around 50% less dynamic power. Since image processing applications are error-tolerant, storage could be provided by extremely low voltage, power-efficient embedded memory with BER. Designers demonstrated that for a similar peak signal to noise ratio, 1 KB (256x32) SE6T memory uses 0.45 dynamic power, 0.83 leakage power, and 0.60 area less than traditional 6T SRAM memory . Also suggested heterogeneous SE6T 1K SRAM memory and shown that it improves PSNR by at least 14 dB when contrasted to homogeneous (using equally sized bit-cells) SE6T SRAM memory for a given power budget. In comparison to heterogeneous 6T SRAM memory, heterogeneous SE6T SRAM memory uses 0.6 area, 0.86 leakage power, and 0.44 dynamic power for nearly identical PSNR. When compared to other hybrid and heterogeneous approximate memories, the SE6T memory performs progressively best in terms of design complexity, area, or power for a given PSNR.

IV.PROPOSED OBJECTIVES

- **Motivation For The Research**

Embedded memory takes up a significant portion of the chip section of today's SoC and CPUs. A sizable amount of the chip region in a modern processor chip is influenced by the embedded SRAM. SRAM bit cell proximity is compressed by 50% for each technology through device scaling in order to increase the thickness of SRAM. As a result of SRAM's significant contribution to the chip area, chip rate and yield are being intensively pushed. Nevertheless, the opposite aspect of nanoscale technology's shortness is that, while technology develops more slowly, process unpredictability and device leakage are escalating quickly. Due to the technology's scalability and the chip's increasing inclusion of more transistors, dynamic power has also been rising.

As component sizes in nanoscale techniques decrease, mechanical problems such as ageing effects become more apparent and begin to degrade the device over time. The SRAM power dissipation, which is the largest component in a significant number of SoCs, affects the SoC's overall power in both operational & standby modes. SRAM power saving is now a significant limitation, especially for low power applications like battery-operated SoCs.

In other words, process variability reduces the SRAMs' stability & write capability, as well as subsequently the SRAM bit cell's durability. The scaling of the SRAM supply voltage adds more complications to this awful situation. When the SRAM supply voltage is kept as small as possible, designing low power VLSI devices becomes challenging.

- **Objectives**

Improvement of various parameter such as stability, power dissipation, delay and power delay product of these considered cell have been investigated. In the total power consumption ,leakage and other parameters also play an important role in the circuit’s performance.

- **TOOLS**

Software requirement- Cadence software tools: 45nm or 90nm

V. RESULTS

To the modeling of SRAM response for read and write process shown below:

Table 1: Parameters for Proposed work

V_{DD}	1v
power	16nw
Delay from st to bl	46 ps
Power delay product	0.736e
Tool	Spectr state

Read operation: Read the data value from the database**.** It is a safe operation, as it does not update any information in the database.

Write Operation: It writes data into the database and saved it for further use. After writing data, data has to be committed (Commit Operation) to making updated information available for further operations. This operation is more prone to vulnerability as it involves modifying database information.

Write operation transfers the address of the desired word to the address lines, transfers the data bits to be stored in memory to the data input lines. Then it activates the write control line.

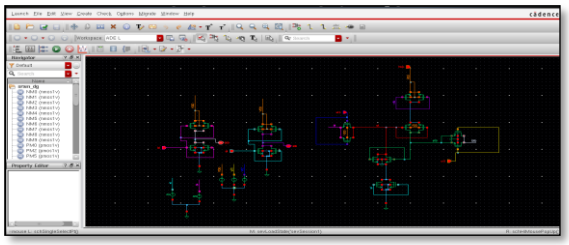

Figure 5: Framework of the Proposed work

The two components that make up the total power consumption in memory architecture are switching or leakage power consumption. The most crucial limitation for building VLSI devices is power consumption decrease. These aspects are predicted to be reduced by a number of memory design strategies. The switching energy consumption has two parts. One is the power used in short circuits as a result of input waveforms' nonzero rise and fall durations, while the other is the power used dynamically as a result of the charging / discharging of load capacitance.

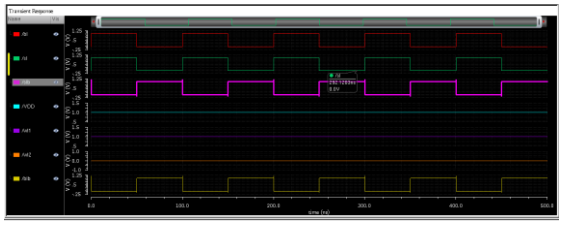

Figure 6: Read operation for SRAM cell

Fig.6 shows the simulation waveform of one row of the SRAM array using the lowered word-line voltage read assist circuit. So it improves the read margin of the SRAM cell, i.e., the cell nodes of the SRAM do not flip in the read operation as it can be observed in Fig.6.

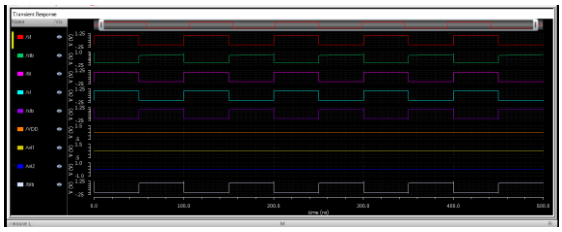

Figure 7: Write operation for SRAM cell

Bit line is low & bit line bar is raised as during write '0' procedure. Consequently, transistor VT1 is turned off, while transistor VT2 enters an ON state. As a result, the voltage source V2 forces a decrease in voltage at the bit line bar's output. Identical to the write "1" action, the transistors VT1 & VT2 turn on after the operation is completed. As a result, the swing at the bit line's output is reduced by voltage source V1.

At higher resonant frequencies, the switching energy consumption is designed to be nearly stable for the memory cell. The durability of the projected memory cell increases along with the switching capacity offered by the voltage

sources. Although switching energy consumption increases as the frequency range expands, voltage supplies are designed to minimize voltage swings at the outputs concurrently. Consequently, as the frequency increases the voltage swing decreases simultaneously.

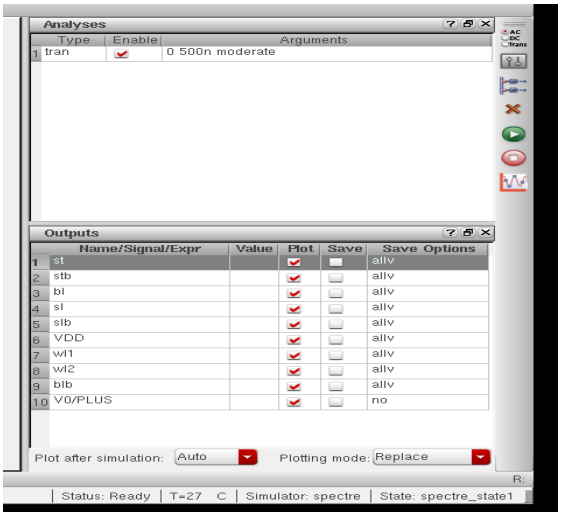

Figure 8:Spectre

Figure 8, For SRAM read operations, we have a spectre stimuli file. However, when We include the file & simulate using the spectre. The results also presented the SRAM cell controller increase the power depending on the load requirement for renewable energy applications. The proposed approach showed promising performance in controlling the system.

VI. CONCLUSION

After reviewing a large number of recent research papers, a new SRAM cell was introduced in this paper. When compared to the other SRAM cells, this SRAM cell has a significant reduction in read and writes power dissipation and a significant increase in read- write access moment. To address the following troubles, the current study compares several design techniques, including Tri-mode Multi-Threshold CMOS, Self-Controllable Voltage Level-Upper and Transmission gate circuit boards, and SVL, and also low swing logic. The Cadence SPECTRE simulator was used to generate all of the results. Because read power as well as read delay is inversely proportional, the read delay of a 7T SRAM cell is greater than that of a 6T, 8T, or 9T SRAM cell. Moreover, 7T and 9T SRAM cells are more effective in terms of write delay, but less effective in terms of read delay when compared to conventional 6T SRAM cells using 45nm or 90nm. The cost of such advancements is enhanced in cell area. As a result, the suggested SRAM cell is a viable option for low-power, high-noise tolerant SRAM cells in measured innovation.

REFERENCES

[1] Neelam Surana and Joycee Mekie, " Energy efficient single-ended 6-t sram for multimedia applications", IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 66, No. 6, pp.1023–1027, 2018.

[2] Y. A. Alqudah, H. Hajj and M. Abdel Moneum, "Defect analysis," U.S. Patent 8 064 682, Nov. 22, 2011.

[3]Neil H.E. weste & David Money Harris "CMOS VLSI Design: A Circuits and Systems Perspective" edition, Pearson Education, 2005.

[4] K. Dhanumjaya, Dr. MN.Giri Prasad, Dr. K.Padmaraju, Dr. M.Raja Reddy "Low Power and Improved Read Stability Cache Design in 45nm Technology" International Journal of Engineering Research and Development, Volume 2, Issue 2, PP. 01-07,July 2012.

[5] L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, S. Borri, M. Hage-Hassan "Efficient March Test Procedure for Dynamic Read Destructive Faults detection in SRAM Memories" JETTA: Journal of Electronic Testing , Vol. 21, No. 21, pp 551-561 ,2005.

[6] G. Shivaprakash1* and D. S. Suresh2"Design of Low Power 6T-SRAM Cell and Analysis for High Speed Application", Indian Journal of Science and Technology, Vol 9, no. 46, 2011.

[7] Lin, Yong-Bin Kim, and Fabrizio Lombardi, Design and Analysis of a 32nm PVT Tolerant CMOS SRAM Cell for Low Leakage and HIGH Stability, Elsevier, vol. 43, no. 2, pp. 176187, 2010.

[8] Chunn, A., Agrawal, A., & Naugarhiya, A., " An 8T TG-DTMOS Based Subthreshold SRAM Cell with Improved Write Ability and Access Times", 24th International Symposium on VLSI Design and Test (VDAT),2020.

[9] Sharma, D., & Birla, S., " Design and Analysis of 10T SRAM Cell with Stability Characterizations", International Conference on Advances in Electrical, Computing, Communication and Sustainable Technologies (ICAECT),2021.

[10] Panguluru, S., & Pandey, J. G., " A Highly Stable and Robust 7T SRAM Cell using Memristor", 24th International Symposium on VLSI Design and Test (VDAT),2020.

[11] Pal, P., Thunder, S., Tsai, M.-J., Huang, P.-T., & Wang, Y., " Benchmarking the Performance of Heterogeneous Stacked RRAM with CFETSRAM and MRAM for Deep Neural Network Application Amidst Variation and Noise", International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA),2021.

[12] Gauchi, R., Kooli, M., Vivet, P., Noel, J.-P., Beigne, E., Mitra, S., & Charles, H.-P., "Memory Sizing of a Scalable SRAM In-Memory Computing Tile Based Architecture", IFIP/IEEE 27th International Conference on Very Large Scale Integration (VLSI-SoC),2019.

[13] Vernekar, P., Kumar Y.B, N., & M.H, V. , "Self Timed SRAM Array with Enhanced low Voltage Read and Write Capability", IEEE Computer Society Annual Symposium on VLSI (ISVLSI),2019.

[14] Shah, A. P., Yadav, N., Beohar, A., & Vishvakarma, S. K., " On-Chip Adaptive Body Bias for Reducing the Impact of NBTI on 6T SRAM Cells", IEEE Transactions on Semiconductor Manufacturing, Vol. 31, No.2, pp.242–249,2018.

[15] Surana, N., & Mekie, J., " Energy Efficient Single-Ended 6-T SRAM for Multimedia Applications", IEEE Transactions on Circuits and Systems II: Express Briefs,2018.