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Peak Detection Control Algorithm for DSTATCOM for balance unbalance non linear load

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Abstract:- Power quality is a big issue in distribution system because of its impact on consumers,manufacturers and utilities.To solve these power quality isues various techniques are developed. This paper present the control alogithm of simple peak detection of DSATCOM for improvement of power quality under linear or nonlinear, balance, unbalanced
load condition in three phase four wire distribution system.DSTATCOM is used for reactive power compensation,neutral current compensation and harmonic elimination.peak detection control algorithm is used to generate the reference supply current of VSC of DSATCOM ,which is based on mathematical formulation.performance of DSATCOM is validated using simulation in matlab software with power system toolbox and its simulink**.**

Keywords- DSTATCOM(distributed static compensator), VSC(voltage source converter), neutral current compensation, power quality.

I. INTRODUCTION

Now-days,AC distribution system is facing[1] poor power quality problem due to the use of linear,non linear and dynamic loads for the industrial ,residential and commercial application.In distribution system power quality problem are categorized in two ways such as current quality problem and voltage quality problem.It included excessive neutral current, load unbalance,distortion in supply ,voltage dip,over voltage,harmonic current etc. These problems can be mitigated using different devices such as Distribution static synchronous compensator,Dynamic voltage restorers,unified power quality conditioner[2].DSTATCOM is connected in shunt with the distribution system,it is use to provide rective power compensation, load balancing,neutral current and harmonics current compensation and provide sinusoidal balance current in supply system.[3]DSTATCOM is consist of six IGBT switches based on current controlled voltage source converter link with a DC capacitor[4]. Various topologies of VSC of Distributed static compensator connected in distribution system, are explain in the literature. Some of these are, Voltage source converter having four legs[5], Voltage source converter of three leg, Voltage source converter of 3 legs with split capacitors[6], Voltage source converter of 3-leg linked with three DC capacitors,Voltage source converter of 3-leg connected with transformers, and Voltage source converter of 2-leg connected with transformers[8]. The transformers used are- a zig-zag transformer, a star-delta transformer, a Scott connected transformer, a transformer with T connection , a star/hexagon type transformer, and a star/polygon type transformer. There are numbers of control algorithm are used to extract the reference current, these are – Control algorithm based on Proportional integral controller [9],Power balance theory (PBT)[10],Icos$_{\varphi}$_based control algorithm,[11]
Current synchronous detection(CSD)based theory, Instantaneous reactive power theory (IRPT),or PQ theory or α–β theory, Synchronous reference frame (SRF) theory also known as d–q theory[12],Singe-phase PQ theory, Singe-phase DQ theory, Neural network theory .
In this paper, peak detection control algorithm is implemented for reduction of harmonics and load balancing because of its advantage of simple structure and fast extraction of reference supply current. The important feature of this control algorithm is reference supply current is directly estimated from load current without use of any reference frame.this mathode is based on mathematical formulation and it gives more accurate and fast respose and it is easy to implement.[13]

II. SCHEMATIC DIAGRAM AND DESIGN OF FOUR LEG VSC BASED DSTATCOM

In this section the designing of reference Dc bus voltage, Dc bus capacitor, AC inductor[14] and Voltage source converter are explain with mathematical formulation.
The schematic diagram of DTATCOM based on 4 leg voltage source converter is connected to the phase four wire system feeding the three phase four wire balance and unbalance load (figure1)

A. .Selecton of DC bus voltage

DC bus voltage across one capacitor is define as $V_{dc}= 2\sqrt{2}V_L/\sqrt{3}m$
Where M is modulation index and considered as 1

V_L = line voltage (415) , hence the value of dc voltage is
$V_{dc}=2\sqrt{2}*415/\sqrt{3}*1=677.69$
selected V_{dc}=700 volt

B. Designing of DC bus capacitor:-

DC bus capacitor is connected in parallel with four leg VSC.
Capacitance is
$C_{dc}=I_o/(2\omega V_{dcpp})$
Where I_o= capacitor current
ω=angular frequency
V_{dcpp}= ripple in dc bus voltage
Consider the ripple is 1.5%
V_{dcpp}=700*0.015=10.5volt
I_o=1.1*I_c
I_c=20*10^3/(700)=28.57A
ω=2Πf=2*3.14*50=314 hz
I_o=28.57*1.1=31.42
C_{dc}=31.42/(2*314*10.5)=0.004764 farad
selected C_{dc}=5000μf for this investigation.

C. Design of Ac inductor:-

The ripple filter inductance for netural leg-
$L_{sn}=mV_{dc}/(3\sqrt{3}af_sI_{crpp})$
f_s=10khz
consider the current ripple is 5%
I_{crpp}=28.57 *0.05*√2= 2.02
m=1
a=overloading factor=1.2
L_{sn} = 1*700/(3√3*1.2*10*10^3*2.02)
= 0.0055575 H
So 5mH is selected in this investigation.

AC filter inductance-
Ac inductance Ls is depends on DC bus voltage(VDC), current ripple Icrpp, and switching frequency (fs)
$L_s=\sqrt{3}mV_{dc}/(12af_sI_{crpp})$.
Consider the current ripple is 5%
a=1.2
$L_s=\sqrt{3}*1*700/(12*1.2*10*10^3*2.02)$
=0.0041681 H

D. Selection of IGBT parameter :-

IGBT switching voltage (V_{sw}) is calculated as
$V_{sw}=V_{dc}+V_d$
Where V_d=10% overshoot in dc link voltage
V_{sw}=700+(0.1*700) =770 volt
With safety factor 1200V IGBT are selected for
VSC IGBT switching current (I_{sw}) is calculated as
$I_{sw}=1.25(I_{crpp}+I_{cp})$
I_c=28.57 A
$I_{cp}=28.57*\sqrt{2}=40.404$ A
$I_{crpp}=28.57*0.05*\sqrt{2}=2.02$
$I_{sw}=1.25(2.02+40.404)=53.03$A, next available rating of 300A IGBT switch is selected for VSC used in DSTATCOM.

E. Designing of ripple filter :-

Time constant of filter should be very small compared to fundamental with period(T),$R_f C_f \leq T_f$
Consider $R_f C_f = T_c/10$
Where R_f =ripple filter resistance= 0.5 Ω
C_f= ripple filter capacitance=15μF
T_c= switching time
T_c=15*10^-6*0.5*10=7.5*10^-5

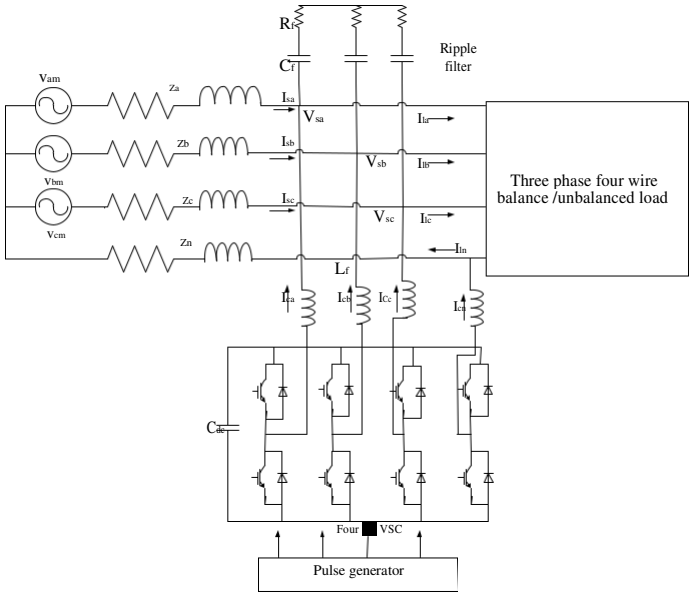

Figure 1. Schematic diagram of four leg VSC of DTATCOM connected to three phase four wire system

III. CONTROL ALGORITHM

Figure 2 shows the control strategy of proposed system.this Simple peak detection control algorithm is used to extract the reference source current which is based on mathematical formulation.
v_a , v_b ,v_c = three phase voltage at
pcc V_{dc}=DC bus voltage

A. PCC voltage and unit vector voltage

The amplitude of pcc voltage (V_{ts}) is
$V_{ts}=\{2/3(v_a^2+v_b^2+v_c^2)\}^{1/2}$ (1)

B. In phase unit vector voltage are

$u_{an}=v_a/v_{ts}$, $u_{bn}=v_b/v_{ts}$, $u_{cn}=v_c/v_{ts}$

C. The quadraure unit vaector voltage

$u_{ad}=(-u_{bp}+u_{cp})/\sqrt{3}$, $u_{bd}=(3u_{ap}+u_{bp}-u_{cp})/2\sqrt{3}$,
$u_{cd}=(-3u_{ap}+u_{bp}-u_{cp})/2\sqrt{3}$ (3)

D. Active and Reactive power components of load current

$I_{la}(t)=I_{av}+I_{lna}(t)+I_{lda}(t)+I_r(t)$ (4)

Where I_{av}= DC components of load current

I_{lna}=active power components of load current for phase a

I_{lda}=reactive power components of load current for phase a

I_r =harmonics present in load current.

To extract the active power components of load current ,load current is multiply by in- phase unit vector voltage then it is passes through the low pass filter and multiply by factor 2 as a gain is used to obtain the amplitude of active power components.fundamental of active power components of load current for phase b and c are also extracted using similar method.

The average amplitude of fundamental active componenets of load current is expressed as

$I_{lnA}=(I_{lna}+I_{lnb}+I_{lnc})/3$

Peak value of reactive power components of load current for phase 'a' is extracted by multipling the quadrature phase unit voltage to the load current of phase 'a' the passes through the low pass filter and multiply by the amplification factor '2' .

Similar process is repeated for obtainingthe reactive power components of load current for phase 'b' and 'c'.

The average amplitude of reactive power of load current is expressed as

$I_{ldA}=(I_{lda}+I_{ldb}+I_{ldc})/3$

E. Acive power components of regerence source current

It is a addition of fundamental active power components of load current of self supporting dc bus of DSTATCOM. The current of DC bus voltage of VSC for n^{th} instant is

$I_{cn}(n)=I_{cn}(n-1)+k_p\{(v_r(n)-v_r(n-1)\}+k_i v_r(n)$

Here error in amplitude of DC bus voltage is

$v_r=v_{dc}^{*}-v_{dc}$

where v_{dc}^{*} =amplitude of reference voltage of dc bus

v_{dc}=amplitude of DC bus voltage . k_p and k_i are proportional and integral gain constant of dc bus voltage.

Total value of active power components of reference supply current is

$I_{sn}=I_{lnA}+I_{cn}$

F. Reactive power components of reference supply current

reactive power components of reference supply current for n^{th} instant is expressed as

$I_{cd}(n)=I_{cd}(n-1)+k_p\{v_r(n)-v_r(n-1)\}+k_i v_r(n)$

Here the error in amplitude of pcc voltage is

$V_r=v_{ts}^{*}-v_{ts}$

where v_{ts}^{*} =amplitude of pcc reference voltage

v_{ts}=amplitude of pcc voltage. K_p and k_i proportional and integral gain constant of PCC voltage bus PI controller.

Total reactive power components of source current is

$I_{sd}=I_{cd}-I_{ldA}$

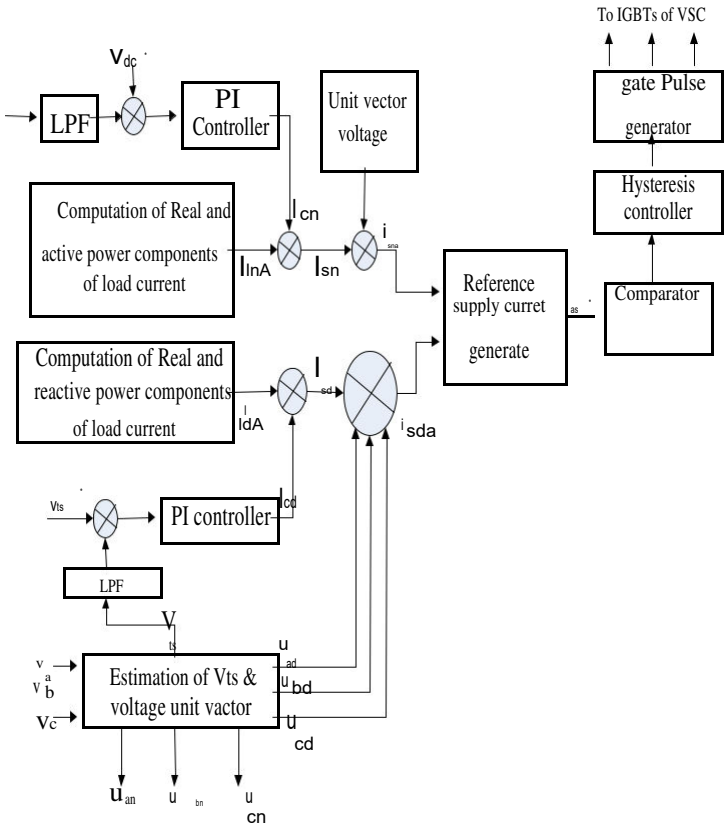

Figure 2- control Algorithm

G. Generation of gating pulses

Active power components of supply current are

$i_{sna}=I_{sn}u_{an}$, $i_{snb}=I_{sn}u_{bn}$, $i_{snc}=I_{sn}u_{cn}$

reactive power components of supply current are

$i_{sda}=I_{sd}u_{ad}$, $i_{sdb}=I_{sd}u_{bd}$, $i_{sdc}=I_{sd}u_{cd}$

Total reference supply current are obtain by adding active and reactive components of reference supply current as

$I_{as}^{*}=i_{sna}+i_{sda}$, $I_{bs}^{*}=i_{snb}+i_{sdb}$, $I_{cs}^{*}=i_{snc}+i_{sdc}$

There phase reference supply current are compared with sensed supply current to estimate the current error.

These current error are amplified using PI controller and out of PI controoler is used to generate gating pulses of IGBTs of VSC

IV. SIMULATION RESULT AND DISCUSSION

The performance of proposed system for various load condition is simulated using matlab model are shown in the following figures.In which voltafe source (V_s),supply current source(I_s),source neutral current(I_{sn}),load cuurents (Ila,Ilb,Ilc),load neutral current (Iln),compensator current (I_c),DC bus voltage(V_{dc}),terminal voltage (V_t) are shown.

A. performance of DTATCOM under nonlinear loads

Figure3 shows the response of DTATCOM for nonlinear load. three single phase bridge rectifier with R=20Ω, L=5mH, C=1000μF are used as a nonlinear load which is connected at 0.8 sec to the supply system.
figure 4 shows its frequency spectrum analysis,the THD for non linear load is 3.60% which is under the limit of IEEE-519 standard.

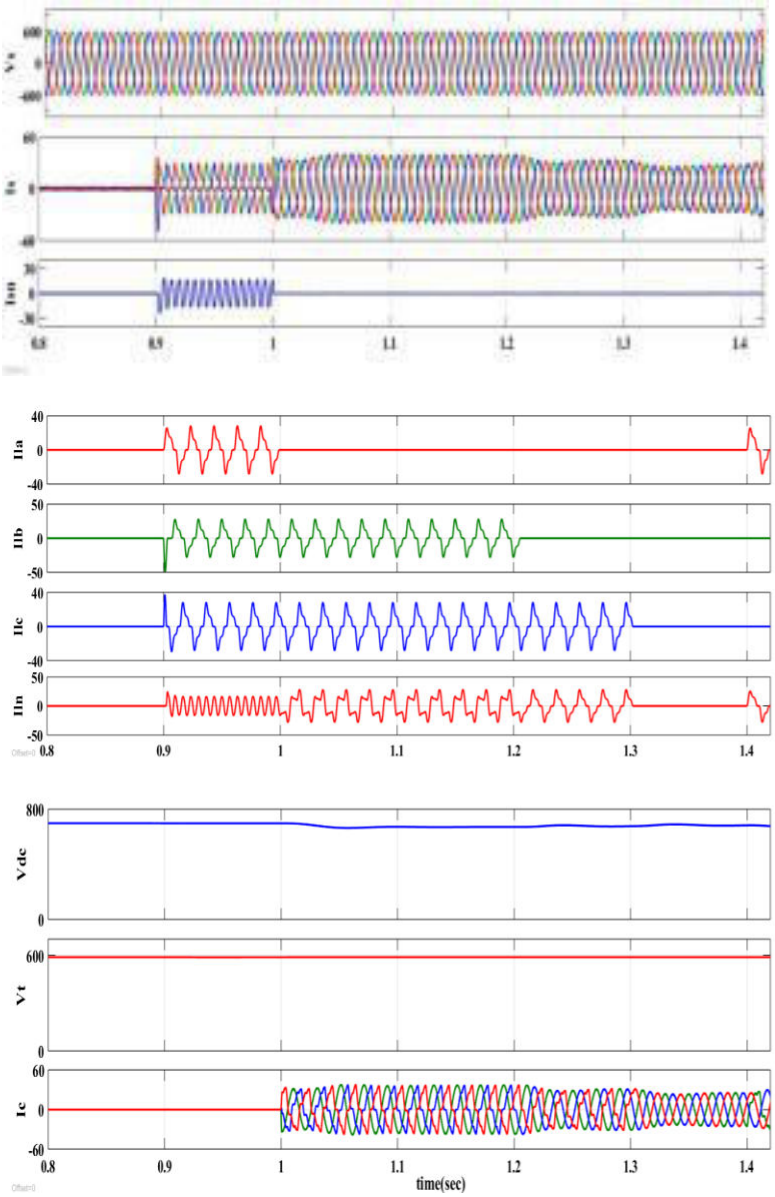

Figure3 performance of DTATCOM under nonlinear load

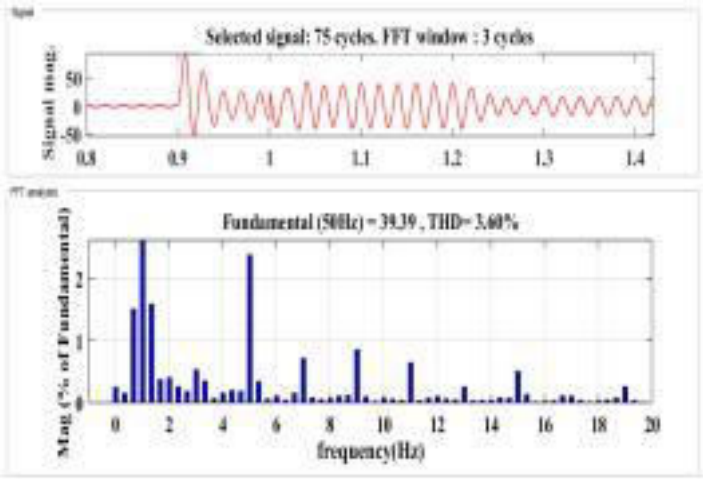

Figure4 frequency spectrum of DSATCOM for nonlinear load

B. performance of DSTATCOM for dynamic load

Figure5 shows the waveform of the DSTATCOM under dynamic load condition ,the load is connected at 0.8 sec to the supply system.the waveform of source current and its harmonic distortion is shown in fig.6 It is observed that THD for source current is 3.60%.which is with in the limit of IEEE -519 standard.

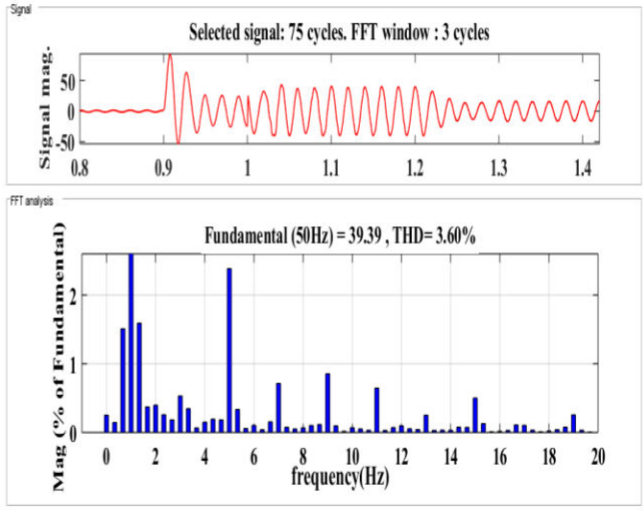

Figure6 frequency spectrum of DSTATCOM for dynamic load

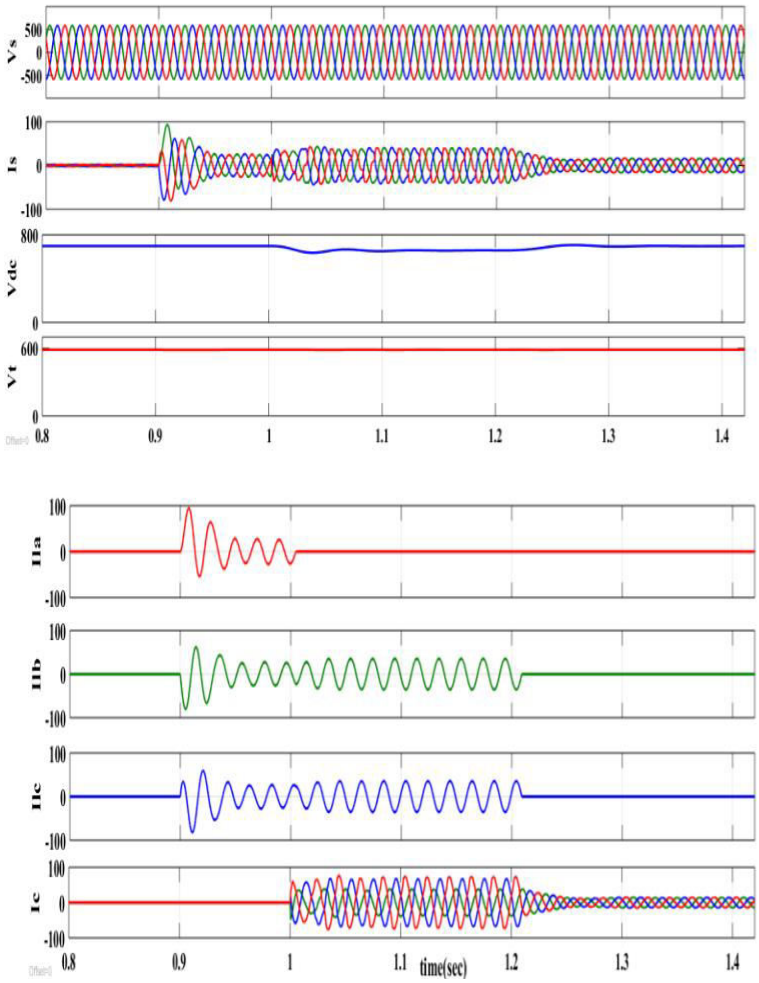

Figure5 performance of DTATCOM for dynamic load

C. Figure 7 shows the performance of DSTATCOM for control converter load.

Figure7 shows the waveform of the DSTATCOM for the load of control converter,the load is connected at 0.8 sec to the supply system.initially the source current is distorted but when the DSTATCOM with 4 leg VSC is connected to the system it become sinusoidal . The waveform of source current and its harmonic distortion is shown in fig.8 The THD(total harmonic distortion) for source current is 3.13%.which is less than 5% as required by the IEEE-519 standard.

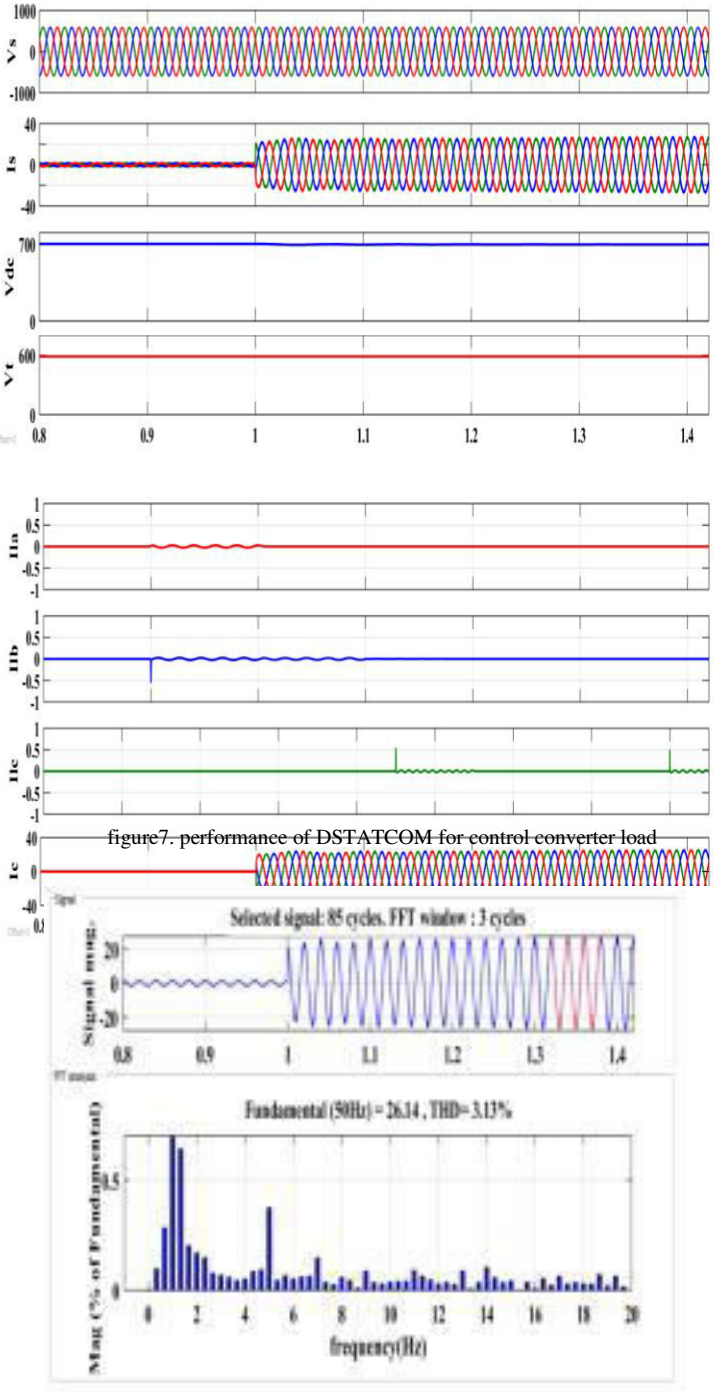

figure7. performance of DSTATCOM for control converter load

Figure8 frequency spectrum of DTATCOM for control converter load.

D. figure9 shows the performance of DTATCOM under RL load

The wave form obtain when RL load is connected to the supply system is represented in the figure 9.RL load is connected at 0.7 sec .the balance source current is observed for unbalance load and THD is recored for the current source is 4.94%.it is less then 5% thus meeting the requirement of IEEE-519 standaed.

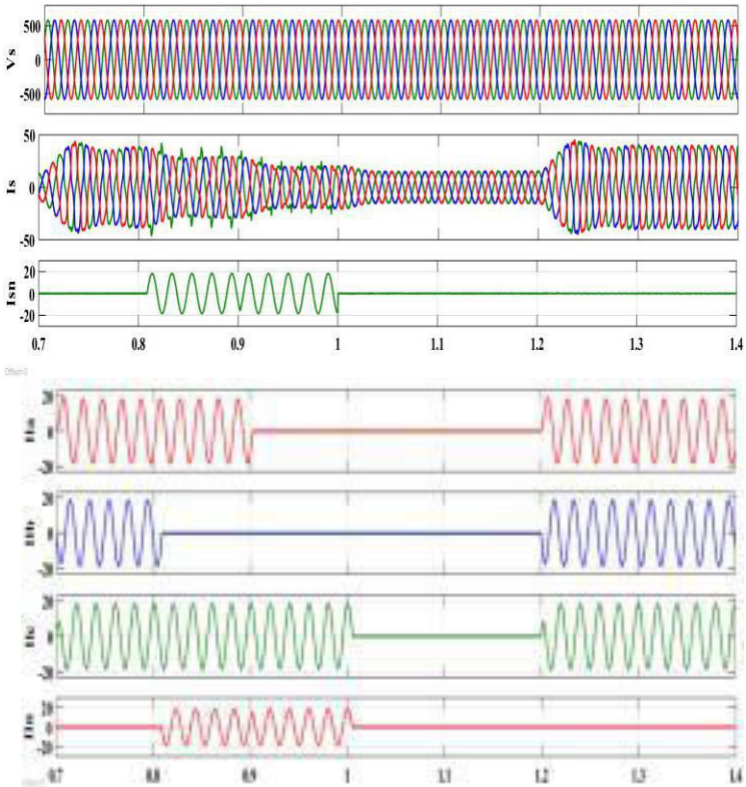

figure9 performance of DTATCOM under RL load

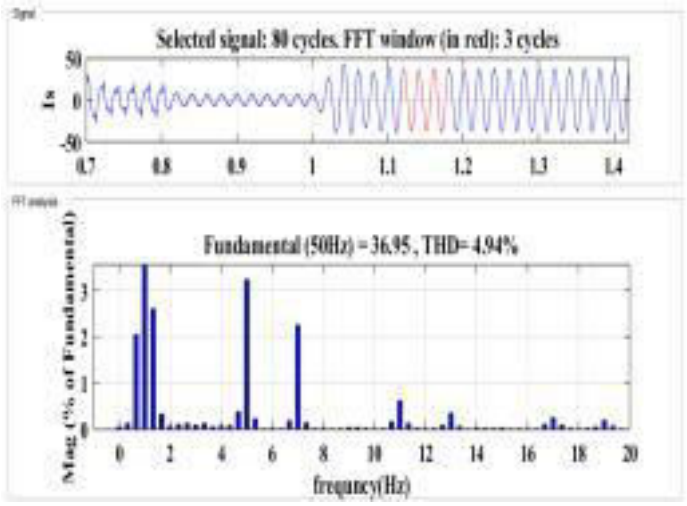

figure10.frequency spectrum of DSATCOM for RL load

V. CONCLUSION

Proposed control algorithm contains DSTATCOM with VSC having 4-legs linked with the DC capacitior which is connected to four wire three phase system for refinement of power factor, harmonic current and to compensate the neutral current.This control algorithm is implemented to draw the reference source current used to generate the gate pulse of VSC.This topology gives the satisfactory operation under balance and unbalance load condition . PI controller upgrades the peformamnce of controller .The result obtained using simulation based matlab model is giving the desired result.

APPENDIX

Three-phase supply voltage: 415V (L-L),50Hz

DC bus capacitor: C_{dc}=5000μF

DC bus voltage: 700V

Source impedance: R_s=5Ω, L_s =1mH

Ripple filter: R_f =5Ω, C_f=15μF

(i)Non-linear load: three single phase bridge rectifier with Resistance=20Ω, L=5mH, C=1000μF

PI controller of DC bus voltage : K_p =0.4,K_i=0.3

PI controller of PCC voltage: K_p =0.8,K_i=0.5 (ii)Dynamic load

PI controller of DC bus voltage: K_p =0.5,K_i=0.3

PI controller of PCC voltage: K_p =0.5,K_i=0.5 (iii) . RL load;

PI controller of DC bus voltage: K_p =0.6,K_i=0.5

PI controller of PCC voltage: K_p =0.3,K_i=0.1 (iv). Control converter load:

PI controller of DC bus voltage: K_p =0.8,K_i=0.5

PI controller of PCC voltage: K_p =0.8,

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