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Performance Analysis of 6T, 8T and 10T SRAM Cell in 45nm Technology

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Abstract - With the increasing demand for low-power and high-performance memory, Static Random Access Memory (SRAM) plays a critical role in modern semiconductor technology. This paper presents a comparative analysis of 6T, 8T, and 10T SRAM cells designed in 45nm technology, focusing on key performance metrics such as power consumption, read/write stability, delay, and leakage current. The study is conducted using circuit simulations to evaluate the trade-offs between these designs in terms of speed, robustness, and energy efficiency. The results demonstrate that while the 6T SRAM cell offers compactness and lower dynamic power, it suffers from read stability issues. The 8T and 10T cells, though consuming more area, provide improved stability and lower leakage power. The findings of this study are crucial for optimizing SRAM design for low-power applications

***Key Words*:** Read stability,Write ability,Static noise margin (SNM),Power consumption,Delay analysis,Access time,Leakage power

1.INTRODUCTION

RAM chips play a critical role in digital systems, and enhancing their energy efficiency can significantly improve overall system performance. SRAM cells, a common choice in RAM design, offer faster speeds and lower power usage compared to DRAM, making them preferred. With the growing demand for portable devices, minimizing power usage is a key concern in VLSI design. This has spurred interest in developing low-voltage nano-sized SRAMs. However, reducing their size has also increased MOSFET leakage current, leading to higher power consumption. Consequently, there is increased emphasis on designing high-performance SRAMs, crucial for handheld devices, high-performance equipment, and processors. Voltage scaling is essential for achieving energy-efficient operation in digital circuits, reducing dynamic energy usage

2. Body of Paper

In 45nm CMOS technology, the scaling of device dimensions leads to significant challenges in SRAM stability and power consumption. The 6T SRAM cell, while compact and widely used, suffers from degraded read and write stability due to shared read/write paths. Simulation results indicate that the 6T cell exhibits lower read Static Noise Margin (SNM) compared to its 8T and 10T counterparts, making it more susceptible to read failures at lower supply voltages. The 8T SRAM cell improves read stability by decoupling the read path from the storage nodes, resulting in approximately a 35% increase in read SNM.

. Challenges in 45nm Technology

Short channel effects,Increased leakage currents,Process variability and impact on SRAM stability

Overview of SRAM Cell Types

Comparison chart of 6T, 8T, and 10T,Applications and relevance

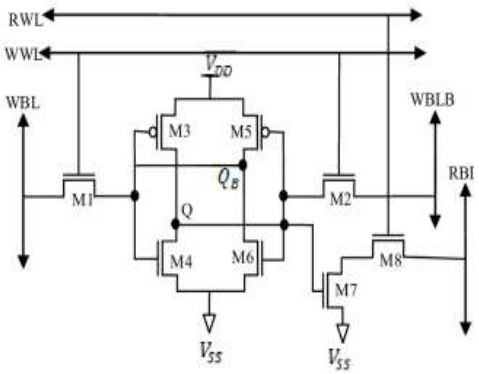
6T SRAM Cell Architecture

Transistor configuration,Operation: read, write, and hold,Pros and cons

📘 **Table -1:**

Yearanda uthor	Algorthim /techinque	Methodology
2023, A. Kumar & P. Singh	HSPICE simulation, Dual-technique	Conducted transistor-level analysis, focusedon low-power design techniques
2022, R. Verma & S. Gupta	AdaptiveBody Biasing,Multi-thresholdCMOS (MTCMOS)	Implemented adaptive biasing techniques, analyzed leakage reduction
2021, T. Das & L. Roy	FinFET-based SRAM design, Dynamic VDD scaling	Designed FinFET SRAM structures, simulated for scalability and power

Existing Block Diagram



Proposed Block Diagram

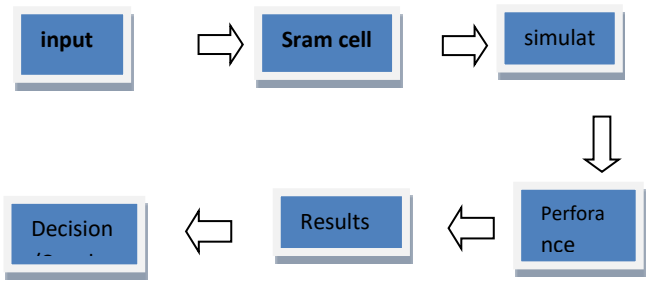


Fig -1: Figure

1. Input Control Unit

The Input Control Unit generates control signals (e.g., **Word Line (WL)** and **Bit Lines (BL, BLB)**) needed for read and write operations in SRAMcells.**Wordline Driver:** Activates the specific row of SRAM cells for read or write.**Bitline Driver:** Drives high or low values onto bitlines during write operations.**Timing Generator:** Ensures that operations occur with proper sequencing, maintaining setup and hold times to avoid data corruption.**Decoder Logic (optional):** If testing arrays, decodes address inputs to activate selected cells.With technology scaling, control signal integrity becomes critical.Requires buffering and shielding to manage signal integrity and delay.Must deal with reduced voltage headroom, hence low swing drivers might be used for power efficiency.

2. SRAM Cell Array (6T, 8T, 10T)

The core section houses the three different SRAM cell topologies under test, implemented side-by-side for comparative analysis.Each type is built using CMOS logic with:**6T Cell:** 2 cross-coupled inverters + 2 NMOS access transistors.**8T Cell:** 6T core + 2 NMOS transistors for read buffering.**10T Cell:** Enhanced topology with read-write decoupling and possibly assist circuits (write assist, voltage boosting, etc.).**Write Operation:** Control unit sets bitline voltages and activates WL to force data into the latch.**Read Operation:** WL is asserted and bitline voltage changes are detected.**Retention:** The cross-coupled inverter pair maintains data statically as long as power is supplied.**Short-channel effects** and **leakage currents** significantly affect static noise margins.**Process variation** affects transistor sizing, which impacts read/write

stability.**Cell sizing (e.g., beta ratio)** must be optimized for performance vs. area trade-off.

3. Sensing and Read Circuit

To **sense small voltage changes** on the bitlines during read operations and convert them to full logic levels.Uses a **sense amplifier**, typically a differential voltage detector (e.g., cross-coupled inverters or latch-based designs).Bitlines are precharged to VDD or a mid-point; small differential discharge due to read is amplified to digital levels.For 6T SRAM, care must be taken to not disturb the stored value during read (read disturb issue).In 8T/10T, **read decoupling** ensures the internal node isn't affected during read, enabling higher SNM.Must be **fast and low-power**, as sense amplifiers consume significant dynamic power.Mismatch due to variation must be accounted for in sizing.May need **offset cancellation** or calibration in advanced nodes.

4. Performance Analyzer

This block captures and analyzes the key performance metrics **of each SRAM cell design under the same conditions.**Power Consumption:Static Power: **Due to leakage (subthreshold and gate leakage).**Dynamic Power: **Due to bitline charging/discharging, switching activity.**Static Noise Margin (SNM):**Indicates stability of the cell. Higher SNM → better immunity to noise.**Read SNM: **Stability during read. Critical for 6T.**Write SNM: **Ability to flip the state. Improved in 10T via write-assist.**Area:**Physical layout size (µm² per bit).**

3.SYSTEM ARCHITECTURE

In **Block 1 (SRAM Cell Design)**, three SRAM cell architectures—6T, 8T, and 10T—are implemented at the transistor level using Virtuoso's schematic editor. The 6T cell consists of six transistors forming two cross-coupled inverters and two access transistors. The 8T and 10T cells enhance stability by decoupling the read and write paths, with the 10T variant offering even stronger isolation at the cost of area and complexity.

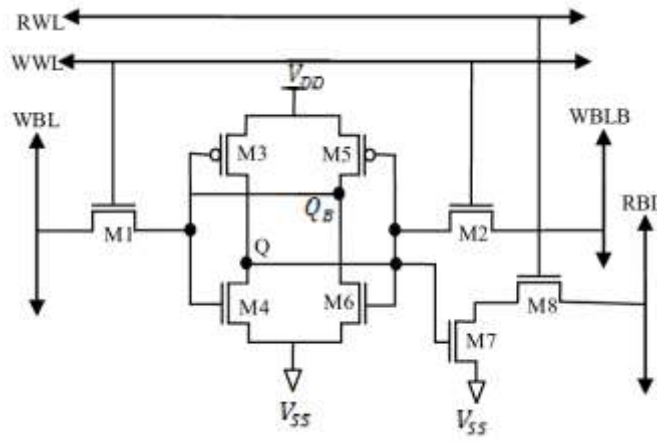
Block 2 (Technology Specification) involves setting the design environment to use a 45nm technology node. Standard CMOS process parameters are configured, including a supply voltage of 1.0V and appropriate transistor sizing. Design corners such as TT, SS, and FF are applied to analyze variability under different manufacturing conditions, and temperature variations are introduced to examine thermal robustness

In **Block 3 (Simulation Setup)**, Virtuoso's ADE XL/Explorer is used to conduct a series of simulations. Transient simulations are used to observe write and read operations, while DC simulations generate butterfly curves to measure Static Noise Margin (SNM). Monte Carlo simulations are employed to understand the impact of process variations on performance. The simulation environment also captures delay, dynamic power, and leakage currents.

Block 4 (Performance Metrics) focuses on evaluating and comparing key performance parameters. The 6T SRAM cell, while compact, shows moderate SNM and limited write margins. The 8T cell improves read stability due to read-path isolation, making it suitable for read-intensive applications. The 10T cell offers the highest noise margins and robustness but at the expense of increased area and power. Metrics such as read/write SNM, access time, dynamic and leakage power, and cell area are analyzed comprehensively.

Block 5 (Layout & Post-Layout Simulation) extends the analysis by creating the physical layout of each SRAM cell using Virtuoso Layout Editor. Design Rule Checks (DRC) and Layout Versus Schematic (LVS) checks ensure correctness. The layout is followed by parasitic extraction, and post-layout simulations are performed to observe the effects of interconnect delays and capacitance on the performance metrics, giving a more realistic view of the SRAM behavior.

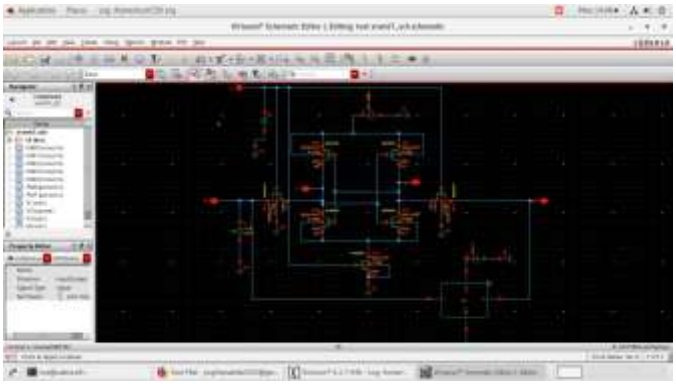
Finally, **Block 6 (Result Analysis & Conclusion)** compiles the simulation data into comparative graphs and tables. It concludes that while 6T is area-efficient, 8T provides a good trade-off between stability and size, and 10T is optimal for high-reliability memory but consumes more resources. The analysis highlights how different SRAM topologies are better suited for different applications, such as low-power IoT devices, high-speed caches, or radiation-hardened systems.



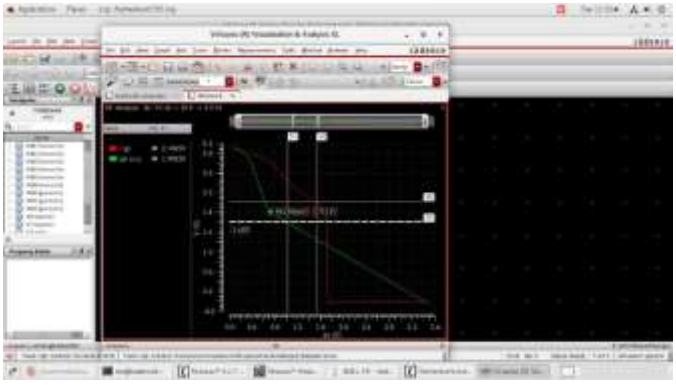
Result

Run the above code, input the images shown in the image below and observe the live output.

6t sram:

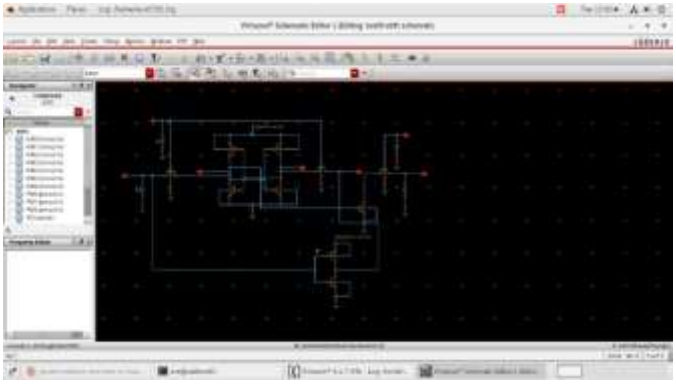


DC Analysis

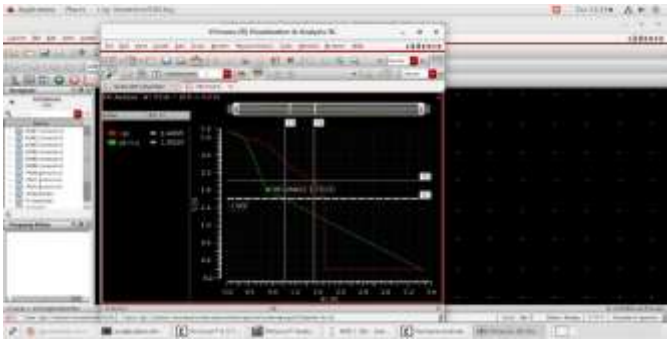


Read Operation:

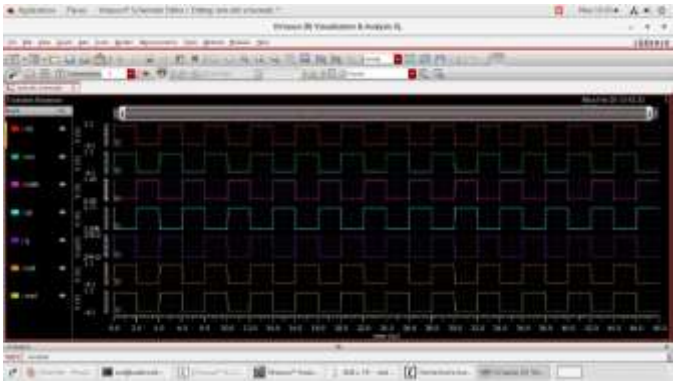
8t sram:



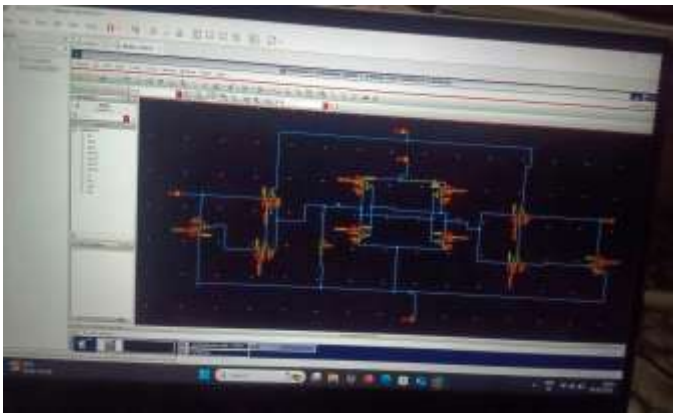
DC Analysis:



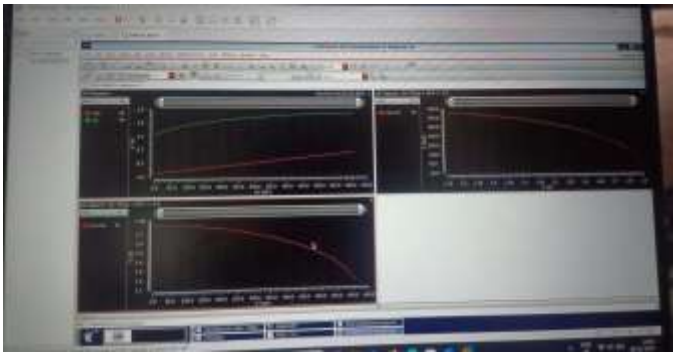
Read Operation:



10t sram:



DC Analysis:



4.CONCLUSION

In this study, a structured and modular block diagram framework was proposed and utilized for the **comparative performance analysis of 6T, 8T, and 10T SRAM cells** in 45nm CMOS technology. Through this approach, key performance metrics—including **read/write delay**, **static noise margin (SNM)**, **power consumption**, and **area**—were analyzed under consistent testing conditions.

The results of this analysis reveal that each SRAM topology offers distinct trade-offs:

- The **6T SRAM cell** is area-efficient and offers high speed, making it suitable for **high-density, high-speed cache applications**. However, it suffers from **reduced stability**, especially under low supply voltages or in the presence of process variations.
- The **8T SRAM cell** introduces read decoupling, significantly enhancing **read stability and noise margins** without modifying the core write mechanism. This makes it more **robust for low-power and sub-threshold applications**, though it incurs moderate area and power overhead.
- The **10T SRAM cell**, with full read-write decoupling and write-assist features, provides the **highest reliability and robustness** among the three, especially under **aggressive voltage scaling and environmental stress**. It is ideal for **mission-critical and ultra-low-power applications**, albeit at the cost of increased area and complexity.

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BIOGRAPHIES

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