Performance Analysis of Multi Level Inverter with Less Number of Switches

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Abstract - A multilevel inverter is a power electronic device that is used for high voltage and high power applications, with the added advantages of low switching stress and lower total harmonic distortion (THD), hence reducing the size and bulk of the passive filters. This paper proposes an enhanced single-phase step-up five level inverter. Compared to conventional five-level topologies, the proposed inverter will reduce the number of power switches, diodes, size and cost of the system. Simple structure, easy control and high step-up voltage ratio will be the main features of the proposed topology. In addition, only four switches will be operating at high frequency and the overall switching losses will be reduced. The system will be modelled with the help of MATLAB/SIMULINK.

Key Words: harmonic, frequency, voltage ratio, switches, level, switching losses.

1. INTRODUCTION

1.1 MULTI LEVEL INVERTERS (MLI)

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application. The concept of multilevel converters has been introduced since 1975. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and re voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output.

1.2 ADVANTAGES OF MULTI-LEVEL INVERTER (MLI)

A multilevel converter has several advantages over a conventional two- level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows.

1. Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore Electro Magnetic Compatibility (EMC) problems can be reduced.

2. Common- Mode (CM) voltage: Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies.

3. Input current: Multilevel converters can draw input current with low distortion.

4. Switching frequency: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency. Unfortunately, the multilevel converters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex. Plentiful multilevel converter topologies have been proposed during the last two decades. Contemporary research has engaged novel converter topologies and unique modulation schemes.

2. PROPOSED MULTILEVEL INVERTER

2.1 AN ENHANCED SINGLE PHASE STEP-UP FIVE LEVEL INVERTER

In the past decade, renewable energy sources such as photovoltaic (PV)-based systems have attracted much more attention due to the advantages such as less environmental impact and improved economic benefits. Multilevel inverters have been receiving significant interest due to the reduced total harmonic distortion (THD) and improved quality of output waveform. As the output voltage level increases, the output harmonic content of such inverters decreases, allowing the use of smaller output filters.

2.2 PROPOSED SYSTEM

The proposed single phase step-up five-level inverter consists of a single dc source, a conventional boost converter, a switch-diode capacitor cell and an H-bridge. The diode-capacitor cell (C1-D1, C2-D2) and the inductor L1 are used to boost the dc-link voltage. The multilevel signal is generated by switch S2 and the diode capacitor cell. The proposed topology can implement the multilevel inversion with high step-up output voltage.

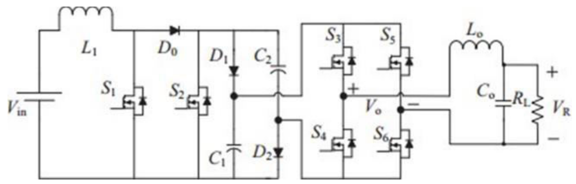
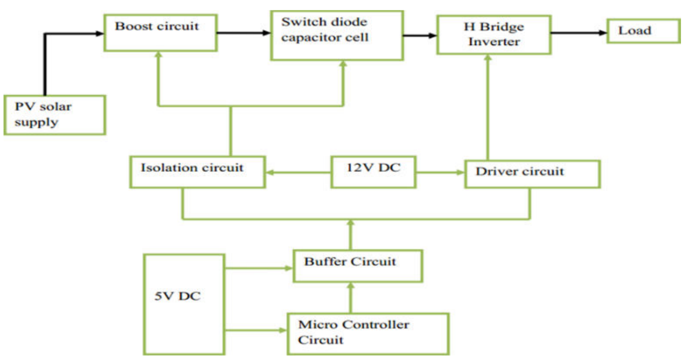


Fig.2.1 Topology of the proposed single-phase step-up five-level inverter.

2.3 MODULATION METHOD

This proposed topology uses the level-shift multicarrier-based pulse width modulation method. Assuming that the capacitorsC1andC2are equal and the diode–capacitor cell (C1–D1, C2–D2) is symmetrical and balanced, one can obtain C1 =C2 =C, uC1 =uC2 =UC (1) whereuC1 and uC2 are the voltage across the capacitors C1 and C2.

2.4 BLOCK DIAGRAM



2.5 OPERATING PRINCIPLE

The working mode of the proposed five-level inverter. The red arrows in the figures show the current path. Overall, it can be seen that there are six switching states in each half-cycle. The operating modes of the positive half sinusoidal cycle (modes 1–6) are discussed in detail as follows.

MODE 1:

S1 is turned ON in this mode. The inductor L1 is charged by the input dc source and the inductor current is increasing linearly. Meanwhile, the load current B flows through S6 and antiparallel diode of S4

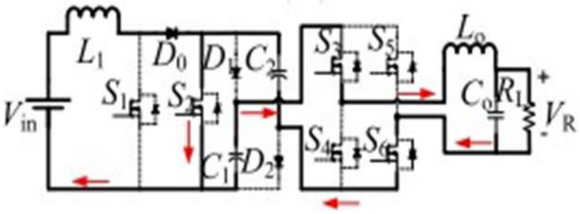


Fig.2.2

MODE 2:

S1is turned OFF in this mode. Diodes D0, D1, and D2 are all conducting. The inductorL1 is discharging and the input source is charging the diode–capacitor network. In this mode, the ac load current still flows through S6 and antiparallel

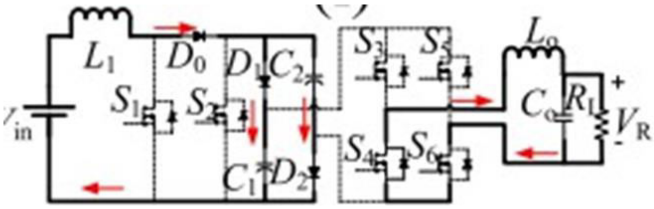


Fig.2.3

MODE 3:

S1 is maintained OFF and S3 is ON in this mode. Diodes D0, D1, and D2 are maintained ON. The input dc source charges the diode–capacitor cell and simultaneously provides the power to the load

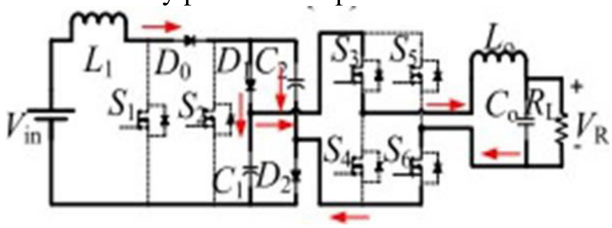


Fig.2.4

MODE 4:

S1 is turned ON again while D0 is turned OFF in this mode. L1 is charged by the input source and capacitors C1 and C2 are working in parallel to feed the load

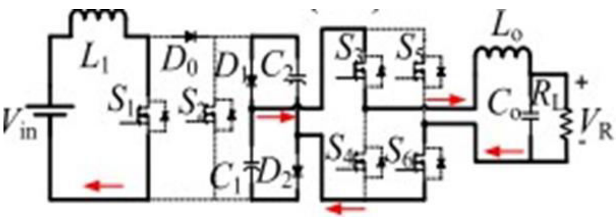


Fig.2.5

MODE 5:

S1stays ON state and S2 is turned ON in this mode. The input inductor L1 is charged again and the capacitors C1 and C2 are connected in series supplying power to the ac load.

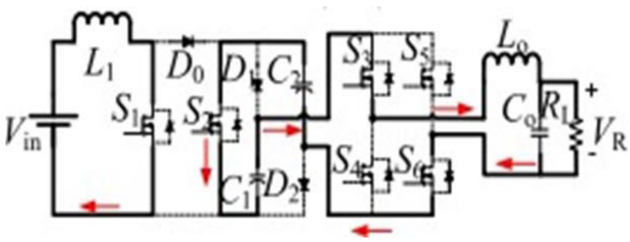


Fig.2.6

MODE 6:

S2 stays ON state and S1 is turned OFF in this mode. Similar as mode 5, the capacitors C1 and C2 are connected in series supplying power to the ac load. Similarly, there are six working modes when the inverter outputs negative voltage and the equivalent working modes

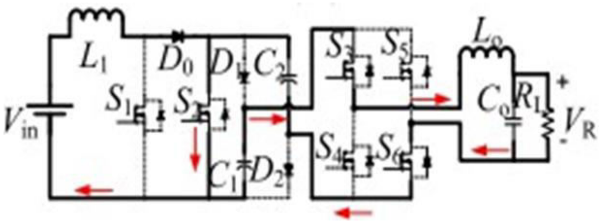


Fig.2.7

3. Result

3.1 INPUT VOLTAGE(Vin=60) VDC WITH R LOAD(200 ohms) Vin=60 v DC ,Ma=1.5, Vrms=194.6 V, Rl=200 ohms

3.1 INPUT VOLTAGE(V_{in}=60) VDC WITH R LOAD (200 ohms)

V_{in}=60 v DC ,Ma=2, Vrms=431.9 V, R_l=200 ohms

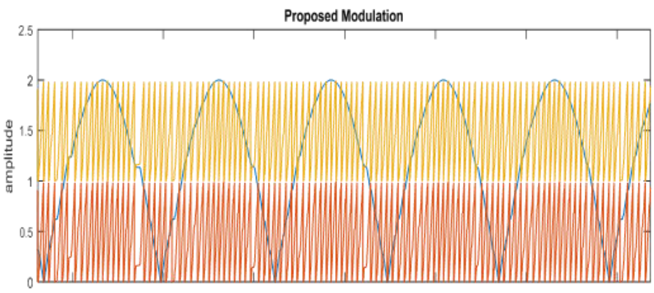


Fig 3.1Proposed Level Shift Carried Modulation (Ma=2)

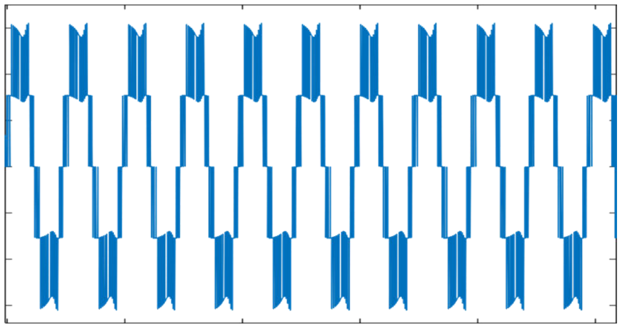


Fig 3.2 Inverter Output Voltage(Vrms=431.9 V

3.2 INPUT VOLTAGE (Vin=12V DC) WITH RL LOAD

(R=200 ohms,L=1e ^-3H)

V_{in}=12 v DC ,Ma=2, Vrms=81.92 V, RL Load=200 ohms, 1e^-3H

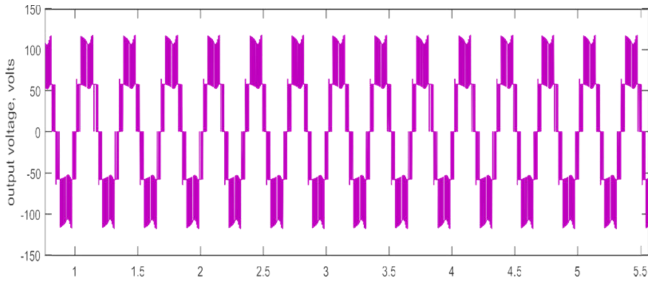


Fig 3.3Inverter Output Voltage (Vrms=194.6 V)

4. CONCLUSIONS

This project proposes an enhanced single-phase step-up fivelevel inverter. Operating principle and output voltage derivation have been performed. Compared to conventional five-level topologies, the proposed inverter reduces the number of power switches, diodes, size and cost of the system. Simple structure, easy control, and high step-up voltage ratio are the main features of the proposed topology. In addition, only four switches are operated at high frequency and the overall switching losses are reduced. Finally, simulation results validate the effectiveness and performance of the proposed topology.

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