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PERFORMANCE ANALYSIS OF ON CHIP INTERCONNECTS FOR ASIC DESIGN

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***Abstract*—Circuit complexity and performance have increased as a result of the constant reduction in semiconductor device feature size. Improved area, power, and speed have resulted from scaling the lateral dimensions of planar devices like MOS transistors. Current scaling patterns hurt interconnects unique properties, especially the global lines. These lengthy resistive cables now consume more electricity and have slower signal propagation times. The connection models must now take inductive effects into account for potential inclusion. Due to these factors, precise interconnect models for on-chip devices are necessary to ascertain the signal properties and construction specifications of fast DSM interconnect. The purpose of this project is to enlighten on the difficulty in designing on-chip connections, particularly for extremely fast purposes.**

***Index Terms*—DSM, Interconnects, Integrated Circuits (ICs)**

I. INTRODUCTION

The essential signal delay's root cause has experienced a significant change. The on-chip connection has emerged as the key component after the development of active device feature sizes into the deep sub-micrometer (DSM) regime. [1]Integrated circuits having high complexity levels and speed are a bottleneck for signal flow (ICs).. The ITRS 2005: International Technology Roadmap for Semiconductors describes how delay caused by passive interconnects has a greater impact, significantly despite the fact that the lower size of the features in DSM technology nodes reduces active device delay. [2] Low power dissipation is now an important design requirement. The quantity of interconnects has multiplied exponentially as a result of decreasing feature size and expanding semiconductor die dimensions. [3] These on-chip lines dissipate the majority of the overall transient power because interconnect capacitance frequently dominates the entire gate load. This feature is particularly true for the massive interconnects used to carry clock signals, where up to of an IC's total power can be lost. Performance improvements include the rise in power dissipation is frequently present, though. [4] As an analogy, having more interconnect layers accelerates the circuit at the expense of more power usage brought on by the increased interconnect capacitance. [5]Interconnect design has emerged as a critical challenge in high-speed ICs, taking into account both power consumption and propagation latency. [6]There is still a major problem with the design complexity of the various connection networks, as well as a rise in interconnect power consumption. [7]Over 1.5 billion transistors are used in microprocessors produced by semiconductor companies these days, and this figure is rising. [3] The clock and power distribution networks each needed a significant number of metal materials in addition to the connections among the many on-chip components. [4]Accurately describing the clock, signal and power networks is challenging;it is even more difficult to allocate metal in the optimal way to construct these networks. [5] The sheer quantity of lines growing is a significant aspect that raises the complexity of interconnect modeling. [6] To accurately represent signal propagation on lines with brief transition periods, RC connection models are not enough. [8] The RC model must now be modified to account for inductance (L).

II. DESIGN TECHNIQUES FOR HIGH-SPEED, LOW-POWER CIRCUITS

When evaluating design strategies for improving circuit performance high-speed and low power circuits. Noise are power significant considerations to take into account. [9]Delay is impacted by noise from both capacitive and inductive interconnect connection between and within layers., waveform shape, and the possibility for inaccurate digital signal interpretation. Furthermore, higher clock rates lead to higher slew rates, which intensifies on-chip noise.

A. Wire Sizing

An IC's power characteristics and propagation delay are influenced by the interconnect's width. [10] The rise in RC interconnect impedances, which results with lengthening the wiring and decreasing the cross-sectional area of the interconnects, reduces gate latency, assume a CMOS inverter driving an RC connection.

B. Driver Sizing

Another design strategy in CMOS logic families that results in trade-offs at the circuit level is transistor sizing. Wider transistors generate greater current, but their physical size and gate capacitance also grow linearly with width,

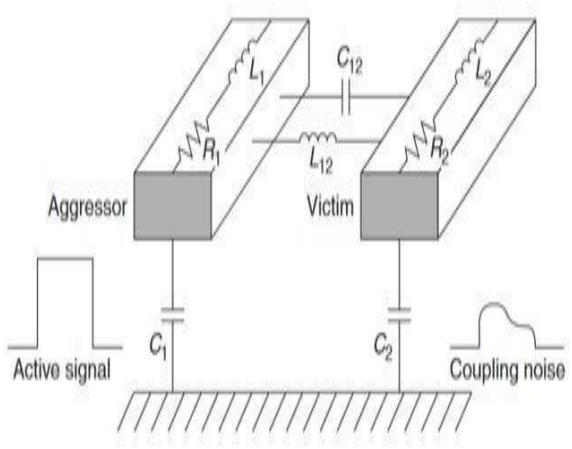

Fig. 1. Cross-coupled interconnect noise in IC's

resulting in larger circuits and more power. As a result, the design trade-offs between area, power, and speed greatly influence ideal transistor sizing.

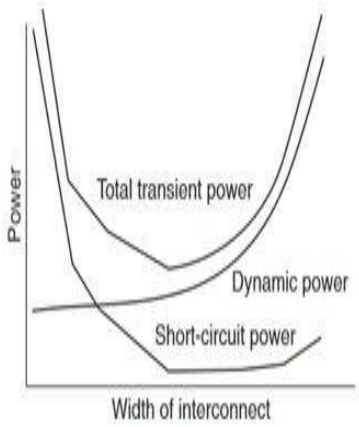

Fig. 2. Parameter as a function of interconnect line width

C. Tapered Buffers

Tapered buffers significantly illustrate transistor size for driving high capacitive loads. [11] The intermediate capacitive loads are driven by the intermediate buffers. The delay is decreased by an inverter that is correctly scaled for the capacitive load, but the inverter loads the prior logic step due to its enormous input capacitance. When another inverter is inserted that is big enough to drive the inverter driving the load, a similar argument can be made. This procedure is repeated until the buffer's initial input inverter is tiny enough to be pushed at a reasonable pace by a logic gate. So, an inverter chain with progressively bigger inverters makes up a tapering buffer. By utilising the first few steps with a fixed-taper factor, the shortest delay of a changeable buffer can be minimized to within a few percent of the wait of a corrected buffer.Thus, resolved buffer systems with larger decreasing constants in the final one to two stages achieve the optimum area-delay trade-offs.

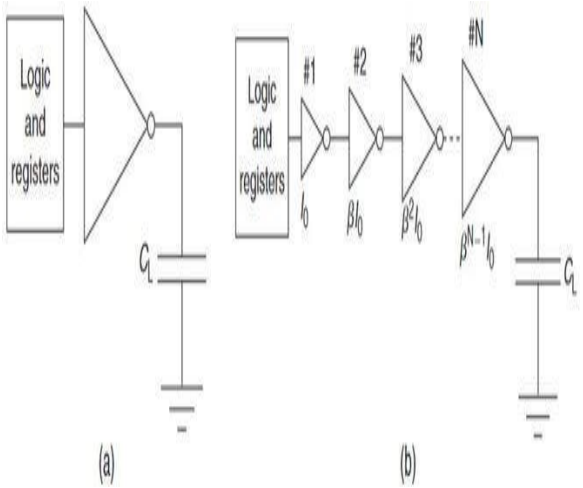

Fig. 3. (a)A large single inverter (b)A system of tapered buffers

D. Repeater Insertion

The overall wire latency is barely impacted by widening a uniform line. Inserting buffers strategically along a line is a more efficient way to reduce the delay of a lengthy link. The procedure is known as repeater insertion, and these buffers are frequently referred to as repeaters. Repeaters divide the line into smaller, roughly equal portions to avoid the delay of the quadratic increase in connection.Since each section's delay has dropped, the original path's duration is now less than the aggregate of the section lags.. Depending on the electrical properties of the line, different methods can be used to increase connection performance. Techniques for repeater insertion perform better for an RC line than wire sizing. In contrast to RC lines, presuming an ideal repeater system is used, the minimum sound radiation time for RLC lines reliably decreases with increasing line width.Wire sizing performs better than repeater insertion in RLC lines because the minimum signal propagation delay with no repeaters is lower than the minimum signal propagation delay when employing any number of repeaters. With broader lines, until there are no more repeaters, the minimum signal propagation delay for an RLC line always gets smaller.

III. Networks for Clock Distribution

The clock signal acts as a reference time for flow of data in synchronous digital systems. Clock signals are most often loaded with any control or data signal within the system that has the largest fanout, travels farthest, and operates at

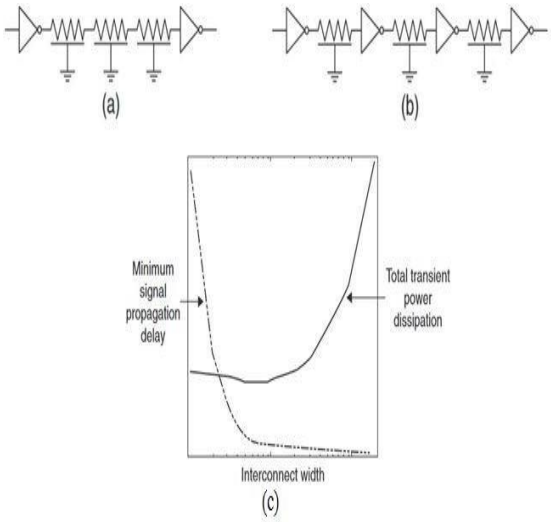

Fig. 4. (a)original interconnect (b)Interconnect line with inserted repeaters (c)Parameters as a function of line width for a repeater system

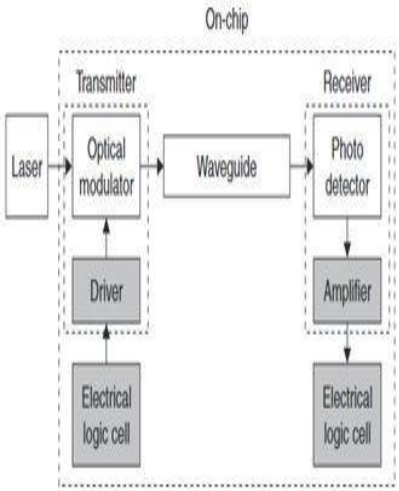

Fig. 5. Block diagram of OI System

the fastest speeds.The maximum system performance can be significantly decreased by controlling any variations in clock signal delay, but doing so can also result in disastrous race conditions where a register may latch onto an invalid data signal.

IV. Emerging On-Chip Interconnect Technologies:

A. Interconnects with Optics

Optical connectors have the ability to overcome the communication bottleneck by changing electrical cables for optical waveguides. Optical interconnects have a slew of advantages over traditional electrical connections, as well as the following: 1. Using only basic on-off modulation schemes, they are capable of supporting enormous intrinsic data bandwidths of several Gbps. 2. They are comparatively resistant to crosstalk, parasitic capacitances, and inductances that cause electrical interference. 3. At the chip level, the transmission distance does not affect their power dissipation. 4. Light beams can physically cross each other with little crosstalk, which simplifies routing and placement.

B. RF/Wireless Interconnects

Another innovative strategy for addressing the constraints of conventional EIs in future lightweight integration technologies is electronic communications interconnects. In such a system, on-chip wires would be replaced by an integrated on-chip antenna that communicates via electromagnetic waves.Baseband data will be transformed to RF/microwave signals and transported over free or directed space, according to this idea. To be effective,the wireless/RF interconnect system's reception and transmission components must be capable of working with upcoming VLSI designs.

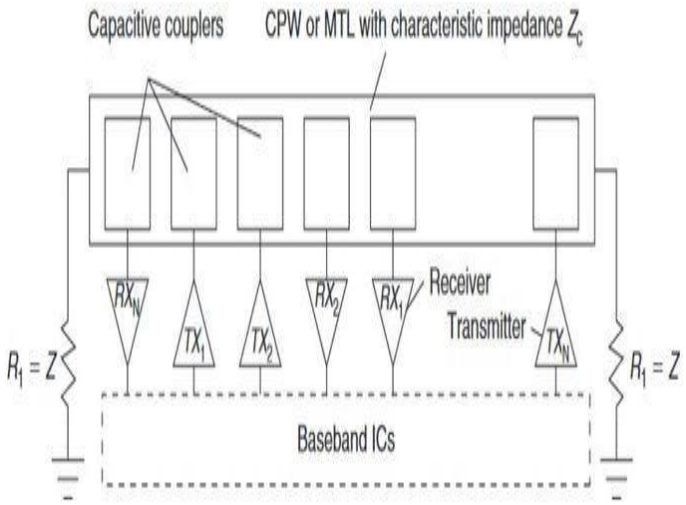

Fig. 6. RF/wireless interconnects with multiple transmitter and repeaters

C. CNT Interconnects

Modifications in the components used for on-chip interconnections are currently being thoroughly investigated in an attempt to reduce the restrictions imposed by copper-based interconnects. In emerging technologies, CNT connections have been considered as a metal interconnect replacement. CNTs are sheets of graphite that have a diameter at around 0.6 and 3 nm. Future technologies may employ CNTs as on-chip interconnects due to their superior mechanical and thermal stability, excellent mechanical properties, and high voltage carrying capability. Because of the covalent bonds in their structure, they are very resistant to other physical breakdown reactions including electron transfer. They have relatively little performance degradation despite becoming capable of surviving very large current densities. Due to its decreased lateral capacitance, which lowers latency at

incredibly close distances, CNTs can replace copper at the local connectivity level. Recent research has shown that CNT bundle architectures exhibit metallic conducting properties. The limitation of current fabrication methods to handle chirality.

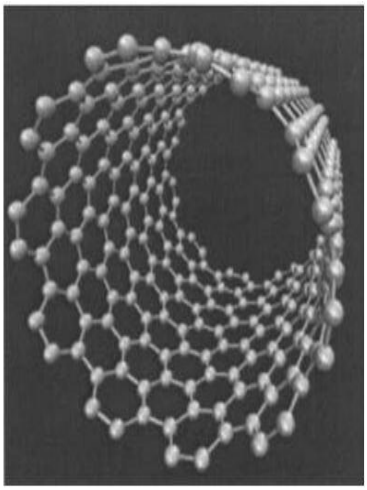

Fig. 7. Single-walled carbon nanotube

V. Conclusion

Each technological generation makes it more challenging to adequately design interconnects under the DSM regime. Understanding the fundamental ideas is important to the development of new process technologies and design methodologies as explained in this paper, as well as to ensuring that electrically interconnect remains a practical method of signal transmission for the coming years. Rolls of graphite sheets with a diameter of between 0.6 and 3 nm are used.

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