Performance Evaluation of A T-Type Multilevel Inverter for Renewable Energy Applications

A.V.Vasanth[1], R. Ramamoorthi[2]

[1] PG Student [PED], Dept. of EEE, Government College Engineering, Salem, Tamil Nadu, India

[2] Assistant professor, Dept. of EEE, Government College Engineering, Salem, Tamil Nadu, India

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ABSTRACT: The increasing demand for clean and efficient energy conversion in renewable energy systems has led to the adoption of multilevel inverters, which offers reduced harmonic distortion and improved efficiency. Among various topologies, the T-Type Multilevel Inverter (T-MLI) is gaining attention due to its lower switching losses, reduced component count, and enhanced power quality. However, challenges remain in optimizing its performance metrics, including efficiency, total harmonic distortion (THD), voltage stress, and grid synchronization. This study aims to evaluate the performance of the T-MLI in total harmonic distortion (THD) and assess its suitability for solar PV integration and compare its performance with NPC multilevel inverters to determine its effectiveness in reducing losses and improving energy efficiency in renewable systems.

Key Words: T-MLI, NPC, THD, renewable energy, reduced component count.

1.INTRODUCTION

A T-Type Multilevel Inverter (T-MLI) is an advanced power conversion technology widely used in renewable energy applications, such as solar PV systems and wind energy integration. This inverter topology is designed to improve efficiency, reduce switching losses, and enhance power quality by generating output voltage in multiple levels, leading to low harmonic distortion (THD). Compared to Neutral-Point-Clamped (NPC) the T-MLI utilizes fewer power semiconductor switches, which reduces cost and complexity while maintaining performance. The control mechanism of the T-MLI plays a vital role in achieving optimal performance. Pulse Width Modulation (PWM) techniques, such as Multiple Carrier Pulse Width Modulation (MCPWM).

Performance evaluation of a T-MLI primarily focuses on factors like efficiency, harmonic distortion, and power conversion capability. The inverter achieves higher efficiency by minimizing conduction and switching losses, making it an ideal choice for clean energy applications. It also enhances power quality by reducing harmonic components in the output waveform, making it highly compatible with grid-connected systems. Due to these advantages, T-MLIs are increasingly used in distributed generation systems, microgrids, and large-scale renewable energy installations where reliable and efficient power conversion is critical. In this project, Hardware implementation of Three phase three level T-Type Multilevel Inverter is fabricated for renewable energy application and tested for resistive loads.

2. MODULATION STRATEGIES FOR MLIs

Modulation strategies play a critical role in controlling the switching of power semiconductor devices in Multilevel Inverters (MLIs). Their primary purpose is to generate the desired output voltage waveform while minimizing harmonic distortion. These strategies directly impact power quality, switching losses, and the overall efficiency of the inverter.Phase Disposition PWM (PD-PWM), illustrated in Fig.1, operates by aligning multiple carrier signals (typically triangular waveforms) in phase. These carriers are distributed across different voltage levels, ensuring consistent modulation. The reference signal, usually a sinusoidal waveform, is compared simultaneously with all carriers.

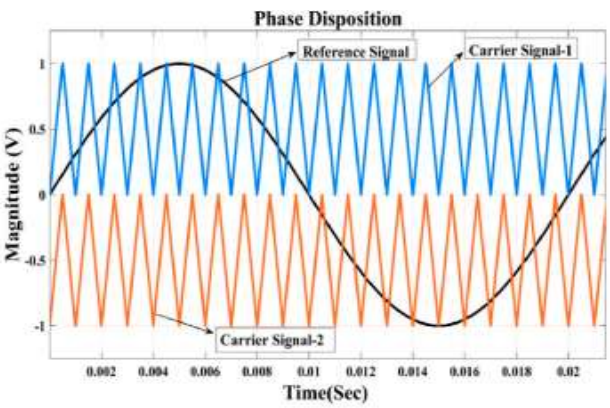

Fig.1: Phase Disposition PWM

This approach results in smooth voltage transitions within the MLI, lower harmonic distortion for enhanced power quality, and better voltage symmetry, making PD-PWM a preferred technique for applications requiring precise voltage control. Multicarrier PWM with Different Modulating Signals is another sophisticated control strategy employed in MLIs to generate high-quality AC output voltage waveforms. Unlike basic PWM, which relies on a single carrier wave, this technique utilizes multiple high-frequency carrier waveforms that are compared with a low-frequency modulating signal. The key advantage lies in the flexibility of using different shapes for the modulating signal to achieve specific performance objectives. Fig. 2 illustrates pure Sinusoidal PWM, the most widely accepted modulating signal, while Fig. 3 presents Third Harmonic Injection PWM. In three-phase systems, the effect of the third harmonic injection is nullified in the output voltage spectrum. By introducing a third harmonic component, the modulator's gain can be increased, with the magnitude of the third harmonic content determining the extent of gain improvement. Studies show that injecting 17% of the third harmonic into a pure sinusoidal wave results in approximately a 15% increase in gain over a pure sinusoidal reference.

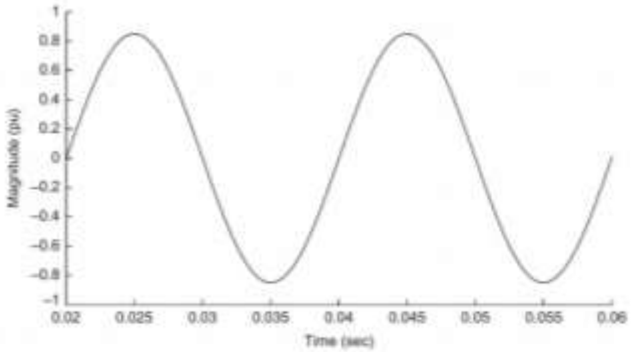

Fig. 2: Pure Sinusoidal Signal.

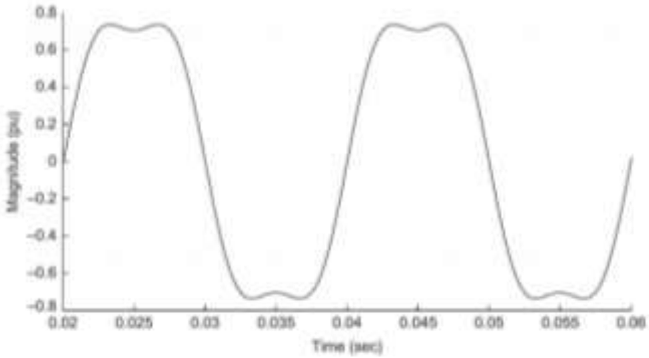

Fig. 3: Third Harmonic Injection Reference Signal.

3. T-TYPE INVERTER TOPOLOGY

The basic topology of the three-level T-type inverter is shown in Fig. 4. This topology extends the conventional two-level voltage source inverter by incorporating an active bidirectional switch at the DC-link midpoint. In low-voltage applications, the high-side and low-side switches (T_1/D_1 and T_4/D_4) typically require devices with higher voltage ratings, as they must block the full DC-link voltage. In contrast, the bidirectional switch at the midpoint only needs to block half of the DC-link voltage, allowing it to be implemented with lower voltage-rated devices. Due to its reduced blocking voltage, this middle switch exhibits low switching losses and acceptable conduction losses, despite consisting of two series-connected devices. There are two main configurations for the lower-voltage-rated switches used in the bidirectional switch: IGBT-based: Either in common-emitter or common-collector configurations. MOSFET-based: Either in common-drain or common-source-configuration.

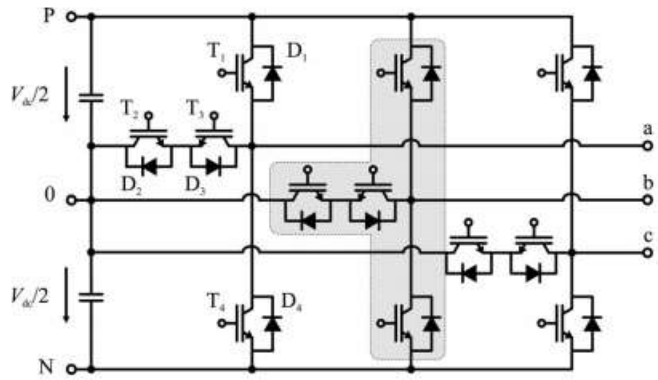

Fig. 4: Schematic of the three-level T-type topology (with IGBT Switch)

Switch Commutation Considerations: The switching behavior of the three-level T-type inverter must be analyzed carefully. The output of a bridge leg can be connected to the positive (P), neutral (0), or negative (N) DC-link voltage levels, as shown in Fig. 5. The following switching sequence is typically used:

Table 1 Switching States

State	V_{out}	T_1	T_2	T_3	T_4
P	$+V_{dc/2}$	On	On	Off	Off
0	0	Off	On	On	Off
N	$-V_{dc/2}$	Off	Off	On	On

Instead of using a current-dependent commutation sequence, a simpler strategy ensures natural current flow regardless of current direction. By closing T_1 and T_2 for the positive voltage level (P), T_2 and T_3 for the neutral level (0), and T_3 and T_4 for the negative voltage level (N), the current commutates naturally to the correct branch. Table 1 summarizes how switch closures achieve the desired output voltage. A simple turn-on delay for all switches prevents DC-link short circuits.

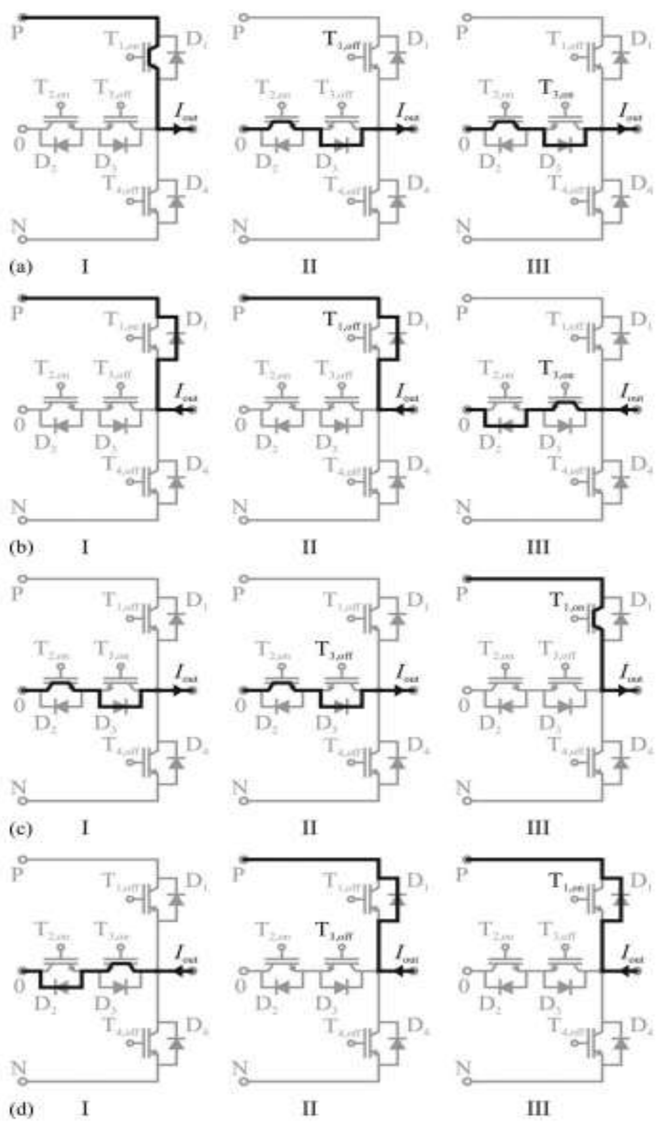

Fig. 5: Current commutation during switching transition (P → 0) for (a) positive and (b) negative output current. Current commutation during switching transition (0 → P) for (c) positive and (d) negative output current.

This modulation method aligns closely with the three-level NPC topology modulation. Current Commutation Behavior: Consider a scenario where the output phase is connected to the positive (P) voltage level, with T_1 and T_2 closed (Fig. 5(a)). To commutate to the neutral level (0): T_1 is opened, and after a short turn-on delay, T_3 is closed. During the turn-off of T_1, the current naturally commutates through T_2 and D_3 to reach the neutral level. Similarly, for negative phase current (Fig. 5.3(b)), the current shifts to the neutral level once T_3 is closed. When switching back from (0) to (P): T_3 is opened, and after the turn-on delay, T_1 is closed. For positive phase current (Fig. 5(c)), the current flows through D_3, eventually shifting to the positive voltage level once T_1 turns on. For negative phase current (Fig. 5(d)), the current moves to D_1 during T_3's turn-off.

Avoiding Direct Transitions: The direct transition from (N) to (P) and vice versa is typically avoided due to space-vector modulation. Although the transition does not significantly impact the three-level T-type inverter, it introduces additional losses in the 600-V diodes. These losses occur because a reverse recovery current pulse flows to the neutral voltage level, triggered by the blocking voltage change from $-V_{dc/2}$ to $+V_{dc/2}$ over D_2 and D_3. By omitting direct transitions between (N) and (P), the semiconductor switches T_1 and T_2 are never switched within the same modulation cycle. Consequently, the high-side switch T_1 does not require increased gate drive power, allowing it to efficiently power T_2's gate drive unit.

4. SIMULATION AND RESULTS

The three-phase, three-level T-type inverter (Fig 6) is simulated in MATLAB/Simulink software using the following design parameters shown in Table 2. For the bidirectional switch, the inverter is simulated using a MOSFET configured in a common-drain arrangement. The carrier wave switching frequency is set to 5000 Hz, and the reference signal is a sinusoidal waveform and Third Harmonic Injection waveform.

Table 2 Simulation parameters

Parameters	Values
Input DC voltage	300 V
Frequency	50 Hz
DC link capacitance	470 µF
Resistive load	100 Ω per phase

For generating T-type inverter control pulse, Phase Disposition PWM is used with sine wave as the reference wave. By comparing sine wave with triangular carrier wave, which is generated by repeating sequence block, PWM is generated. Fig. 7 shows R phase PWM generation. For Y and B phases, phase delay has been implemented. Fig.8 shows R phase Control PWM. Fig 9 shows T-type inverter voltage waveform. The THD value of the T-type inverter is calculated using FFT Analysis and Compared with Neutral Point Clamped (NPC) inverter without filters in Table.3. THI refers to Third Harmonic Injection waveform.

Table 3 NPC vs T-Type inverter THD values

Inverter Topology	Reference signal	Voltage THD (%)	Current THD %)
NPC	Sine wave	41.03	73.17
	THI	37.95	71.78
T-Type	Sine Wave	41.36	41.33
	THI	38.19	38.26

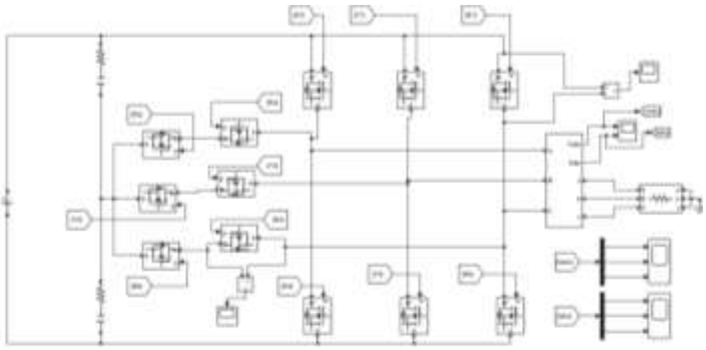

Fig. 6: T-type inverter Simulink diagram

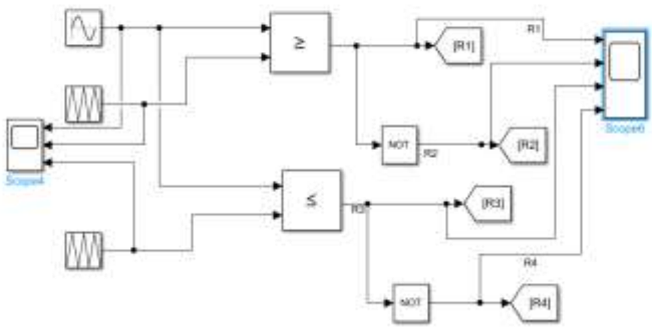

Fig. 7: R phase PWM generation

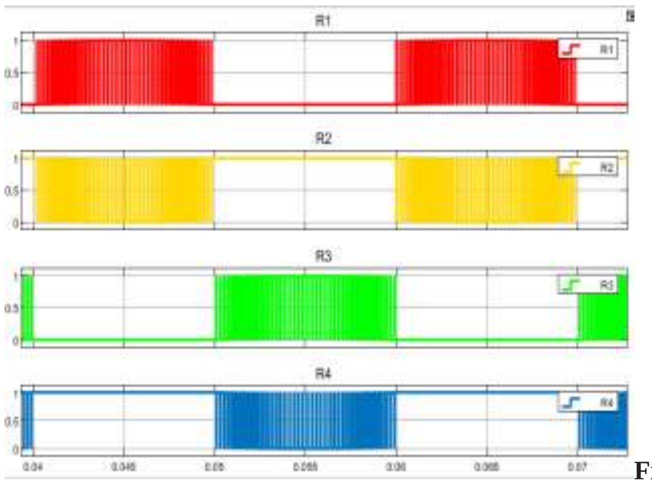

Fig. 8: R Phase Control PWM

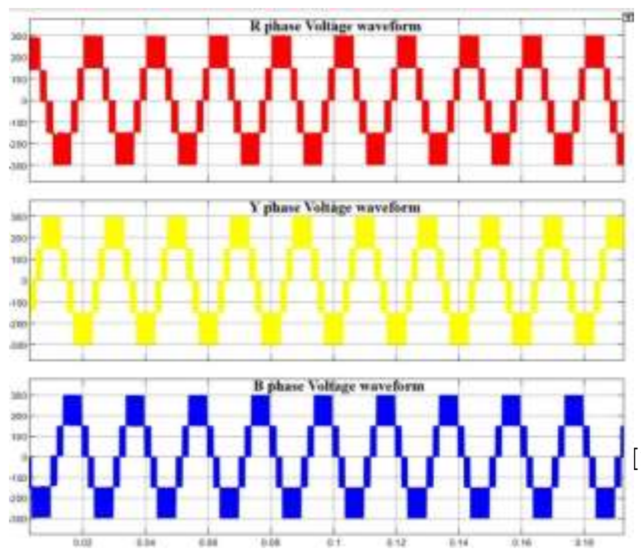

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Fig. 9: shows output voltage waveform for the three phases.

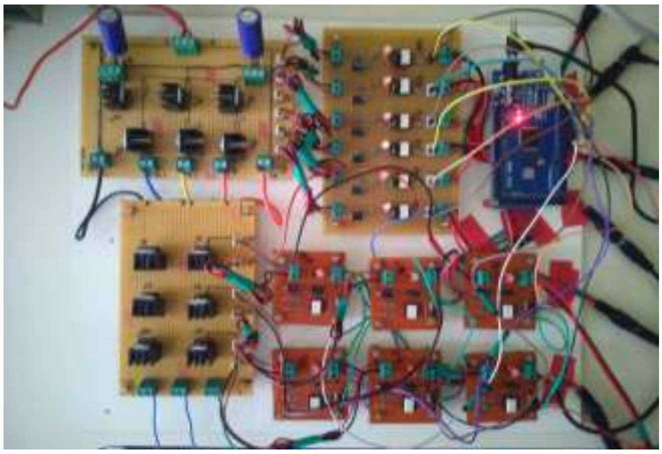

Fig.10: T-Type Inverter prototype

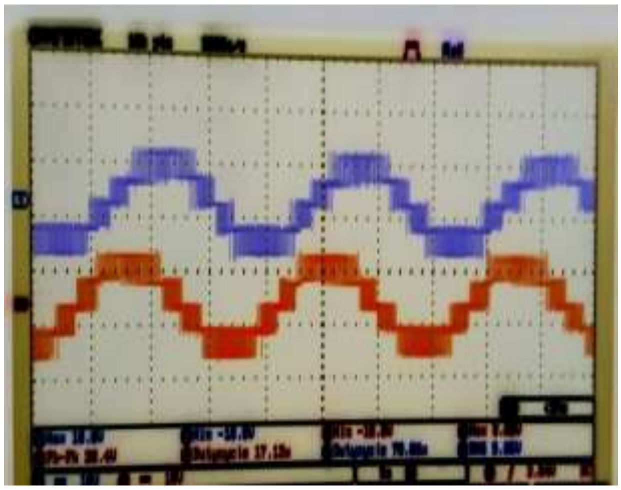

Fig.11: T-Type Inverter line to line volage of two phases

The NPC topology shows a slight advantage in voltage distortion reduction, the T-Type inverter is far superior in minimizing current distortion. This suggests that hardware implementation of T-Type inverters may provide better power quality in renewable energy applications where current distortion needs to be minimized. In both cases THI reference signal is slightly better than sine wave signal.

5. CONCLUSION

The study of the T-Type Multilevel Inverter (T-MLI) demonstrates its potential for high-efficiency power conversion with minimized total harmonic distortion (THD), making it a viable solution for renewable energy applications. Through MATLAB/Simulink analysis, the performance of the inverter has been evaluated, showcasing its ability to produce high-quality output. Additionally, the implementation of Pulse Width Modulation (PWM) techniques has further optimized the inverter operation, leading to improved stability and efficiency. The development of a hardware prototype validates its practical applicability and paves the way for real-world deployment in sustainable energy systems.

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