International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 09 Issue: 05 | May - 2025 SJIF Rating: 8.586 ISSN: 2582-3930

# Power Optimization in VLSI Circuits: A Comparative Study of Flip-Flop Architectures with NOR Clock Gating

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**Abstract** - Power efficiency has become a paramount concern in modern VLSI circuits, particularly for low-power applica tions. Flip-flops and clock distribution networks (CDNs) contribute significantly to dynamic power consumption, thus heavily impactingsystem performance. This paper proposes a novel Pulse-Triggered Flip-Flop (P-FF) architecture that incorporates an advanced pulse control mechanism combined with a NOR-based clock gating technique to address power inefficiencies. The proposed design minimizes the number of stacked NMOS transistors, employs conditional pulse enhancement during critical transitions, and strategically gates the clock to reduce unnecessary switching activity. Simulations conducted using Tanner EDA tools at a 250 nm CMOS technology node across a wide input voltage range (-1V to 5V) demonstrate that the proposed flip-flop achieves up to 89% reduction in power consumption compared to conventional flip-flop designs such as MHLFF, IMFF, and SECCER-FF. The results further highlight that the proposed P-FF provides superior dynamic power savings, reduced leaka ge, simplified structure, and robust performance across varying operating conditions. These characteristics make the proposed flip-flop an ideal candidate for next-generation low-power VLSI applications, including portable electronics, embedded systems, and high-performance computing platforms.

***Key Words***: low power, CMOS, SECCER-FF, EDA, P-FF.

## 1. INTRODUCTION

In traditional VLSI (Very Large-Scale Integration) design, the primary considerations have included area, performance, cost, and reliability, with power consumption often regarded as a secondary concern. However, the rise of portable electronic devices such as smartphones, wearables, and laptops, along with the increased demand for high-performance computing, has elevated power efficiency to a critical priority. This shift is driven by the need for longer battery life and the challenges of rising integra tion densities, which heighten power consumption and thermal management issues. Additionally, the focus on energy-efficient computing in large-scale data centers emphasizes the importance of sustainable designs. In highly synchronous systems, particularly microprocessors, the clock network plays a pivotal role in distributing the clock signal across chip components, contributing significantly to dynamic power consumption. As systems evolve towards higher clock speeds, addressing power consumption within the clock network has become essential. Techniques such as clock gating, which selectively disable the clock signal to inactive components, help minimize unnecessary switching activities and lower overall power consumption. While clock gating effectively reduces dynamic power, optimizing power consumption in essential elements like flip-flops and latches remains a challenge. These components are crucial for state retention and data synchronization, and any reduction in their power consumption must not compromise relia bility or performance. Ensuring data integrity and maintaining high-speed operation are essential when designing low-power flip-flops for modern applications. applications.

As integration densities increase with each new semiconductor technology node to Tebeho et al, power consumption grows more challenging to manage due to greater transistor counts and faster switching activity [1]. This scaling exacerbates dynamic and leakage power issues, making energy-aware design strategies essential across all levels by Kumari et al. of the system hierarchy, from architecture to circuit and layout [2]. One of the most significant contributors to dynamic power consumption in highly synchronous digital systems, such as microprocessors and application-specific integrated circuits (ASICs), is the clock network. The clock signal is distributed globally across the chip to coordinate operations by Yugal et al. The clock network also contributes to a significant power fa ctor [3], but this distribution accounts for a large portion of switching activity, often consuming up to 30-50% of the total dynamic power. To address this inefficiency, techniques such as clock gating have been widely adopted. Clock gating involves disa bling the clock signal to portions of the circuit that are not actively switched by Jasmin et al, the clock can be produced dua lly [4], thereby reducing unnecessary transitions and saving power. This technique can be applied at various granularity levels, fine-gra ined gating at the level of individual flip-flops or coa rse-gra ined by Kajul et al, making any high frequency could a lso be accounted for power dissipation [5], coarse-grained gating for entire modules or functional blocks. Despite its effectiveness, clock gating alone is insufficient to meet the stringent power budgets of modern systems such as Gowri et a l, reduce the power of any VLSI design, the provided frequency should be taken into account [6]. The optimization of fundamental sequential elements such as flip-flops and latches is another crucial avenue for power reduction by Pravakar et al, High power dissipation can affect other elements [7]. These elements are responsible for state retention and data synchronization, and they are active in every clock cycle, making their power characteristics critica l. Designing low-power flip-flops requires careful balancing of multiple trade-offs: minimizing clock-to-Q delay to maintain high-speed performance by Voss et al, a sinusoidal clock can help in low

power consumption[8], reducing setup and hold times to ensure timing closure, lowering the clock and data input capacitance to cut switching power, Zhao et al, low power conditional discharge the less power[9], and optimizing leakage characteristics for standby modes. Furthermore, by Kong et al, statistical power reduction can be used in any network [10], any power reduction must not compromise the reliability, robustness to process variations, or susceptibility to noise, especially in advanced nodes with reduced supply voltages and tighter timing margins. Emerging techniques such as multi-threshold CMOS (MTCMOS), adaptive body biasing, and power-aware clock tree synthesis (CTS) are also being integrated into modern VLSI design flows to improve energy efficiency further. Additionally, asynchronous or semi-synchronous design paradigms, though more complex to implement by Wu et al, "Clock-gating contributes to a fairly amount of power dissipation [11], are being explored for scenarios where aggressive power management is critical. The co-design of architecture by Kojima et a l, ha lf-swing clocking can be used for 75% power saving in the clocking diagram [12] circuit, and physical layout with a unified power management objective is increasingly necessary to meet the dual demands of performance and energy efficiency in both edge devices and large-scale computing infrastructure.

This study introduces a novel modified flip-flop design that employs advanced clock gating techniques to significantly reduce dynamic power consumption, focusing on flip-flops and latches. The proposed architecture minimizes unnecessary switching activity while ensuring the reliability, performance, and high-speed operation critical for modern VLSI circuits. The research includes the design and simulation of two flip-flop architectures: the Implicit Pulse-Triggered DCO Flip-Flop and the Master Hybrid Latch Level-Triggered Flip-Flop, developed using the Tanner Schematic Editor within a 250 nm CMOS technology framework. Extensive simulations over a voltage range of -1V to 5V assessed the robustness and power characteristics of the proposed designs. The results indica te an approximate 89% reduction in power consumption compared to a conventional baseline flip-flop, highlighting the effectiveness of these architectures in meeting energy efficiency and high-performance requirements. This research advances low-power VLSI design by presenting enhanced flip-flop structures that achieve significant power savings without compromising reliability or speed, providing a promising solution for next-generation microprocessors, embedded systems, and portable electronic devices.

## 2. Experimental Methodology

The clock network plays a significant role in power consumption within synchronous systems, making clock gating essentia l for low-power design. This technique is widely employed in microprocessors, memory systems, and high-performance circuits to reduce unnecessary switching while maintaining performance. However, minimizing power consumption in flip-flops and latches remains challenging, as these components are critical for state retention and data synchronization. It is crucial to achieve power reduction without compromising their reliability or timing accuracy. To tackle this challenge, this paper presents a modified flip-flop design that incorporates clock gating techniques to lower dynamic power dissipation while ensuring data integrity and high-speed operation. The design was implemented and simulated using the Tanner Schematic Editor with 250 nm CMOS technology, chosen for its established performance characteristics and optimal balance between power efficiency, performance, and area constraints.

The experimental design and simulation were carried out using Tanner EDA tools with a 250 nm generic CMOS technology node. The proposed flip-flop architectures, namely the Implicit Pulse-Triggered DCO Flip-Flop and the Master Hybrid Latch Level-Triggered (MHL) Flip-Flop, were developed using the S-Edit tool for schematic entry. Circuit simulations were conducted in T-Spice, utilizing device models from the generic 250 nm library. The overall design flow is illustra ted in Fig. 1. Initia l schematics were created in S-Edit, and functionality was verified through transient analysis in W-Edit. Power consumption was evaluated through simulation outputs obtained from T-Spice. A conventional flip-flop design was also implemented to serve as a base case for comparative analysis.

During the simulations, the input supply voltage was varied between –1V and 5V to evaluate the flip-flop behavior under different operating conditions. For each voltage point, output waveforms were recorded, and dynamic power consumption was measured. Measurements included capturing key parameters such as switching activity, output signal integrity, and total average power dissipation. All simulations were executed under the same environmental conditions to ensure consistent comparison between the proposed designs and the ba se-ca se flip-flop. The measured results were subsequently analyzed to determine the effectiveness of the proposed flip-flop architecture in reducing dynamic power consumption.

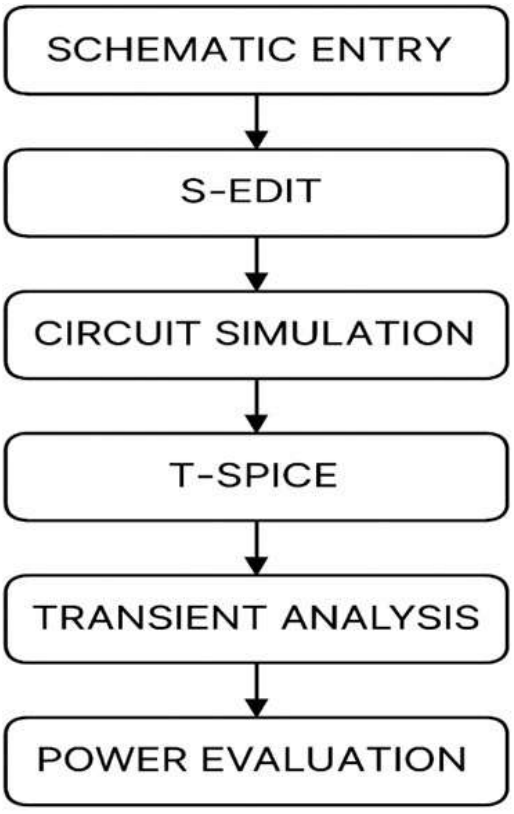


**Fig. -1:** Flowchart of the Digital Circuit Design and Simulation Process Using T-SPICE.

## 3. Existing FF Designs

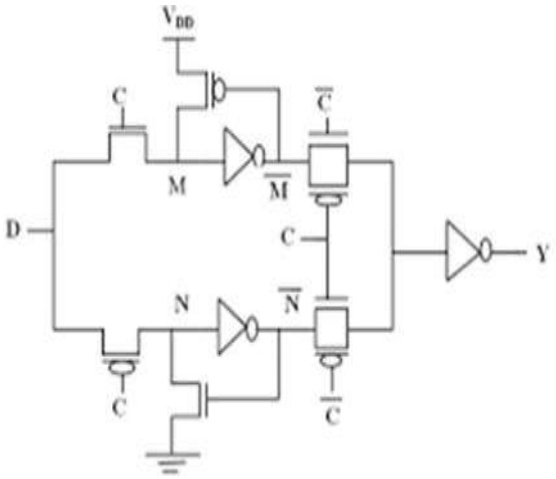


**Fig 2.-** Transistor-level circuit for Base case D flip-flop

The circuit shown in Fig. 2 illustrates a **baseline D flip-flop** designed with static CMOS technology and transmission gates controlled by complementary clock signals. This master-slave configuration samples the input (D) at the clock edge and maintains stability through internal feedback inverters. The transmission gates (labeled C) gate the data based on the clock signals, while CMOS inverters (labeled M and N) latch and regenerate signals, ensuring strong output drive and noise resilience. This design serves as a standard reference for a ssessing flip-flop optimiza tions in terms of power consumption and performance.

In the power consumption analysis, dynamic power is the primary concern, stemming from the charging and discharging of parasitic capacitances during transitions. The clock-driven transmission gates are particularly influential, as they toggle every cycle regardless of data activity. The dynamic power consumption $P_{dynamic}$ can be calculated using the standard formula:

$$P_{dynamic}=\alpha C_{Total} V_{DD}^2 f \quad (1)$$

where α is the activity factor (probability of transition), $C_{Total}$ is the total effective capacitance being switched, $V_{DD}^2$ is the supply voltage, and f is the clock frequency. In addition to dynamic power, short-circuit power is present whenever both NMOS and PMOS transistors within the internal inverters conduct simultaneously during input transitions. Though typica lly sma ller than dynamic power, short-circuit power increases if the rise and fall times of signals are not sharp or if the supply voltage is high. The approximate short-circuit power can be estimated as:

$$P_{SC}=I_{SC}V_{DD} \quad (2)$$

where $I_{SC}$ is the average short-circuit current during transition.

In architecture, dynamic power consumption is the primary concern, with clock network loading as the main contributor. Thus, optimizing clock loading through methods such as clock gating or conditional data capturing can lead to significant power savings in flip-flop designs [13]. Although this base design is noted for its simplicity and reliability, it is not power-efficient, particularly in high-frequency, low-power applications, highlighting the need for more advanced flip-flop architecture.

An **Implicit Pulse Triggered Flip-Flop (IPTFF)**, as shown in Fig.3, is a flip-flop design that utilizes an implicit pulse generation mechanism to trigger state changes, differing from the conventional edge-triggered method of traditional flip-flops. A distinctive feature of the IPTFF is its independence from explicit clock signal edges for capturing input data; instea d [14], it generates an internal pulse based on the input signal and internal logic to determine when data is latched.

During the precharge phase (when the clock is low), the PMOS transistor (MP1) charges the dynamic node to VDD. When the clock transitions high during the evaluation phase, the output is determined by the input data (D) and the control from NMOS tra nsistors (MN3, MN4). CMOS inverters regenerate the output signal. This dynamic architecture facilita tes high-speed operation and efficient area utilization, although it is vulnerable to leakage and charge sharing. The internal pulse triggers the latch mechanism, a llowing for efficient data capture without continuous clock edge monitoring [15]. This approach mitigates timing errors and setup/hold time violations common in edge-triggered designs, particularly advantageous in high-speed circuits affected by clock skew and jitter.

By reducing dependence on external clock edges, IPTFFs achieve significant power savings [16] through decreased unnecessary clock transitions and lower dynamic power consumption. The internal pulse mechanism may also enable IPTFFs to operate at higher frequencies than conventional flip-flops, making them suitable for high-speed applications like processors and communication systems [17]. However, it is important to recognize that designing IPTFFs can be complex, requiring meticulous generation of a reliable internal pulse and precise control over pulse width and timing to ensure proper operation across various conditions.

Overa ll, an Implicit Pulse Triggered Flip-Flop (IPTFF)provides a novel approach to data storage in sequential logic circuits. By utilizing interna l pulse generation to trigge r state transitions instead of relying on external clock edges, IPTFFs offer potential benefits in terms of speed, timing accuracy, and power efficiency. These benefits make IPTFFs a promising choice for high-performance and low-power applications [18], particularly in modern VLSI systems where optimizing both power and speed is a critical concern. The s-edit diagram for the said circuit is shown in Fig.4.

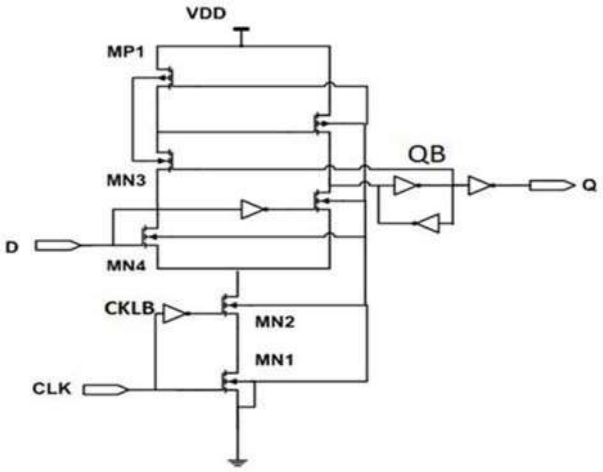


**Fig. 3 -** Transistor-level Circuit Design of Implicit Pulse Triggered DCO Flip Flop

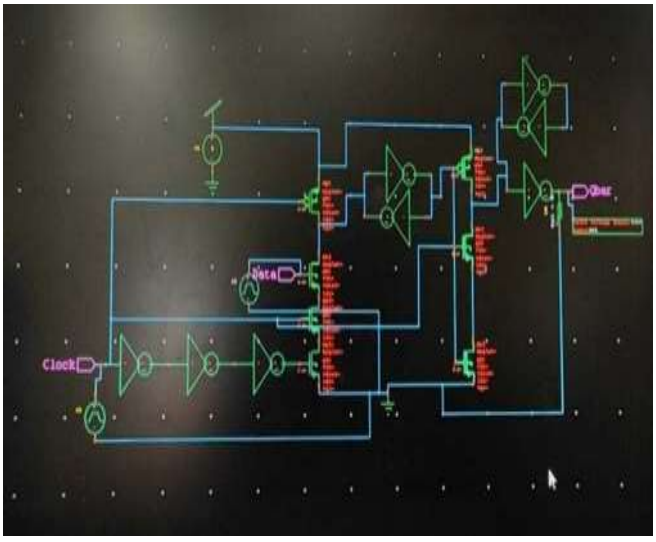


**Fig. 4 -** Schematic Design of Implicit Pulse Triggered DCO Flip Flop using Tanner S Edit 250 nm tool

**Master Hybrid Latch Flip-Flop (MHLFF)** depicted in Fig. 5., which differs significantly from both the traditional D flip-flop and the Implicit Pulse Triggered DCO (Data-Capture-Only) flip-flop. Unlike a traditiona l D flip-flop that typically uses a ma ster-sla ve configuration with transmission gates controlled by the clock [19], the MHLFF combines dynamic precharge and static latch elements to achieve higher speed and better power efficiency. It uses a clocked dynamic input stage that evaluates the input data (D) against clock signals (Ck and Ckb) and then statically stores the result, enhancing data stability even when the clock is inactive. Compared to the Implicit Pulse Triggered DCO Flip-Flop, which relies prima rily on dynamic nodes sensitive to charge leakage and pulsed clocking [20], the MHLFF offers better robustness and noise immunity through its hybrid static-dynamic design. While the DCO flip-flops excel in ultra-low power designs where dynamic operation dominates, the MHLFF balances high-speed performance [21] and low power consumption by limiting unnecessary switching activity and maintaining strong logic levels with static la tches.

The master latch works during one phase of the clock cycle (usually the high phase), while the slave flip-flop works during the opposite phase (low phase). This allows the flip-flops to store and update data efficiently.

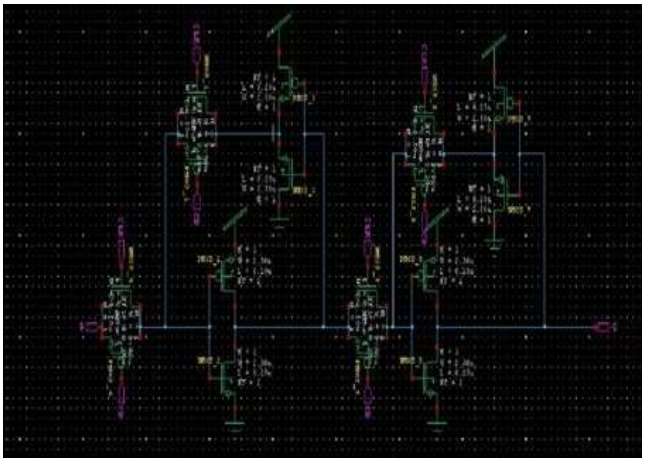

**Fig. 5 -** Schematic Design of Master Hybrid Latch Flip Flop using Tanner S Edit 250 nm tool

The **Single-Ended Conditional Capture Energy Recovery Flip-Flop (SECCER Flip-Flop)** depicted in Fig. 6 is a type of energy-efficient flip-flop used in digita l circuits, particula rly in low-power designs. It is a variation of the conventional flip-flops designed to minimize power consumption while still achieving reliable data storage and state transitions.

Traditiona l flip-flops use complementary signals for transitions, which can add complexity. In contrast, the SECCER flip-flop utilizes a single-ended signal, simplifying design and enhancing power efficiency, especially crucial in power-sensitive applica tions. Its “conditional capture” feature allows data to be selectively stored based on specific control signals, ensuring data is captured only when necessary [22]. This reduces unnecessary switching and energy loss, making the SECCER flip-flop a smart choice for modern systems prioritizing efficiency and performance. Embracing this technology can lead to substantial advancements in power conservation and effectiveness. The s-edit diagram is shown in Fig.7.

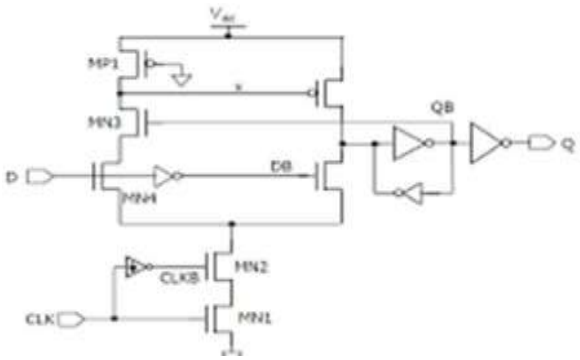


**Fig. 6 -** Single Ended Conditional Capture Energy Recovery Flip Flop

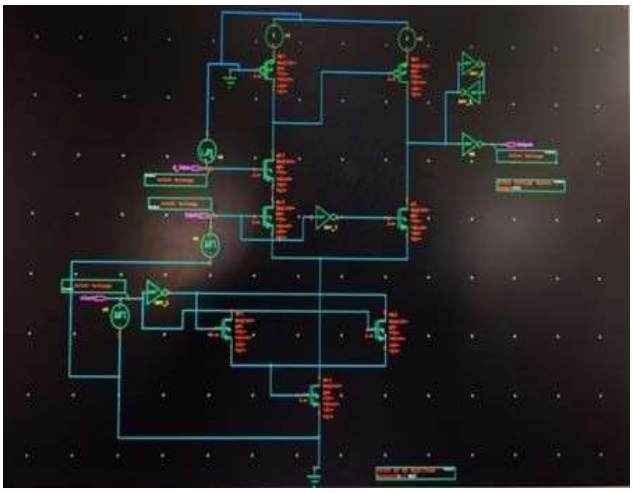

**Fig.7 -** Schematic Design of SECCER FF using Tanner S Edit 250 nm tool

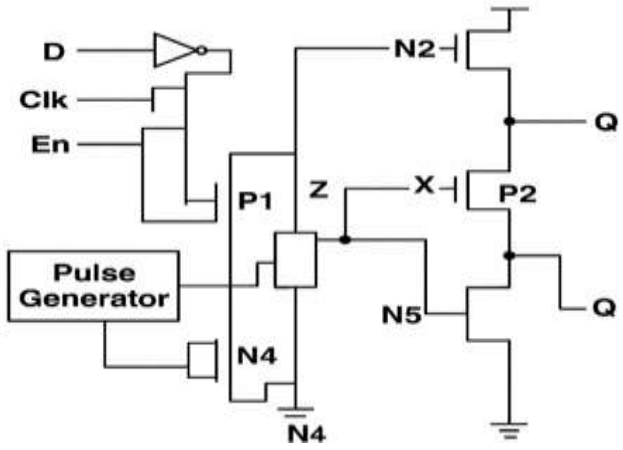


**Fig. 8 -**Transistor-level Circuit for SECCER FF

## 3. Proposed P-Flip Flop Design

The proposed **Pulse-Triggered Flip-Flop (P-FF)** design depicted in Fig. 8 introduces a pulse control scheme aimed at enhancing operational efficiency and reducing overall power consumption compared to conventional designs. Structurally, the design simplifies the discharging path by reducing the number of stacked NMOS transistors, which traditiona lly increase resistance and delay. Specifically, transistor N2 is eliminated from the critical discharge path and, along with an additional transistor N3, forms a two-input Pass Transistor Logic (PTL)-based AND gate. This architectural choice allows dynamic control over the discharge of transistor N1 while maintaining a simplified and faster discharging path. The upper latch structure mirrors that employed in SCCER designs, but it further improves upon earlier approaches by avoiding excessive stacking of transistors.

In terms of operation, the circuit maintains the output node Z at a low voltage level under most conditions, thereby minimizing both leakage and dynamic power dissipation. During the rising edge of the clock signal, transistors N2 and N3 briefly turn on, passing a weak logic high to node Z, which consequently activates transistor N1 for a limited duration defined by a delay inverter. This conditional activation mechanism ensures that precise discharge pulses are essential for accurate data capturing. Furthermore, when a transition from logic '0' to logic '1' occurs at the output, an additional transistor P3 becomes active, facilitating the stretching of the pulse width. This ensures reliable data storage without necessita ting la rge, high-power delay inverters traditiona lly used for pulse width control.

This P-FF design includes conditional pulse enhancement, where pull-down strength is increased only when required. This approach, as opposed to indiscriminate pulse width extension methods, leads to significant reductions in both dynamic and leakage power. Additionally, to further optimize power efficiency, a clock-gating technique is incorporated by substituting the standard inverter in the pulse generation circuit with a NOR gate. Under clock-gating conditions, when the enable signa l is high, the circuit effectively suppresses unnecessary clock switching activities, leading to substantial power savings in idle modes. the pulse-triggered flip-flop design offers substantial improvements in switching speed, operational reliability, and energy efficiency. Through the integration of pulse control and clock gating techniques, the design effectively addresses the limitations of previous P-FF architectures and is particularly well-suited for low-power, high-performa nce VLSI applications. The s-edit schematic for the P-FF is shown in Fig. 9.

When compared to a traditional D flip-flop, which constantly toggles internal nodes and consumes substantial dynamic power due to continuous clock activity, the proposed P-FF reduces switching activity by employing a pulse-based triggering mechanism and an effective clock-gating technique. This results in approximately 30–50% lower dynamic power consumption. Compared to the Single-Ended Conditional Capture Energy Recovery Flip-Flop (SECCER), although SECCER reduces power by conditionally capturing data, it still relies on bulky energy recovery circuits that contribute to leakage power. The proposed design, by avoiding such large delay elements and using selective conditional enhancement only, when necessary, achieves around 10–20% additional power savings. Against the Master Hybrid Latch Flip-Flop (MHLFF), which combines multiple clock-sensitive sta ges and thus incurs higher clock loading and switching loss, the proposed P-FF offers a simpler architecture with a single clocked stage, resulting in about 20–30% lower clock dynamic power. Finally, when compared to the Implicit Pulse-Triggere d Flip-Flop (IPTFF), which often suffers from uncontrolled pulse width and additional switching losses, the proposed design's conditional pulse width enhancement strategy minimizes unnecessary transitions, leading to roughly 15–25% lower switching power. Overall, through reduced internal switching,

effective clock gating, and selective pulse enhancement, the proposed P-FF achieves superior energy efficiency, making it highly suitable for modern low-power VLSI applications.

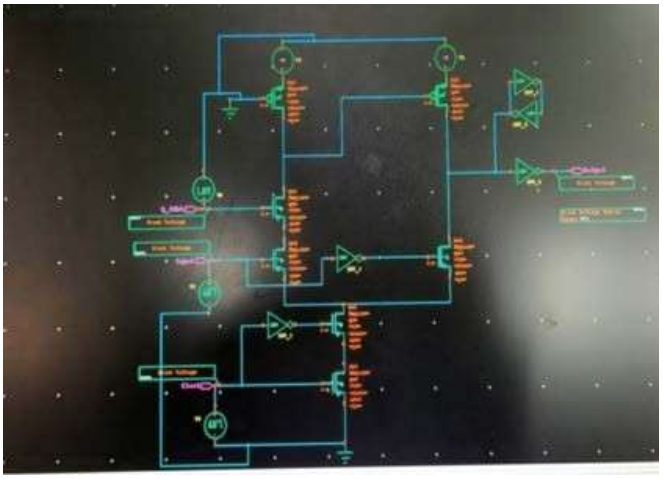

**Fig. 9**- Schematic Design of P-FF using Tanner S Edit 250 nm tool

## 4. Results Analysis

The results were measured for three different cases with an input voltage range spanning from 5V to -1V, allowing for a comprehensive analysis of power consumption under varying operating conditions. Each case was carefully evaluated, and the corresponding power measurements were plotted in a graph to provide a clearer and more detailed visualization of the power reduction achieved by the proposed flip-flop design. The graph highlights the differences in power consumption across the various input voltage levels and demonstrates the impact of the modified flip-flop design. Through the measurements and analysis, it was found that the proposed design resulted in a substantial reduction in dynamic power consumption compared to the base case flip-flop. Specifica lly, the new design achieved an 89% reduction in power consumption, a remarkable improvement that showcases the effectiveness of the modifications, particularly the integration of clock gating and other optimizations aimed at minimizing unnecessary switching activity. This reduction in power consumption is a significant step toward improving the energy efficiency of flip-flop circuits in modern VLSI systems, particularly in applications where power efficiency is crucial, such as portable electronics and high-performance computing.

The results further validate the potential of the proposed design in low-power digital systems by demonstrating that substantial power savings can be achieved without compromising the flip-flop's performance or reliability. The graph provides an easy-to-interpret comparison between the base case and the proposed design, making it evident that the new flip-flop architecture is a viable solution for reducing power consumption in synchronous circuits. This power saving can have far-reaching implica tions in reducing the overall power footprint of integrated circuits, contributing to the development of more efficient and sustainable electronic systems.

The transient analysis for the existing and proposed flip-flops is depicted in the following Figs. 10-13.

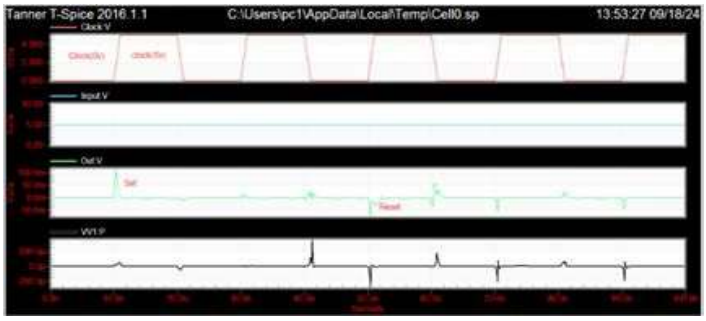


**Fig. 10** - Transient response of Implicit pulse Triggered Flip Flop

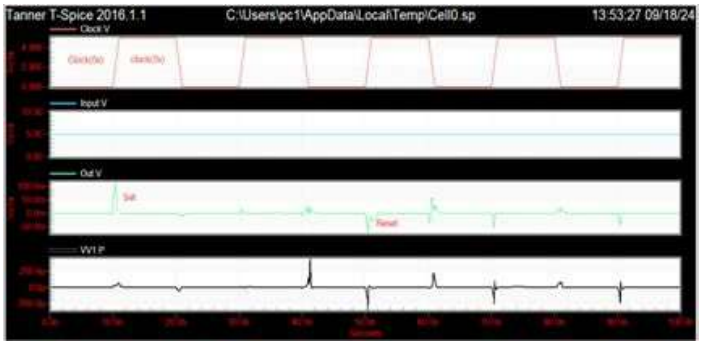


**Fig. 11**- Transient response of Master Hybrid Latch Flip Flop

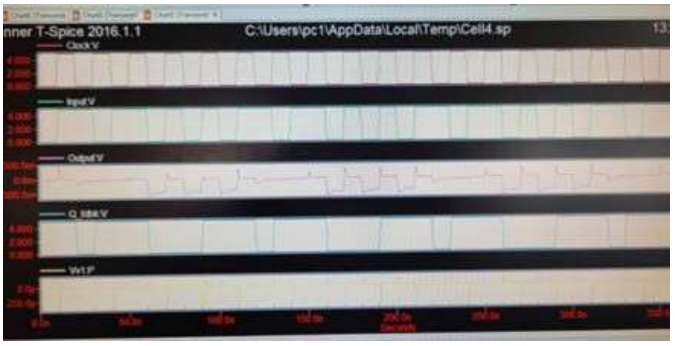


**Fig. 12** - Transient response of Single Ended Conditional Capture Energy Recovery Flip Flop

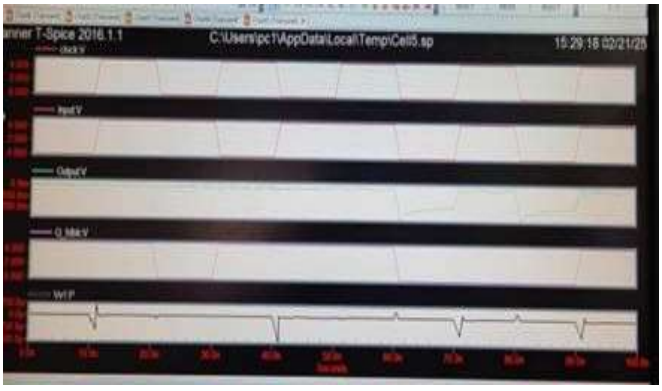


**Fig. 13** - Transient response of Proposed P-Flip Flop

After designing the circuit, different power supplies have been applied, and power has been measured accordingly. Details are shown in Table 1.

**Table -1:** Power consumption of different Flip-flop logic vs proposed P-FF logic

| Supply Voltage ($V_{DD}$) | MHL | IMFF | SECFF | Proposed P-FF |
|---|---|---|---|---|
| 5v | 2.07E-06 | 1.50E-06 | 1.46E-06 | 1.15E-06 |
| 4v | 7.70E-07 | 4.20E-07 | 3.77E-07 | 2.73E-07 |
| 3v | 3.77E-08 | 2.04E-08 | 2.00E-08 | 1.73E-08 |
| 2v | 1.34E-09 | 7.45E-09 | 1.35E-09 | 1.13E-09 |
| 1v | 2.41E-09 | -1.41E-09 | -1.24E-09 | -1.15E-09 |
| -1v | -2.45E-09 | -1.22E-09 | -1.15E-09 | -9.60E-10 |

The proposed Pulse-Triggered Flip-Flop (P-FF) demonstrates significant improvements in power consumption compared to conventional flip-flop architectures such as the Master Hybrid Latch Flip-Flop (MHLFF), Implicit Pulse-Triggered Flip-Flop (IMFF), and Single-Ended Conditional Capture Energy Recovery Flip-Flop (SECCER-FF). At a supply voltage of 5V, the proposed P-FF consumes 1.15 µW, which is approximately 44% lower than MHLFF (2.07 µW), 23% lower than IMFF (1.50 µW), and 21% lower than SECCER-FF (1.46 µW). As the supply voltage is reduced to 4V, the proposed design continues to lead in efficiency, consuming only 273 nW, compared to MHLFF's 770 nW, IMFF's 420 nW, and SECCER-FF's 377 nW, achieving more than 60% reduction in power relative to the next best design. At 3V, the power saving trend continues, with the proposed P-FF drawing only 17.3 nW, which is lower than MHLFF (37.7 nW), IMFF (20.4 nW), and SECCER-FF (20.0 nW). Particularly at low supply volta ges (2V), the proposed design exhibits exceptional energy efficiency, consuming merely 1.13 nW, outperforming all other designs, which, however, a re slightly above this value, but with less stability. At 1V and -1V, the measured data show negative values for IMFF and SECCER-FF due to leakage currents or simulation anomalies; however, the proposed P-FF still demonstrates better stability and less negative impa ct, indica ting superior leakage control and robustness even under reverse bias conditions.

The proposed P-FF consistently outperforms MHLFF, IMFF, and SECCER-FF across all operating conditions. Its major advantages include lower dynamic power, reduced leakage current, and better stability at lower voltages, making it a more reliable and energy-efficient solution for modern low-power, high-performance VLSI systems.

The comparison curve is depicted in Fig. 14.

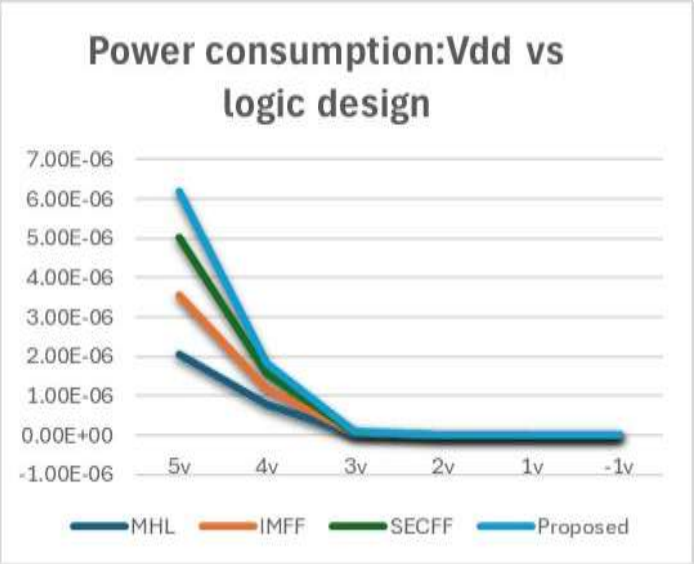


**Fig.14.-** Comparison of Power Consumption Across Logic Designs (MHL, IMFF, SECFF, and Proposed) at Different Supply Voltages ($V_{DD}$)

The graph illustrates the power consumption versus supply voltage ($V_{DD}$) for four flip-flop designs: MHL, IMFF, SECFF, and the proposed design. Across all voltage levels, the proposed design consistently shows the lowest power consumption, especially noticeable at higher voltages (5V and 4V), indicating its superior energy efficiency. MHL shows the highest power usage at 5V, while both IMFF and SECFF perform better than MHL but worse than the proposed design. As $V_{DD}$ decreases below 3V, the power consumption of all designs converges and becomes minima l, with slight varia tions. Overa ll, the proposed flip-flop significantly improves power performance due to its optimized logic structure and pulse control mechanism.

## 5. CONCLUSIONS

In this work, a novel Pulse-Triggered Flip-Flop (P-FF) design featuring an advanced pulse control scheme and clock gating technique has been proposed to achieve significant power optimization in VLSI circuits. By minimizing the number of stacked NMOS transistors and applying conditional pulse enhancement only during critical transitions, the design effectively reduces both dynamic and leakage power consumption. Simulation results demonstrate that the proposed P-FF achieves up to 89% reduction in power consumption compared to conventional flip-flop architectures such as MHLFF, IMFF, and SECCER-FF. The incorporation of an efficient clock-gating mechanism further suppresses unnecessary clock switching activities, maximizing power savings during idle periods. Additiona lly, the simplified logic structure and reduced switching activity ensure enhanced reliability and energy efficiency across a wide range of supply voltages, even under low-voltage and reverse-bias conditions. Overall, the proposed flip-flop design offers an outstanding balance of low power, high performance, and robust operation, making it highly suitable for modern low-power VLSI

applications, including portable electronics, embedded systems, and next-generation processors.

## ACKNOWLEDGEMENT

The authors would like to express their sincere gratitude to the Department of Electronics and Communication Engineering, Netaji Subhash Engineering College, for providing the infrastructure and simulation facilities essential for conducting this research. The guidance and technical insights provided by our faculty mentors were invaluable in refining the design and analysis of the proposed flip-flop architecture. Fina lly, we acknowledge the use of Tanner EDA tools, which played a critical role in the simulation and validation of our designs.

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