

# POWER QUALITY ENHANCEMENT OF DIODE CLAMPED MULTILEVEL INVERTER USING 3RD HARMONIC INJECTION

Dr. Reeta Pawar<sup>1</sup>, Mr. Rajesh Kumar Vishwakarma<sup>2</sup>, Mr. Balwant Singh Parihar<sup>2</sup>

Professor<sup>1</sup>, Associate Professor<sup>2</sup>

Electrical & Electronics Engineering

Madhyanchal Professional University, Bhopal<sup>1,2,3</sup>

[reetapawar2010@gmail.com](mailto:reetapawar2010@gmail.com)<sup>1</sup>, [rjsh\\_vishwakarma@yahoo.co.in](mailto:rjsh_vishwakarma@yahoo.co.in)<sup>2</sup>

[balwantparihar1012@gmail.com](mailto:balwantparihar1012@gmail.com)<sup>3</sup>

## ABSTRACT

The concept of multilevel power conversion has been gaining popularity mainly due to improved power quality, lower switching losses, better electromagnetic compatibility, and higher voltage capability. These converters are suitable in high-voltage and high-power applications due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltages with a limited maximum device rating. These improvements in power conversion are achieved by using multiple voltage steps strategy which is an essential reason for medium voltage operation to lowering  $dv/dt$  and reducing stress on motor winding insulations. Multilevel power conversion has been receiving increasing attention in past few years for high power applications.

**Keywords:** -Variations in load, Multilevel inverters, Semiconductor Devices.

## 1. INTRODUCTION

Multilevel inverters are the class of inverters in which the output voltage waveform composed of number of levels of voltage typically obtained from the capacitor voltage sources. Researchers suggested various topologies of the multilevel inverters i.e DCMLI, FCMLI, CMLI etc. Apart from the advantages there are some inherent problems associated with different topologies of the multilevel inverter like capacitor voltage unbalance, common mode voltage generation, voltage drift problems with increased voltage levels, Neutral Point Potential Variation (3-Level Diode Clamped Inverter). Hence the possible research areas in multilevel inverters are Unequal Ratings of Switching Devices, Capacitor Voltage Unbalance, High Voltage Rating for Blocking Diodes, Optimized modulation strategy, Real Power Flow Control, Common mode voltage reduction, Optimization of a soft-switching circuit

with inductor coupling, Voltage drift problems with increased voltage levels, Transformer-less Distribution System, Use of Optical Fibers for Sensors and Controls, Use of Advanced High-Voltage, High-Power Semiconductor Devices, Unequal duty of individual device, Switching Losses. some research are based on the analysis and comparison of these topologies among themselves on the basis of their cost, number of switching devices, capacitors, diodes used in the circuit of same level, THD in the output voltage for the same level and the magnitude of the output voltage produced.

## 2. CONCEPT OF MULTILEVEL INVERTERS

Multilevel inverter includes an array of power semiconductor devices and capacitors voltage sources, the output of which generates voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitors voltages to obtain high-voltage at the output, while the power semiconductors have to withstand only reduced voltages. We can observe a two level inverter generates an output voltage with two values (levels) with respect to negative terminal of the capacitor. While three and level inverter generates three voltages, and a nine-level inverter generates a nine level output voltages. In all this cases devices are not arranged in series but they are arranged in such way that, they gain the capability to generate such kind of voltages.

Herein, we should remember one important thing i.e. as the number of steps increases in the output waveforms; harmonic content comes down. Thus power quality of such waveforms will increase drastically. However, in order to generate step kind of waveforms in output side, different Multilevel based archetypes are successfully built and verified. But general principle of multilevel inverters is the synthesis of the AC voltage from several different voltage levels on the DC bus. As the number of voltage levels on the input DC side increases, the output voltage adds more steps which approach the sinusoidal wave.

### 2.1 2-LEVEL AND 3-LEVEL VOLTAGE SOURCE INVERTERS

A 2-level voltage source inverter, also known as half-bridge inverter is depicted in Figure 2.1.1 S1 and S2 are the two power switches which are AC activated for equal intervals to generate a 2-level square wave output waveform. Both S1 and S2 operate in strict complement sense so as to avoid the short circuit across the DC voltage source. Output voltage levels with corresponding switch states are given in table 2.1.1 The structure of a 3-level voltage source inverter, also known as full-bridge inverter or H-bridge inverter along with its output is shown in Figure 2.1.2 It employs four power switches S1, S2, S3 and S4. Similar to the half-bridge inverter, S1 and S3 operate in strict complement sense to avoid short circuit across the DC voltage source. Same is the case for switches S2 and S4. Table 2.1.2 explains how power

switches in full-bridge inverter are activated.

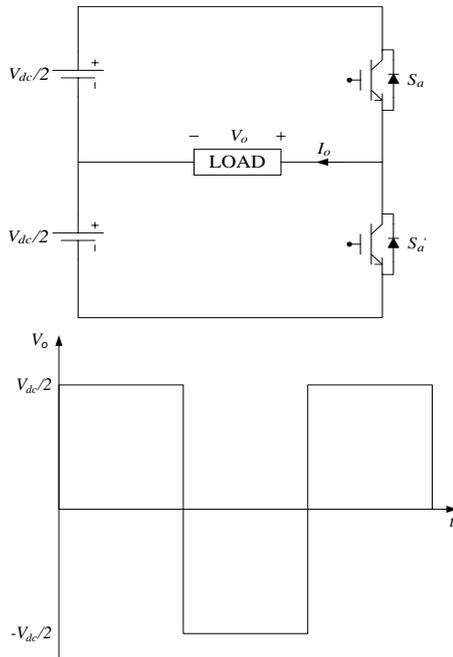


Figure 2.1.1 half bridge inverter and its output

Table 2.1.1 Switching Pattern of a Half-Bridge Inverter

ON state switch	Output voltage $V_o$
$S_1$	$+V_{DC}/2$
$S_2$	$-V_{DC}/2$

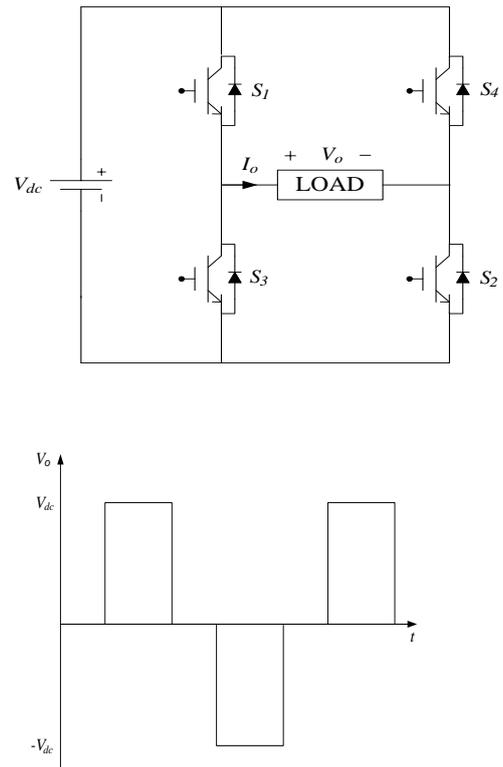


Figure 2.1.2 Full bridge inverter

Table 2.1.2 Switching Pattern of a Full-Bridge Inverter

ON state switch pairs	Output voltage $V_o$
$S_1, S_2$	$+V_{DC}$
$S_3, S_4$	$-V_{DC}$

Inverters employing 2-level waveform are rarely used in practice due to presence of relatively large 3<sup>rd</sup> and 5<sup>th</sup> order harmonics and high dv/dt stress. Although a 3-level waveform is better than a 2-level waveform and can be used for household applications like uninterruptible power supplies

(UPS), still there is significant presence of lower order harmonics which can cause reduction in efficiency of the circuit. As an alternative to these issues, multilevel voltage source inverters were introduced.

### 2.2 MULTILEVEL INVERTERS

Multilevel inverters are recognized by their stepped output waveform. The generalized stepped waveform for a single-phase  $N$ -level multilevel inverter is shown in Figure 3.3 The waveform is composed of equal positive and negative halves of  $(N-1)/2$  voltage levels wherein a sine wave can be approximated as shown.

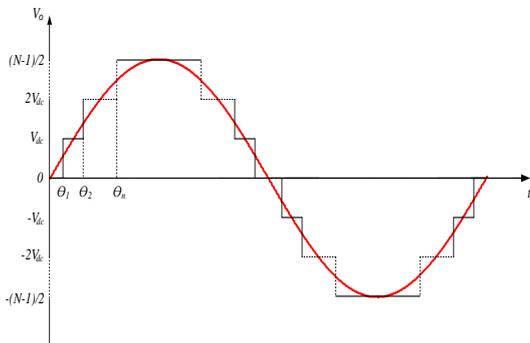


Figure 2.2.1 Generalized stepped waveform of multilevel inverters

### 2.3 MULTILEVEL INVERTERS

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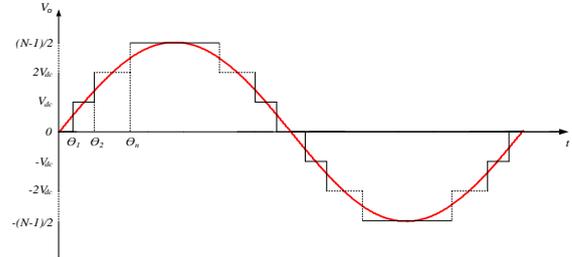


Figure 2.3.1 Generalized stepped waveform of multilevel inverters

### 2.4 MULTILEVEL INVERTER STRUCTURES

Three different major multilevel converter structures have been applied in industrial applications: cascaded H-bridges converter with separate DC sources, diode clamped, and flying capacitors

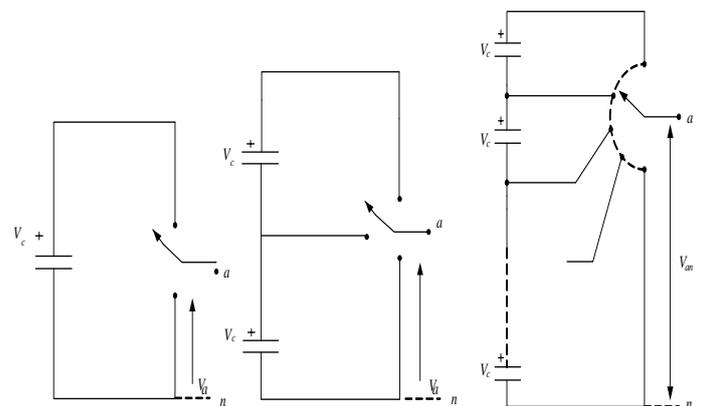


Figure 2.4.1 one phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels

## 2.5 CLASSIFICATION OF MULTILEVEL INVERTERS

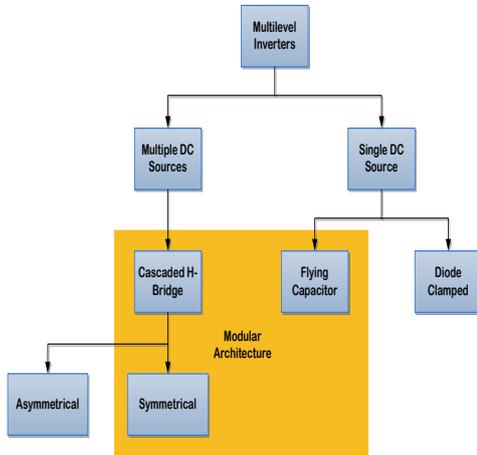


Figure 2.5.1 Multilevel inverter classifications

## 2.6 DIODE CLAMPED MULTILEVEL INVERTER

Diode-clamped multilevel inverter is the name given to neutral-point clamped PWM inverter extended to higher number of levels [3, 4]. The diode-clamped multilevel inverter has found wide acceptance for its capability of high voltage and high efficiency operation. Figure 3.6

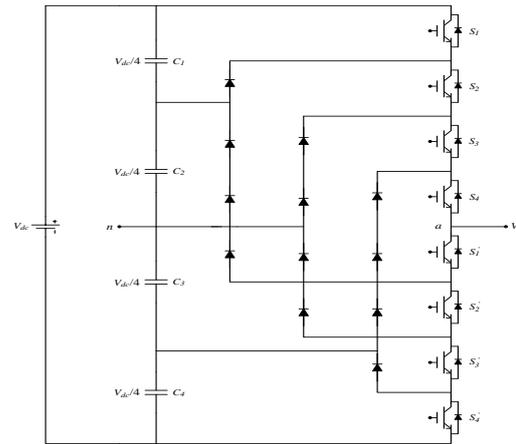


Figure 2.6.1 5-level Diode-clamped inverter

Table 2.6.1 Switching Pattern of Diode-Clamped Multilevel Inverter

Output Voltage $V_o = V_{an}$	Switch states							
	$S_1$	$S_2$	$S_3$	$S_4$	$S_1'$	$S_2'$	$S_3'$	$S_4'$
$V_{DC}/2$	1	1	1	1	0	0	0	0
$V_{DC}/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-V_{DC}/4$	0	0	0	1	1	1	1	0
$V_{DC}/2$	0	0	0	0	1	1	1	1

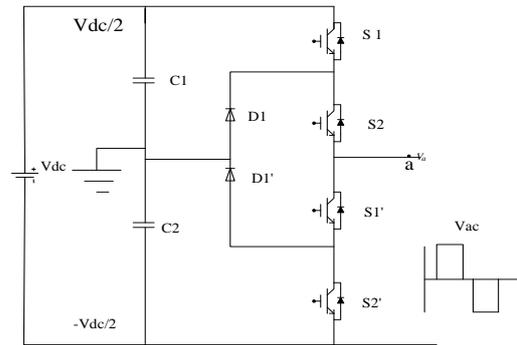
**Table-2.6.2 Switching States In One Leg of the Three-Level Diode Clamped Inverter**

Switch status	state	Pole voltage
$S_1 = \text{on}, S_2 = \text{on}$ $S_1 = \text{off}, S_2 = \text{off}$	$S = +ve$	$V_{ao} = V_{DC} / 2$
$S_1 = \text{off}, S_2 = \text{on}$ $S_1 = \text{on}, S_2 = \text{off}$	$S = 0$	$V_{ao} = 0$
$S_1 = \text{off}, S_2 = \text{off}$ $S_1 = \text{on}, S_2 = \text{on}$	$S = +ve$	$V_{ao} = - V_{DC} / 2$

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$S_1 = \text{off}, S_2 = \text{on}$ $S_1 = \text{on}, S_2 = \text{off}$	$S = 0$	$V_{ao} = 0$
$S_1 = \text{off}, S_2 = \text{off}$ $S_1 = \text{on}, S_2 = \text{on}$	$S = +ve$	$V_{ao} = - V_{DC} / 2$

Figure 2.6.2-level Diode-clamped inverter



### 3. CONCLUSION

The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series of capacitors. The concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels where two capacitors are connected across the DC bus resulting in one additional level. The additional level was the neutral point of the DC bus. However, with an even number of voltage levels, the neutral point is not accessible, and the term multiple point clamped (MPC) is sometimes applied. Due to capacitors voltage balancing issues, the diode-clamped inverter implementation has been limited to three level. Because of industrial developments over the past several years, the three level inverter is now used extensively in industrial application.

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