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Power Quality Improvement in Multifeeder Using MC-UPQC

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Abstract: Power Quality (PQ) issues have been a major concern as there is increased load demand and usage of variety of nonlinear loads. The innovation of Flexible AC Transmission System (FACTS) devices is a great way of solving PQ issues. Many devices like UPFC, D-STATCOM, and TCPST are emerging and are widely used for PQ improvement. In this paper, the Multi Converter Unified Power Quality Conditioning (MC-UPQC) System will be used for improving PQ in multi-bus systems. The system of MC-UPQC contains one shunt and two series Voltage Source Converter (VSCs). The conventional methodology contains one shunt and one series static devices. In the proposed methodology, two series VSCs will be used for further reduction of overall THD value. The simulation results of a reduction in THD and an improvement in PQ are compared with and without the proposed using MATLAB.

Keywords—PQ, MC-UPQC, series VSC, shunt VSC, MATLAB.

I. INTRODUCTION

The use of nonlinear loads in modern power distribution system has increased drastically in recent years. With increasing applications of nonlinear and power electronic converters in distribution systems and industries, consumers are concerned not only about continuity of supply but also the quality of power being supplied. In addition to that, natural causes like lightning strikes on transmission lines also cause power quality problems such as transient voltage sag swell and interruption [1] . For smooth operation of sensible loads and complicated purposes a pure sinusoidal wave is need to be supplied.

Power quality issues such as voltage sags, swells, and harmonics can have a significant impact on the performance and reliability of electrical loads, leading to reduced efficiency and increased downtime. In multi-feeder systems, these power quality issues can be particularly challenging to address, as they can affect multiple loads simultaneously.

One promising solution for improving power quality in multi-feeder systems is the use of a multi converter unified power quality conditioner (MCUPQC). An MCUPQC is a device that is designed to improve the quality of electrical power by mitigating various power quality issues using multiple converters to provide active power compensation and reactive power compensation. [7] [8].

Here, a new configuration of a UPQC called the multi-converter unified power-quality conditioner (MC-UPQC) is presented. The system is extended by adding a series-APF in an adjacent feeder. MC-UPQC can be used for simultaneous compensation of voltage and current imperfections in both feeders by sharing power compensation capabilities between two adjacent feeders which are not connected. Here, power is distributed in two lines connected by the fact devices [10].

Figure 1 shown in theline diagram of proposed MC-UPQC system.

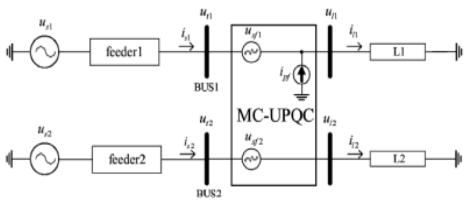

Fig: 1 single line diagram of a distribution system with MC-UPQC

In this paper, a new conventional controller is used with SPWM, generate the pulse to the converter connected to the distribution line cumulatively maintain the desired values by justified the performance of the MC-UPQC. First run the model without controller and next with PI controller [12]. At last, compare total harmonic distortion (THD) values with and without use of control technique [3] [4] [13]. The complete model and operation of MC-UPQC in section 2nd insection 3red shown a conventional control technique for control of MC-UPQC. Section4 defined simulated result with and without proposed system.

II. MC-UPQC SYSTEM CONFIGURATION

A. *Circuit Configuration*

The essential figure of MC-UPQC in distribution systemshowed in figure 1.

According the figure, there are two feeders connected with two different substation supplies the load L1 and L2. Inthe MC-UPQC voltage ut2 and ut2 for both buses BUS1 and BUS2 [2]. The shunt connected MC-UPQC at load L_1 having current i_{l1}. Us1 and u_{s2} are the supply voltage and u_{l1} and u_{l2} are the load voltage, i_{s1} and

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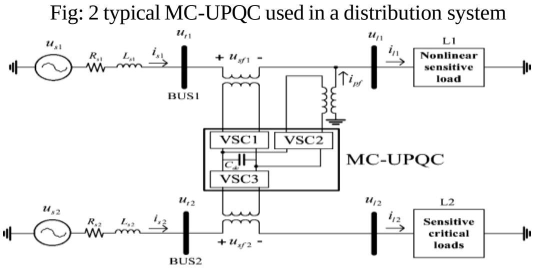
i_{s2} is feeder current and load current i_{l1} and i_{l2}. The bus voltage ul1 and u_{l2} may be subjected to as sag and swell [5]. For proper operation the nonlinear/sensitive load L_1 is needed to pure sinusoidal but its current in the form of sinusoidal with cantoning harmonic.

B. *Structure of MC-UPQC*

The internal structure of the typical MC–UPQC used in a distribution system is shown in Figure 2. It consists of three APFs (APF1, APF2, and APF3) which are connected back-to-back through a common DC link capacitor. In this configuration, APF1 is connected in series with BUS1 and APF2 is connected in parallel with load L1 at the end of Feeder1. APF3 is connected in series with BUS2 at the end of feeder2. Each of the three APFs in Figure 2 is realized by a three-phase converter with a commutation reactor and high-pass output filter which prevents the flow of switching harmonics into the supply.

Fig: 2 typical MC-UPQC used in a distribution system



The RC filter is connected between the converters and line for the prevention of losses during switching, the RC filter relates to commutating reactors as shown in figure 3. MC-UPQC is used to reduce load voltage and buses 1 and 2 and the multi converter is reduce the harmonics and to regulate the voltage level. Here single capacitor is connected as input to converter to maintain always constant dc link voltage.

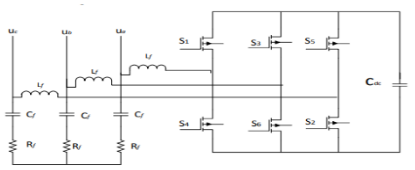


Fig:3 voltage source converter

III. CONTROL STRATEGY

According to figure 2 there are two series VSCs and one shunt VSCs present in MC-UPQC. The switching phenomena for series and shunt VSCs are taken for SPWM voltage and hysteresis control.

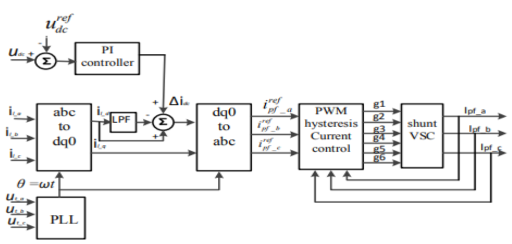


Fig: 4 control block diagram of shunt VSC

Shunt VSCs: function of shunt VSCs are as following

1) Shunt VSC is used to compensate to the reactive component of load L_1.
2) It compensates the harmonics of the load L_1.
3) The shunt VSC is used to regulate the voltage by the common dc link [6].

In the figure 4 the block diagram shows shunt VSC. The load current ($i_{l\text{-}abc}$) is transformed into synchronous dq0 is given by [1]

$$i_{l\_dq0}=T_{abc}{}^{\wedge dq0}\, i_{l\_ab}$$

$$T_{abc}^{dq0}=\frac{2}{3}\begin{bmatrix}\cos(\omega t) & \cos(\omega t-120^\circ) & \cos(\omega t+120^\circ)\\ -\sin(\omega t) & -\sin(\omega t-120^\circ) & -\sin(\omega t+120^\circ)\\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2}\end{bmatrix}$$

By this transform, the fundamental positive-sequence component, which is transformed into dc quantities in the *d* and *q* axes, can be easily extracted by low-pass filters (LPFs). Also, all harmonic components are transformed into ac quantities with a fundamental frequency shift.

The feeder current of d-q components are:

$i_{s\text{-}d} = i_{l\text{-}d}$

$i_{s\text{-}q} = 0$

This means that there are no harmonic and reactive components in the feeder current. Switching losses cause the dc-link capacitor voltage to decrease. Other disturbances, such as the sudden variation of load, can also affect the dc link. In order to regulate the dc-link capacitor voltage, a proportional–integral (PI) controller is used as shown in in Fig. 4. The input of the PI controller is the error between the actual capacitor voltage (u_{dc}) and its reference value (u^{ref}_{dc}). The output of PI controller is added to the d component of shunt VSC reference current to form a new reference current.

Series VSC: The function of the series VSC areas following

1) Voltage sag and swell is mitigated
2) Voltage distortion is compensated
3) Only in feeder 2 interruptions are compensated

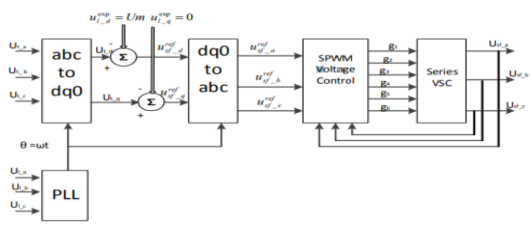


Fig: 5 block diagram of series VSC

$$u_{t\_dq0} = T_{abc}{}^{dq0}\, u_{t\_abc} = u_{t1p} + u_{t1n} + u_{t10} + u_{th}$$

According to control objectives of the MC-UPQC, the load voltage should be kept sinusoidal with a constant amplitude even if the bus voltage is disturbed. Therefore, the

expected load voltage in the synchronous d_{q0} reference frame ($u_{t\_dq0}^{exp}$) only has one value.
where the load voltage in the *abc* reference frame ($u_{t\_abc}^{exp}$) is

$$\begin{cases} u_{t1p} = [u_{t1p\_d} \quad u_{t1p\_q} \quad 0]^T \\ u_{t1n} = [u_{t1n\_d} \quad u_{t1n\_q} \quad 0]^T \\ u_{t10} = [0 \quad 0 \quad u_{00}]^T \\ u_{th} = [u_{th\_d} \quad u_{th\_q} \quad u_{th\_0}]^T \end{cases}$$

The compensating reference voltage in the synchronous d_{q0} reference frame is defined as

$$u_{l\_abc}^{\exp} = \begin{bmatrix} U_m \cos(\omega t) \\ U_m \cos(\omega t - 120°) \\ U_m \cos(\omega t + 120°) \end{bmatrix}$$

$$U_{sf\_dq0}^{ref} = u_{tdq0} - u_{t\_dq0}^{exp}$$

This means u_{t1p_d} in above should be maintained at U_m while all other unwanted components must be eliminated. The compensating reference voltage in above is then transformed back into the abc reference frame. By using an improved SPWM voltage control technique (sine PWM control with minor loop feedback) [8], the output compensation voltage of the series VSC can be obtained.

IV. SIMULATION RESULT

In this work, the proposed MC-UPQC and its control schemes have been tested through MATLAB. In this section, simulation results are presented, and the performance of proposed MC-UPQC system is shown. By using MATLAB/Simulink Software find and discussed some result which is find from MC-UPQC design. MC-UPQC working time is 0.2 to 0.5.

Now from simulation model, applying series (Series VSC1) and shunt VSC on line 1 then the Bus1 voltage and current waveform is shown in figure 6 and figure 7.

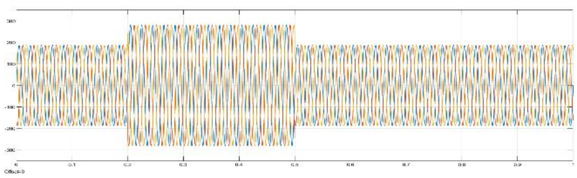


Fig 6: Bus 1 voltage (source side)

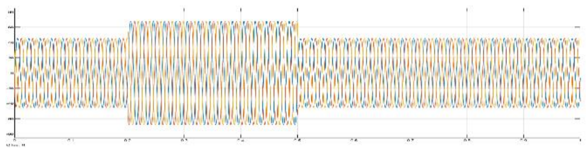


Fig 7: Bus 1 current (source side)

Here voltage having swell in between time interval of 0.2 to 0.5 and having a value of 0.5pu. After applying series and shunt VSC's on line 1 then Bus 2 (load side) voltage and current wave form is shown in figure 8 and figure 9.

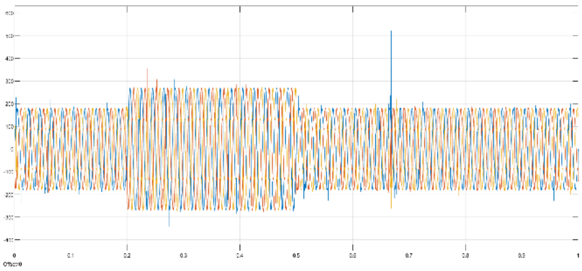


Fig 8: Bus 2 voltage (load side)

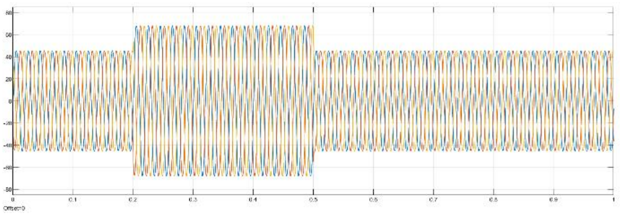


Fig 9: Bus 2 current (load side)

The above graphs show the voltage and current both are increasing.

In line 2, applying series Voltage Source Converter for the voltage sag of 0.7, graph of bus 3 (generation side) voltage and current are shown in figure 10 and figure 11.

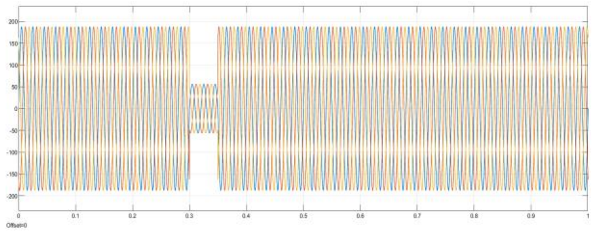


Fig 10: Bus 3 voltage (Source side)

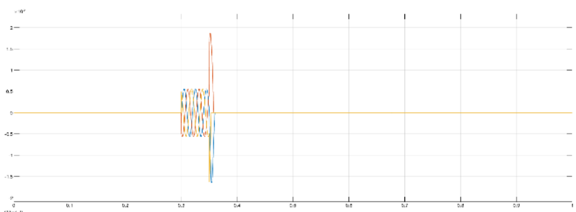


Fig 11: Bus 3 current (Source side)

Applying series VSC2 on line 2 current and voltage both are maintained but sag is applied in both waveform at fault time (0.3 to 0.35). The graph of voltage and current of Bus 6 (load side) shown in fig 12 and fig 13.

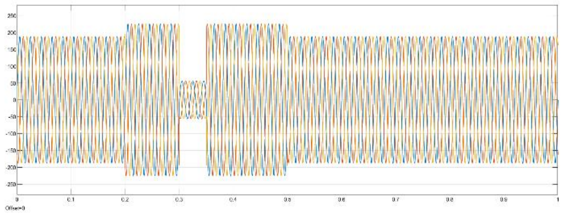


Fig 12: Bus 4 current (load side)

After running the simulation, the result shows the power quality issues are compensated and MC-UPQC is working properly at multi feeder system and the total harmonic distortion on this simulation model then found result is improved after applying MC-UPQC, the voltage THD is 0.02% and current is 22.39% at on load side of line 1 and in line 2 THD is improved up to 0.92% (voltage) and current is 1.14% (current).

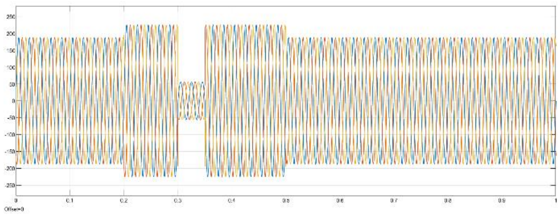


Fig 13: Bus 4 voltage (load side)

V. CONCLUSION

In conclusion, the use of a multi converter unified power quality conditioner (MCUPQC) is a promising approach for improving power quality in multi-feeder systems. MCUPQCs can effectively mitigate a wide range of power quality issues, including voltage sags, swells, and harmonics. Power quality problems because of nonlinear load is compensate and THD is also improve by this mythology. Overall, the proposed method will provide a flexible and effective solution for improving the power quality of the multi-feeder system, while also providing a number of other benefits such as improved system stability and reduced electrical losses.

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