International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 08 Issue: 11 | Dec - 2024 SJIF Rating: 8.448 ISSN: 2582-3930

Realization of an All-Digital Phase-Locked Loop

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Abstract - An all-digital phase locked loop (PLL) is presented in the paper. The goal of a PLL, a closed-loop control system, is to synchronize the phase and frequency of an incoming signal. Clock generation and recovery communication systems are the most flexible uses of PLL. Digital PLLs are chosen because of the greater integration of digital designs. The implementation of ADPLL utilizing a Xilinx Vivado tool and code is written in Verilog.

***Key Words*:** *All Digital PLL, digitally controlled oscillator(DCO),Low Pass Filter(LPF),Increment-Decrement (ID)*

1.INTRODUCTION

With the continuous advancement of components for digital applications, many signal-processing systems are transitioning from the analog to the digital domain. This shift is driven by the numerous advantages offered by the digital domain, including easier calibration, enhanced accuracy, improved predictability, and the ability to handle increased complexity without requiring intricate adjustments or frequent calibrations. These benefits make the digital domain a superior choice compared to its analog counterpart, fostering greater interest and innovation in this field of research and experimentation.

2. Design Overview

2.1 Structure of PLL

A phase-locked loop (PLL) can be implemented using either analog or digital circuitry, but both share the same fundamental structure. Regardless of the implementation type, PLL circuits consist of four key components :

- **Phase Detector**: Compares the phase of the input signal with the output signal and generates an error signal proportional to their phase difference.
- **Low-Pass Filter**: Processes the error signal from the phase detector, removing high-frequency noise and producing a smooth control signal.
- **Variable-Frequency Oscillator:** Adjusts its output frequency based on the control signal, ensuring synchronization with the input signal.
- **Feedback Path** : Feeds the oscillator output back to the phase detector for continuous comparison, often incorporating a frequency divider to adjust the feedback signal as needed.

This structure forms the basis of both analog and digital PLL systems, enabling them to perform a wide range of synchronization and signal-processing tasks

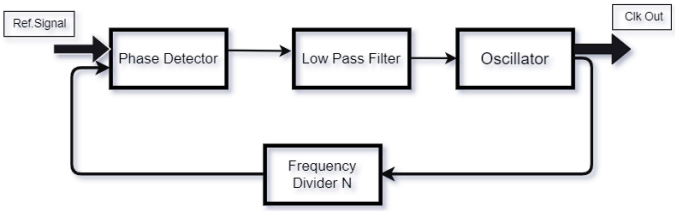

Fig -1: Block diagram of PLL

2.2 Implementation of ADPLL

The all-digital phase-locked loop (ADPLL) provides several advantages over other types due to its exclusive use of digital signals. An ADPLL consists of three main components :

- Digital Phase Detector
- Loop Filter
- Digitally Controlled Oscillator

The primary function of a PLL is to synchronize the phase and frequency of one signal with another. The phase detector detects the phase difference between the two signals The loop filter then filters out any out-of-band noise from the detected signal. Finally, the digitally controlled oscillator (DCO) takes the output from the loop filter and adjusts the phase and frequency of Signals to match.

In an ADPLL, all the functional blocks of the system must be realized using entirely digital circuits. The signals involved are digital (binary) and they can be either single signals or combinations of parallel digital signals. The key advantages of

this implementation include the absence of off-chip components and reduced sensitivity to variations in technology.

Digital Phase Detector (DPD)

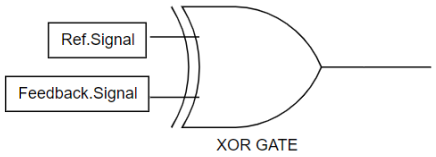

Fig -2: XOR based Phase Detector

A phase detector (PD) is used to measure the phase difference between the reference signal and the desired signal. Historically, the PD was the first component to be digitized and has been employed in digital PLLs. This concept can also be extended to all-digital PLLs (ADPLLs). The common implementations of a digital phase detector include:

- Exclusive-Or (XOR) Gate
- Digital Phase-Frequency Detector

For this paper, we focus on the XOR gate-based Digital Phase Detector (DPD). The XOR mechanism provides a simple and effective method for phase detection. In this setup, the reference signal and the feedback signal are fed into the inputs of the XOR gate. This type of detector inherently locks itself 90 degrees behind the phase of the input signal.

The design incorporates an XOR gate along with a 15-bit counter to calculate the phase error. The XOR gate output (Phase error) acts as the clear signal for the counter, while the reference signal is used as the reset (negative logic) for the counter. The feedback signal is derived from the Digital Controlled Oscillator (DCO).

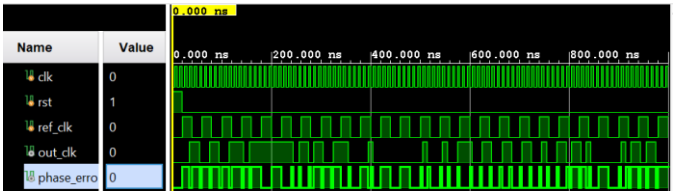

Fig -3: Phase error from Digital Phase Detector(DFD)

Loop Filter

The digital loop filter is not a mandatory component in all phase-locked loops. However, in higher-order loops used in applications like servo control and telecommunications, the loop filter is essential. Different types of phase detectors generate various signal formats, and the digital loop filter helps by removing the high-frequency components of the phase error signal. In a K-counter-based loop filter, two separate counters are used, whereas a single counter preceded by a pulse-forming circuit is employed in the UP/Down counter-based loop filter.
In this study, a K-counter-based loop filter is implemented, with its block diagram shown in Fig-3. The value of K is set to 16. Therefore, the down counter counts from 0 to 15 when the signal Phase error is high, while the up counter counts from 0 to 15 when Phase error is low. the most significant digit (MSD) is 1. Based on whether the up or down counter is active, the carry or borrow signals are generated accordingly

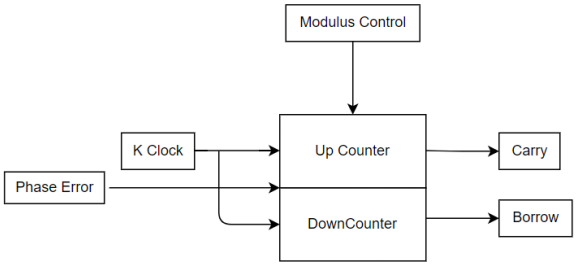

Fig -4: K Counter based Loop Filter

Digital Controlled Oscillator (DCO)

The Digital Controlled Oscillator (DCO) is the digital equivalent of the voltage-controlled oscillator (VCO). In a DCO, control signals are employed to adjust the frequency of the oscillator's output. This allows for precise frequency tuning in digital systems.
There are two primary types of DCOs commonly used:

- **Divide-by-N Counter Type** In this type of DCO, a counter is used to divide the input clock frequency by a fixed integer value (N). The output frequency is determined by the division factor, providing a frequency that is a fraction of the input clock.
- **Increment-Decrement Counter Type**This type of DCO adjusts its frequency by incrementing or decrementing the count value based on input control signals. The oscillator's output frequency is directly modified by the control signal, allowing for dynamic frequency adjustments in real-time.

Both types of DCOs play crucial roles in various applications, where fine control of frequency is necessary, such as in phase-locked loops (PLLs) and frequency synthesis.

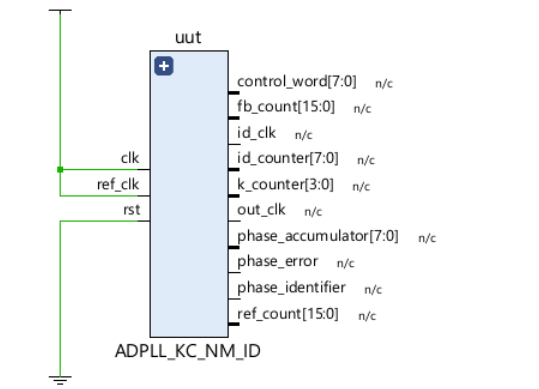

Fig -5: RTL Schemetic of ADPLL

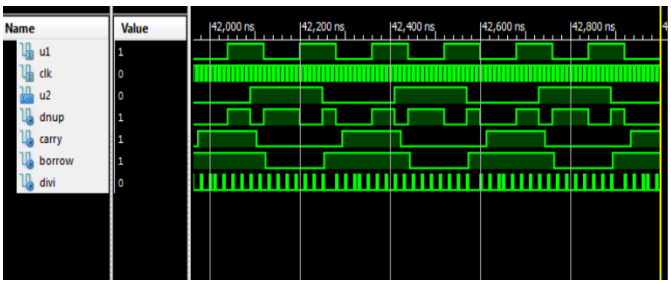

Fig -6: Simulation result

The locking process involves three key stages: frequency acquisition, phase alignment and steady-state tracking, all handled digitally to ensure precision and flexibility.

Initially, the ADPLL detects the frequency difference between the reference clock and the output of the DCO using a phase-frequency detector (PFD) or equivalent digital logic. The detector produces control signals, typically in the form of "up" and "down" commands, indicating whether the oscillator's frequency should increase or decrease. These signals are processed through a digital loop filter, which smooths out the commands to prevent abrupt changes. The loop filter's output serves as a control word for the DCO, adjusting its frequency in fine steps.

As the ADPLL operates, it narrows the frequency difference, transitioning from the frequency acquisition phase to the phase alignment phase. During this stage, the phase error, or the difference in timing between the edges of the reference clock and the DCO output, is minimized. The ADPLL uses a phase detector to measure this error and generates correction signals to align the two clocks. The process continues iteratively, with the loop filter ensuring that the corrections are stable and do not overshoot.

Once the frequency and phase are aligned, the ADPLL enters the steady-state tracking phase. In this state, the loop dynamically adjusts the DCO's frequency to compensate for any small variations in the reference clock or environmental factors such as temperature and supply voltage changes. The digital nature of the ADPLL allows it to maintain high resolution and stability, as the corrections are applied in discrete, predictable steps.

The key to the ADPLL's locking mechanism lies in its feedback loop, where the output is constantly compared with the reference. The system's digital design eliminates many of the noise and nonlinearity issues found in analog PLLs, making it ideal for modern applications requiring high precision, such as wireless communication, processors, and clock synchronization. Through iterative corrections, the ADPLL locks the phase and frequency, ensuring a stable and synchronized output clock.

3. CONCLUSIONS

This project successfully explored the implementation of an All-Digital Phase-Locked Loop (ADPLL) using Verilog. The project provided valuable insights into the design and functionality of ADPLLs, covering the fundamental concepts and offering hands-on experience with digital PLL design. While the implementation met its basic objectives, there are numerous opportunities for future enhancement. For instance, a full custom design could be developed to further optimize the performance and adaptability of the ADPLL. Additionally, the extra clock input could be eliminated by creating a clock-independent Digital Controlled Oscillator, improving the overall design efficiency.

The project laid a solid foundation for understanding digital PLLs, but further exploration into advanced concepts such as noise reduction techniques, multi-frequency operation, and adaptive control mechanisms could significantly enhance the ADPLL's capabilities. These improvements would make it suitable for a wider range of applications, including high-speed communication systems and advanced signal processing tasks. Overall, this project was a highly enriching learning experience, offering both theoretical knowledge and practical skills in digital design, while highlighting areas for continuous improvement and innovation in ADPLL technology.

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ACKNOWLEDGEMENT

We would like to express our deepest gratitude to Mrs. Shyamala S C, for their invaluable guidance, continuous support, and expert insights throughout this research on the design and implementation of a high-performance floating-point multiplier. Their encouragement and technical advice were instrumental in helping us navigate challenges and improve the quality of our work. We are also thankful to the faculty members and staff of P.E.S. Institute of technology and Management for providing the resources, facilities, and a conducive environment that facilitated the progress of this project. The support received from our institution played a significant role in refining the methodologies and ensuring accurate implementations using Xillinx Vivado.

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