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RESEARCH STUDY ON IMPROVE POWER QUALITY USING CASCADED MULTI-LEVEL INVERTER

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Abstract - The cascaded multilevel inverter (CMLI) has gained much attention in recent years due to its advantages in high voltage and high power with low harmonics applications. A standard cascaded multilevel inverter requires n DC sources for 2n+1 levels at the output, where n is the number of inverter stages. This paper presents a topology to control cascaded multilevel inverter that is implemented with multiple DC sources to get 2n+1 – 1 levels. With using Pulse Width Modulation (PWM) technique, the firing circuit can be implemented which greatly reduces the Total Harmonic Distortion (THD) and switching losses..

1.INTRODUCTION

In this paper, a digital logic control circuit is proposed for a solar-powered CMLI to achieve higher levels with a reduced number of switches without requiring bidirectional switches, filter components, detailed look-up tables, and output transformers. The techniques include "binary", "trinary" and "modified multilevel connections" (MMC) to achieve 15 levels and 27 levels respectively. In some literatures, voltage balancing, ultra-capacitors, PWM switching and transformers are required, which will cause increased cost and manufacturing problems, therefore not desirable for motor drive applications. In MMC, a level of 15 is achieved with the single-stage inverter by adding the input voltages using the built-in controller based on the proposed switching sequence. Comparison of three methods with existing techniques is analyzed and experimentally verifiedPower Multilevel inverter provides a suitable solution for medium and high power systems to synthesize an output voltage which allows a reduction of harmonic content in voltage and current waveforms. Multilevel refers to the multiple connections of individual inverters termed as ‘stages’ to provide the output voltage with required ‘levels’. Increasing the number of levels will result in the reduction of harmonic distortion. The three topologies such as flying capacitor (FC), neutral point clamped (NPC) and cascaded multilevel inverters (CMLIs) are preferred for various applications depending upon its structure and modulation algorithms. Among the three topologies, CMLI is highly preferred for the interconnection of renewable energy systems because of the advantages such as absence of voltage unbalance problem, possible elimination of DC–DC boost converter, adaptive at low switching Frequency and absence of clamping capacitors and diodes.

2. PROPOSED SYSTEM

The Proposed System investigates improvement of power quality for Cascaded MLI with reduced number of semiconductor switches. Binary mode uses only 12 switches to obtain the required 15-level output while that MMC mode uses only 10 switches to obtain same output as that in binary mode that is 15 level output. 27-level output is obtained with 12 switches in trinary mode in addition, power circuit being the same as that of the binary mode. Comparison has been made among the 3 modes by carrying a detailed simulation study in MATLAB for various levels. The method proposed provides with the multiple advantages such as less cost (in case of hardware), reduced THD, minimum computational complexity, simple design and absence of transformers, filter circuit, detailed look-up table and boost converters.

3. IMPLEMENTATION OF PROPOSED METHODOLOGY

Solar photovoltaic (PV) fed CMLI is dealt in various literatures, but it intends for low voltage and low level configurations. Pulse width modulation (PWM) technique for a 5-level CMLI .In this paper, a twenty five-level Cascade H-bridge inverter based T-STATCOM configuration has been presented. The adoption of Cascade H-bridge inverter for T-STATCOM applications causes to decrease the device voltage and the output harmonics by increasing the number of output voltage levels. This paper presents a T-STATCOM with a PIC controller based twenty five-level CHB multilevel inverter for the voltage sag, voltage swell and reactive power mitigation of the nonlinear load[1]

Solar photovoltaic (PV) fed CMLI is dealt in various literatures, but it intends for low voltage and low level configurations. Pulse-width modulation (PWM) technique for a5-level CMLI and 7-level CMLI for PV system is addressed which requires boost converter, auxiliary circuitry and multiple reference signals for pulse generation. A 5-level current CMLI for a single phase grid connected PV system given in requires there design of LC filter to reduce the inductive and resistive losses for higher power levels [2]

A 5-level current Cascaded MLI for grid connected PV system which fed by single phase is addressed. But the redesigning of LC filter is needed for this which further reduces the resistive and inductive losses forgetting higher power levels. [6]

Modified multilevel connections (MMCs) to achieve 15 levels and 27 levels, respectively. The three stage CMLI power circuit used to achieve 15 levels by binarymode using digital switching technique comprises of counters and logic functions. The same power circuit is used to achieve 27 levels by trinary mode using embedded controller. In certain literature, voltage balancing, ultra capacitors, PWM switching and transformers are required which will be the cause for the increase in cost and manufacturing problems thereby not desirable for motor drive applications In conventional approach, PWM techniques are used by the comparison of reference and carrier signals to provide the required gating signals for the inverter switches. The number of output voltage levels obtained from this approach is given in the following equationm = $2N_s$+ 1 Where m denotes the output voltage levels and Ns is theindividual inverter stages. The number of switches (l) required to achieve m levels is given in the following equation.

$$l = 2(m - 1)\ 2$$

For the implementation of 15-level CMLI, the number of switches required is 28 with seven individual inverterstages. In addition to the 28 switches, 182 clamping diodes in case of NPC or diode clamped multilevel inverter and 91balancing capacitors in case of FC type multilevel inverter along with 14 DC bus capacitors are needed to achieve 15-level output. The proposed paper deals with the following topologies for the reduction of switches. Increasing the number of levels will subsequently reduce the harmonic distortion which in turn improves the power quality.

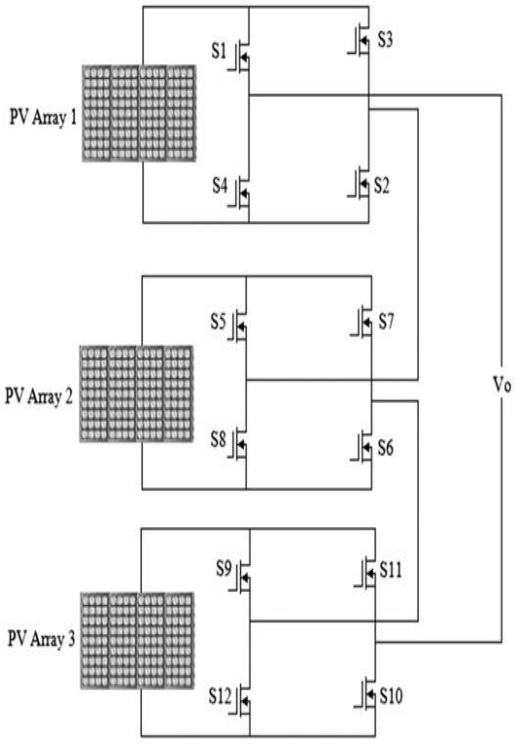
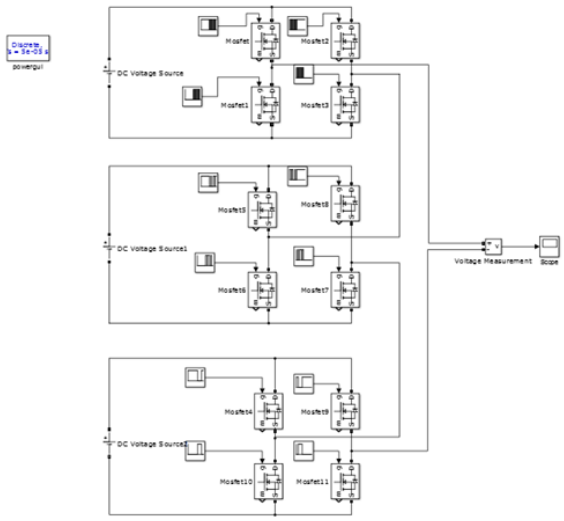


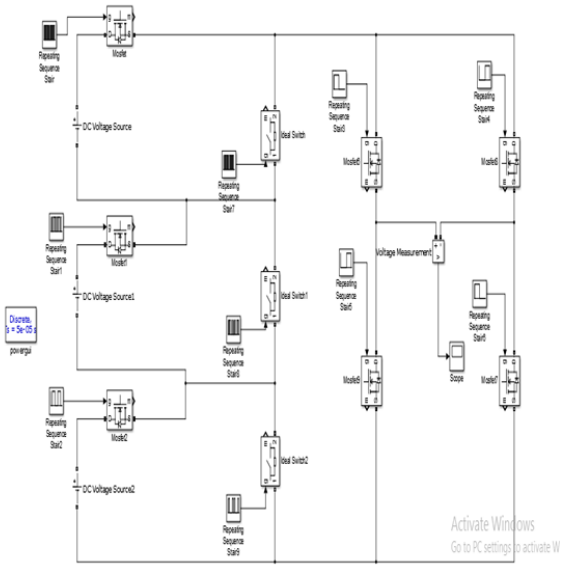
Figure 1Three Stage Inverter Power Circuit

4. RESULTS

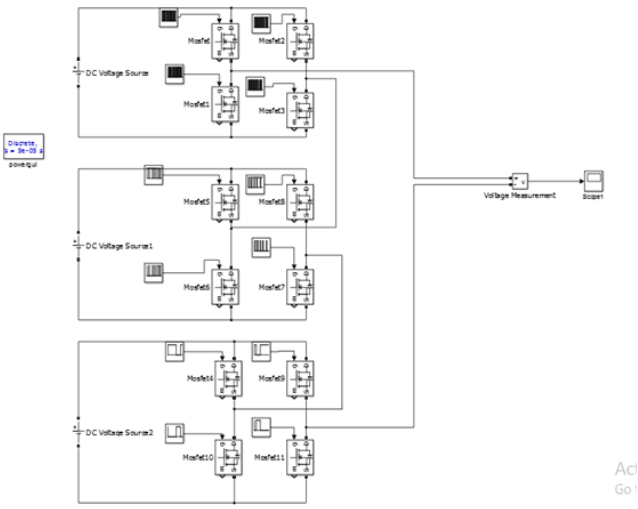
1. Simulink model of Cascaded MLI In binary mode



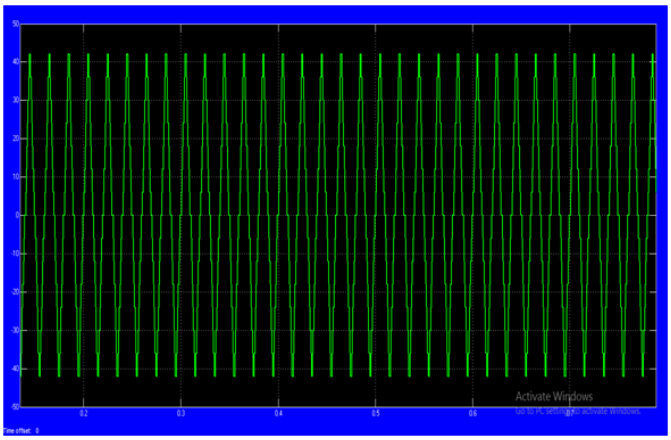
2. Simulink model of Cascaded MLI in MMC mode.



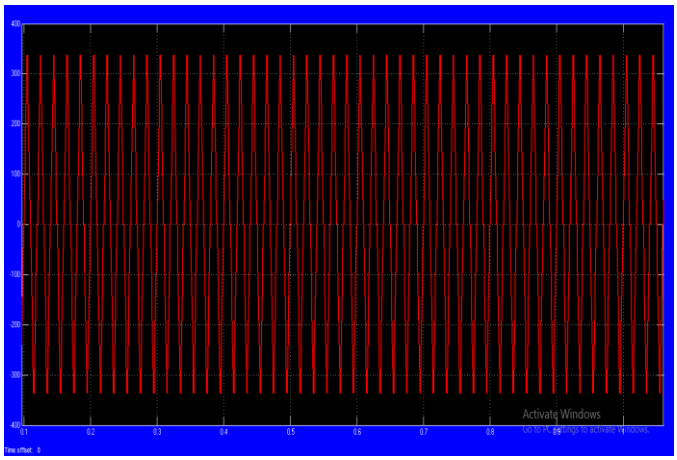
3. Simulink model of Cascaded MLI in trinary mode



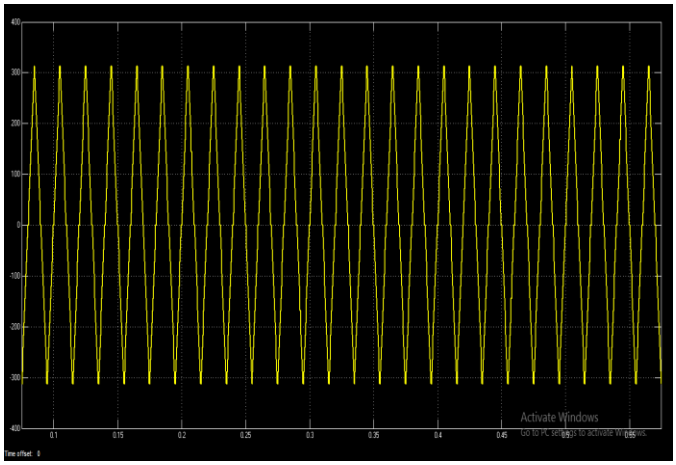
4. **Binary mode MLI output voltage.**



2. **MMC mode MLI output voltage.**



3. **Trinary mode MLI output voltage.**



CONCLUSION:

With Improving the power quality of the solar-fed CMLI while reducing the number of semiconductor switchgear was investigated in this project. The required 15-level output is achieved using only 12 keys in binary mode and 7 keys in MMC mode. In addition, 27-level output with 12 keys is obtained through the triple mode. A mathematical model of solar PV is implemented which serves as the input to the phases of the inverter. A detailed simulation study was conducted for different levels and a comparison was made. A CMLI of 3 kWps was implemented for all forms of harmonics and harmonics.

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