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Review Paper

Design and Development of UART Protocol Using Verilog with UVM Testbench

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Abstract: Verification of a complex VLSI design is a tedious process. Verification of Integrated Circuits using System Verilog lacks the reusability of the test bench of the environment UVM provides control over simulation behaviour in a ordered systematic way and will be executed sequentially to avoid race condition. System Verilog is a language same alike Verilog with its own constructs. UVM is a framework of System Verilog classes from where test benches will be built. This paper presents the Design of UART using Verilog and verifying using UVM. The verification done in this paper provides the complete working of UART which can be tested using UART device The verification done using UVM will reduce the overall time consumption done by the logic gates. Since the tests of sequences are kept apart from the original test bench hierarchy and the reusability of stimulus will reduce the overall execution time.

Keywords: Transmitter, Receiver, Baud rate, Synchronous Communication, Asynchronous Communication, FSM.

1. Introduction

The problem addressed in this project is the need for a robust UART (Universal Asynchronous Receiver-Transmitter) protocol implementation in VLSI (Very Large Scale Integration) designs. UART is a fundamental communication protocol widely used in digital systems to facilitate asynchronous serial data transmission. The task is to design, create, and test a Verilog UART protocol, making sure it complies with industry standards, achieves data transmission reliability, and satisfies requirements for baud rates, data formats, and other factors. By creating a UART protocol in Verilog and validating it using a UVM (Universal Verification Methodology) testbench, the project provides a complete solution. The solution involves carefully incorporating the functionality of the protocol in the design of the UART transmitter and receiver modules. A methodical and scalable verification environment comprising sequences, drivers, monitors, and scoreboards is offered by the UVM testbench. This project confirms, via a series of thorough simulations, that the UART protocol adheres to industry standards and the set parameters, guaranteeing a dependable and effective method of asynchronous serial communication in VLSI systems.

2. Literature Survey

B. Priyanka, M. Gokul et al (2021) [1] The design of a Universal Asynchronous Receiver and Transmitter (UART) using Verilog and its verification through Universal Verification Methodology (UVM) is the main topic of the presentation given at the 7th International Conference on Advanced Computing & Communication Systems.(ICACCS). The authors discuss the complexities of verifying integrated circuits in VLSI designs and emphasize the importance of efficient verification methodologies, using UVM to enable systematic and ordered simulation control to prevent race conditions. The UART design, a crucial component for asynchronous data transmission between devices, is explained along with the intricate verification process using UVM. By employing UVM, the paper highlights the reduction in time consumption for logic gates and the enhanced reusability of test sequences and stimulus, resulting in comprehensive testing of the UART device.

The research delves into the details of UART functionality, including its structure, transmission process, frame formats, and various modes of communication. It explores the working principles of UVM, elaborating on its key components like sequences, sequencers, monitors, drivers, agents, and environments, which aid in creating a systematic and reusable verification environment. The verification process involves generating test sequences, tracking successful data transmission, and validating functionality. The paper concludes by showcasing successful data matching in the simulation, providing detailed insights into the verification process and indicating the feasibility of incorporating the proposed verification environment as an IP in System-on-Chip (SoC) architecture for functional verification. The paper's references also indicate an extensive study in this domain, further supporting the significance of their work in the context of previous research in UART design and verification methodologies.

S. Harutyunyan, et al., (2020) [2] The paper presented at the 2020 IEEE 40th International Conference on Electronics and Nanotechnology details the development of a Configurable Verification Intellectual Property (VIP) for Universal Asynchronous Receiver-Transmitter (UART) interfaces. System Verilog is employed to create a verification architecture that emphasizes flexible, reusable test environments using Object-Oriented Programming (OOP) concepts. The VIP encompasses various components such as generators, drivers, monitors, and scoreboards to simulate UART functionality accurately. The test environment, including the application and scoreboard, facilitates comprehensive verification by testing loopback mode, directed test cases, error injection scenarios, and random test cases for diverse UART configurations. Functional coverage and simulation results indicate achieving 100% coverage through an assortment of meticulously designed test scenarios, validating the effectiveness of the verification environment in ensuring thorough testing of UART functionality.

C. Elakkiya, N. S. Murt et (2017) [3] The paper presents a comprehensive UVM-based verification approach for JTAG functionality, aiming to ensure proper functionality before the fabrication stage, emphasizing the significance of functional verification in IC design. The Universal Verification Methodology (UVM) is highlighted as a pivotal framework in this pursuit, aiming to improve testbench reusability and efficiency. The paper delineates a systematic testbench architecture for JTAG using UVM components such as Sequences, Tests, Drivers, Monitors, Agents, Scoreboards, and Environments. Through the implementation of various test cases, the verification ensures coverage of critical functionalities like Bypass, IDCODE, Sample/Preload, Extest, MBIST, random instruction selection, reset scenarios, and assertion checks. The verification process includes code and functional coverage analyses using Questa sim, reporting a 94.06% code coverage, 100% functional coverage, and 96.45% cross-coverage. This robust UVM-based approach showcases the effectiveness of reusable test environments, constrained random testing, and coverage-driven verification, illustrating its superiority over traditional Verilog-based verification methodologies in ensuring quality and functional correctness in the VLSI industry.

W. Ni (2015)[4] The study describes the creation of strong UVM-based verification platform for evaluating the performance of UART IP cores in System on Chip (SoC) architectures. To accomplish a thorough coverage of the UART protocols, the platform makes use of a functional coverage model that makes use of UVM's restricted random testing. The configuration combines multiple elements such as Test Suites, Bus-Monitor, and XCVR to create an adaptable environment for UART-based device verification. Using drivers, sequencers, and monitors to manage transactions and protocol checks, the XCVR module mimics DTE or DCE behavior. The Bus-Monitor component makes assertions, tracks protocol conformance, watches and analyzes data, and has a checker, sequencer, and monitor. To test for a variety of circumstances, random, fundamental, and error tests are used. The solution uses both limited and unconstrained random tests to expose and address uncovered areas, utilizing a systematic approach to coverage convergence. This approach, in conjunction with directed tests, addresses synchronization issues during test case creation and guarantees an exhaustive verification procedure. Overall, the results show that 100% functional coverage was attained, demonstrating the platform's efficacy in validating UART IP cores and possibly expanding its use to include a wider range of SoC designs.To meet the growing complexity of integrated circuits, the study presents a UVM-based verification platform especially made for validating UART IP cores in SoC designs. The platform accomplishes comprehensive coverage of UART protocols by utilizing UVM's restricted random testing methodology in conjunction with a functional coverage model. The foundation of the verification environment is made up of essential elements including XCVR, Bus-Monitor, and Test Suites, which enable protocol checks, transaction processing, emulation of DTE or DCE behaviors, and extensive testing scenarios. Through the use of a systematic convergence technique, the verification process first uses unconstrained random tests to find coverage gaps, and then it uses restricted random and guided tests to close these gaps. Ensuring comprehensive verification, the architecture of the platform has techniques to address sequence synchronization issues during test case development.In the conclusion, the platform accomplishes an impressive 100% functional coverage, proving its effectiveness in confirming UART IP cores and showing promise for wider uses in various SoC architectures.

L. M. Kappaganthu et al.,[5]The paper "I2C Protocol and its Clock Stretching Verification using System Verilog and UVM" discusses the significance and implementation of the I2C protocol for inter-integrated circuit communication, emphasizing the advantages over other protocols due to its reduced wiring complexity, support for multiple devices, and various speed modes. The paper outlines the basic functionality of the master and slave within the I2C protocol, addressing clock stretching, ultra-fast mode, and extension modes such as 7-bit and 10-bit addressing formats.. It also describes the verification process, which tests the protocol's design between a slave and his master using System Verilog with UVM in SimVision. The work includes examples of acknowledgment, data writing, and clock extending scenarios. Using a range of pertinent articles and studies, the list of references emphasizes the importance of the I2C protocol and its verification in modern electronics and communication systems. "I2C Protocol and its Clock Stretching Verification using System Verilog and UVM" is a research that examines the aspects of the protocol and emphasizes how it can help with communication between different devices and simplify wiring. It goes into great detail about addressing formats, clock stretching, and ultra-fast mode for both the slave and master components.The architecture of the master and slave I2C protocols is carefully examined using UVM and System Verilog in the Sim Vision tool, as part of a detailed description of the verification process. The paper provides real-world examples of data writing, acknowledgment signaling, and clock stretching scenarios, as well as references to a wide range of studies and works that demonstrate the significance of protocols in modern electronics and communication systems.

N. B. Harshitha, Y. G. Praveen Kumar(2021)[6] The paper provides a comprehensive review of the Universal Verification Methodology (UVM) in the digital design of Integrated Circuits (ICs), with a focus on the challenges faced in System on Chip (SoC) verification. It is It discusses numerous case studies and literature reviews as it explores the importance of UVM in lowering verification complexity, saving time, and improving reusability. By providing insights into its application in validating protocols like DDR2 memory, 40Gbps high-speed serial interfaces, vision-based hardware accelerators, and Controller Area Network (CAN) IPs, the work highlights UVM's importance in functional verification. It also examines the link between UVM and System Verilog, pointing out the benefits and drawbacks of UVM. The article discusses many UVM applications on various IC protocols, showcasing its usefulness and reusability in digital verification procedures.

Girdhar, D., & Shukla, N. K (2014)[7]The "Design and Verification of AMBA APB Protocol" document uses Verilog HDL and the Universal Verification Methodology (UVM) to give a thorough study and implementation of the APB (Advanced Peripheral Bus) and AMBA

(Advanced Microcontroller Bus Architecture) protocols. It describes the read and write cycles, simulation results, architecture, operating states, and the APB design verification procedure. The APB protocol is thoroughly examined in this study, with particular attention paid to its block diagram, operational states, signal interactions, simulation outcomes, and verification using UVM. This illustrates the accuracy and smooth operation of the system. The verification process is a crucial step in ensuring the RTL design's accuracy.The outcomes of UVM verification and simulation confirm that the design works as intended and that the data that is read and written from memory locations match. The study's conclusion emphasizes the possible use of SystemC in the construction of an Electronic System Level (ESL) model and its subsequent verification. This thorough investigation makes a substantial contribution to our understanding of the AMBA APB protocol and how it is used in SoC design.

Yammanuru, P. et al,.(2021)[8]The paper "Design and Verification of Advanced Peripheral Bus Protocol Using UVM" explores the integration of the Advanced Peripheral Bus (APB) within the Universal Verification Methodology (UVM) framework using Verilog HDL. It delineates the features and functionality of the APB as part of the Advanced Microcontroller Bus Architecture (AMBA), focusing on low power, simple interfaces, and communication between master and slave devices. The study covers the APB's operational states, read and write access protocols, and discusses its advantages such as low complexity signals and power consumption, along with its limitations, notably the lack of support for burst transfers and multiple transfers.

The paper underscores the verification process, testing functionality by comparing the Design Under Test (DUT) output with the reference model output. It references various sources and previous works in the field of AMBA protocols and UVM, highlighting the importance of standardized on-chip communication for high-performance System on Chip (SoC).

Kulkarni, A. et al,.(2020, December)[9]The article underscores the importance of this UVM-based approach in verifying and validating the full-duplex data transfer between master and slave cores for different character lengths and data formats. The validation simulations occur on both the positive and negative edges of the clock cycle for every transaction, ensuring the functionality and integrity of the SPI communication in various scenarios. The authors suggest that this proposed verification environment can be adapted as a verification Intellectual Property (IP) for SOC architectures to carry out comprehensive functional verification. The research leverages Mentor Questa and EP Wave tools in the EDA playground cloud environment for their simulations and assessments. Additionally, the paper references other related works and studies focusing on IP design, verification methodologies, and specific protocol implementations using UVM and System Verilog approaches.

This research significantly contributes to the realm of integrated circuit design, particularly in the verification process, by showcasing a robust methodology using UVM for ensuring the accuracy and reliability of SPI protocol implementations.

Kumar, K. A.et al,.(2015)[10]The paper authored by Kumar and Krishna in 2015 presents the design and functional verification of an SPI (Serial Peripheral Interface) Master Slave Core using Universal Verification Methodology (UVM). The study details the development process of the SPI core and focuses on its verification utilizing UVM, a standardized methodology for verifying integrated circuits. Through comprehensive descriptions, the paper discusses the various stages of design, the implementation of the SPI master-slave architecture, and the thorough verification process conducted using UVM. This research contributes to the advancement of reliable and efficient SPI communication systems by demonstrating a systematic approach to design and verify such cores, crucial in ensuring their accuracy and performance in real-world applications.

Sharath, S. G. (2022) et al ,.(2022)[11]The paper titled "UVM based Verification of Watchdog Timer with APB" published in the Journal of Algebraic Statistics Volume 13, No. 3, 2022, delves into the challenges of verifying complex VLSI designs, emphasizing the significance of effective verification methodologies due to the time-consuming nature of this process. The focus of the paper lies in the development and verification of a Watchdog Timer integrated with an APB interface, employing System Verilog and UVM methodologies. It highlights the importance of reusability in verification components, particularly in designs utilizing APB interfaces, and explores the advantages of UVM in creating a standardized testbench environment. The paper outlines the significance of the Watchdog Timer, its functionality, and application in detecting and resetting system faults. Through the use of UVM, the methodology aims to streamline the verification process by generating random stimulus and ensuring comprehensive test coverage, enabling the designed components to be reusable in similar designs with APB interfaces. The research significantly contributes to enhancing the efficiency and reliability of verification processes in VLSI designs.

P. Jain et al,.(2021)[12]The paper discusses the design and verification of the Advanced Peripheral Bus (APB), a key component of the Advanced Microcontroller Bus Architecture (AMBA) family, aimed at improving interface simplicity, reducing power consumption, and lowering interface complexity in connecting low-bandwidth peripherals to System on Chip (SoC). Utilizing Verilog for design and Verilog Testbench for verification, the study meticulously describes the functionality of the protocol, addressing read and write operations, standby states, and error responses.

Workflow	System Verilog Methodology	Verilog Methodology
Requirements Gathering	Collaborate with stakeholders to define operational requirements.	Collaborate with stakeholders to define operational requirements.
Architecture Design	Design the UART module architecture, considering components like transmitter, receiver, and control logic.	Same as System Verilog.
Module Implementation	Implement the UART modules using System Verilog constructs, such as classes and interfaces.	Implement the UART modules in Verilog, focusing on procedural blocks and traditional structural modeling.
Simulation and Verification	Develop a UVM testbench using System Verilog for stimulus generation, coverage analysis, and assertions.	Develop a Verilog testbench using procedural constructs for stimulus generation and assertions.
Functional Verification	Utilize UVM components such as sequences, drivers, and monitors to verify UART functionality.	Write Verilog test cases targeting specific UART functionalities and simulate using a Verilog simulator.
Timing Analysis and Optimization	Perform timing analysis using System Verilog constructs for timing checks and optimizations.	Analyze timing using traditional Verilog timing constructs and optimize the design accordingly.
Integration and System Testing	Integrate the UART module with other system components using System Verilog interfaces and verify system-level interactions.	Integrate the Verilog UART module into the larger system environment and conduct system-level testing.
Documentation	Document design specifications, test plans, and verification results using System Verilog constructs.	Document using comments within the Verilog codebase, focusing on clarity and maintenance.
Validation	Validate against requirements using System Verilog assertions and coverage metrics.	Validate using Verilog test cases and ensure compliance with specified requirements.
Deployment	Deploy the System Verilog implementation of UART protocol into the target system environment.	Deploy the Verilog implementation of UART protocol into the target system environment.

3.Conclusion

The comprehensive analysis of multiple research papers focused on the Universal Verification Methodology (UVM) application in verifying diverse Integrated Circuit (IC) protocols, such as UART, I2C, SPI, and APB, presents a substantial advancement in the field of VLSI design. These papers collectively underscore the pivotal role of UVM in tackling the complexities of functional verification, emphasizing the methodology's ability to improve testbench reusability, reduce verification time, and ensure comprehensive coverage. The studies explore the intricacies of various IC protocols, detailing their functionalities, design aspects, operational modes, and verification strategies while consistently highlighting the significance of UVM in achieving 100% functional coverage and demonstrating its effectiveness in ensuring the accuracy and reliability of IC designs. The papers also emphasize the significance of UVM in enabling systematic and standardized verification environments, showcasing its potential for adoption as intellectual property (IP) in System-on-Chip (SoC) architectures. Overall, these collective works contribute significantly to advancing the understanding and implementation of robust verification methodologies using UVM in the domain of IC design, laying a strong foundation for future developments and improvements in ensuring the functional correctness of complex VLSI designs.

4.References

[1] B. Priyanka, M. Gokul., A. Nigitha. and J. T.Poomica., "Design of UART Using Verilog And Verifying Using UVM," 2021 7th International Conference on Advanced Computing and Communication Systems (ICACCS), Coimbatore, India, 2021, pp. 1270-1273,doi: 10.1109/ICACCS51430.2021.9441789.

[2] S. Harutyunyan, T. Kaplanyan, A. Kirakosyan and H. Khachatryan, "Configurable Verification IP for UART," 2020 IEEE 40th International Conference on Electronics and Nanotechnology (ELNANO), Kyiv, Ukraine, 2020, pp. 234-237, doi: 10.1109/ELNANO50318.2020.9088878.

[3] C. Elakkiya, N. S. Murty, C. Babu and G. Jalan, "Functional Coverage - Driven UVM Based JTAG Verification," 2017 IEEE International Conference on Computational Intelligence and Computing Research (ICCIC), Coimbatore, India, 2017, pp. 1-7, doi: 10.1109/ICCIC.2017.8524556.

[4] W. Ni and X. Wang, "Functional coverage-driven UVM-based UART IP verification," 2015 IEEE 11th International Conference on ASIC (ASICON), Chengdu, China, 2015, pp. 1-4, doi: 10.1109/ASICON.2015.7517188.

[5] L. M. Kappaganthu, M. D. Prakash and A. Yadlapati, "I2C protocol and its clock stretching verification using system verilog and UVM," 2017 International Conference on Inventive Communication and Computational Technologies (ICICCT), Coimbatore, India, 2017, pp. 478-480, doi: 10.1109/ICICCT.2017.7975245.

[6] N. B. Harshitha, Y. G. Praveen Kumar and M. Z. Kurian, "An Introduction to Universal Verification Methodology for the digital design of Integrated circuits (IC's): A Review," 2021 International Conference on Artificial Intelligence and Smart Systems (ICAIS), Coimbatore, India, 2021, pp. 1710-1713, doi: 10.1109/ICAIS50930.2021.9396034.

[7] Girdhar, D., & Shukla, N. K. (2014). Design and verification of amba apb protocol. International Journal of Computer Applications, 95(21).

[8] Yammanuru, P., & Reddy, M. A. (2021). Design And Verification Of Advanced Peripheral Bus Protocol Using Uvm. Journal of Artificial Intelligence, Machine Learning and Neural Network (JAIMLNN) ISSN: 2799-1172, 1(02), 1-9.

[9] Kulkarni, A., & Sakthivel, S. M. (2020, December). UVM methodology based functional Verification of SPI Protocol. In Journal of Physics: Conference Series (Vol. 1716, No. 1, p. 012035). IOP Publishing.

[10] Kumar, K. A., & Krishna, M. S. (2015). Design and Functional Verification of A SPI Master Slave Core using UVM. International Journal of Scientific Engineering and Technology Research (IJSETR), 4(51), 11023-11030.

[11] Sharath, S. G. (2022). UVM based Verification of Watchdog Timer with APB. Journal of Algebraic Statistics, 13(3), 5343-5350.

[12] P. Jain and S. Rao, "Design and Verification of Advanced Microcontroller Bus Architecture-Advanced Peripheral Bus (AMBA-APB) Protocol," 2021 Third International Conference on Intelligent Communication Technologies and Virtual Mobile Networks (ICICV), Tirunelveli, India, 2021, pp. 462-467, doi: 10.1109/ICICV50876.2021.9388549.