Review Paper on FPGA Based VGA Signal Generation

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Abstract: As a standard display interface, VGA(Video Graphics Array)has been widely used. This paper presents the design and implementation of VGA controller. Hardware architecture is implemented on a ALTERA CYCLONE-ii EP2C5T144C8FPGA（Field Programmable Gate Array）chip. The paper has given its top layer module design and the timing function simulation. Detailed information is focused on the system architecture, hardware design and software programming. This controller is developed using only VHDL (hardware description language) based in the IEEE standards, to ensure the portability with any manufacturer. The system can display various color strip, Chinese characters and image. The results show that this proposed algorithm gives good performance with short processing time, low resource utilization, small power consumption and memory usage. Because the data can be sent directly to monitors, the design can speed up data processing, improve system reliability in real time and save hardware resource.

Keywords : Field Programmable Gate Array (FPGA's), VGA Controller, Verilog HardwareDescription Language (VHDL).

This 25MHz internal clock is then used to generate V-Sync and H-Sync synchronisation signals as per standard resolution timing (i.e., Sync pulse width, visible region, front & back porch). As shown in circuit diagram this synchronisation signals are generated at Pins 114 & 115 of FPGA. As FPGA can processes various signals through various logic blocks concurrently so it is able to generate V-Sync and H-Sync signals concurrently which are synchronized with each other as they are sharing same internal clock signal of 25MHz.

For RGB Analog colour signal generation a DAC (Digital to Analog Converter) is required which is not present on-board or in FPGA chip. In order to generate these RGB Analog colour signals from FPGA a R2R-Ladder based DACs are used. As shown in circuit diagram combination of 1K and 1.8K resistors are used to form 6-Bit R2R-Ladder circuit for every colour channel (i.e., Red, Green, and Blue). This three 6-Bit R2R-Ladders can generate 262K colours. These R2R-Ladders are connected to 18 Pins of FPGA as shown in circuit diagram. The output from R2R-Ladder (i.e., VGA_R, VGA_G, VGA_B) is then feed into VGA monitor along with H-Sync and V-Sync signals.

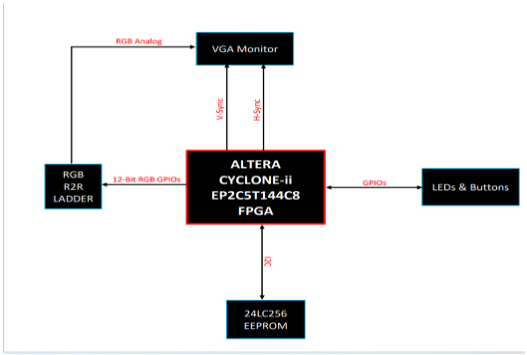
Introduction :

FPGA based VGA signal timing pattern generation is a hardware VGA driver based on Field Programmable Gate Array (FPGA). This driver circuit is implemented on Altera's Cyclone-ii FPGA (EP2C5T144C8) which consist of 4608 Logic Elements (Logic Blocks based on Logic Gates), 119808 RAM bits, 2x PLLs, and 158 IOs. Out of 158 IOs only few of them are used to interface VGA monitor, EEPROM, and LEDs, buttons. The FPGA calculates timing based of resolution and FPS (Frames/Seconds) of monitor and generates precise timing VGA signals such as Vertical Sync (V-Sync), Horizontal Sync (H-Sync), and R2R Ladder RGB analogue signals.

For image or text data storage, a 24LC256 EEPROM is used which can store up-to 32KB of data. This EEPROM can be used to store small images of resolution QQVGA (160x120), or QCIF (176x144). For text data storage it only needs 1-byte per character for UTF-8 Unicode. This EEPROM is interfaced to FPGA via two of its IOs. These two signal pins are called as SCL (Serial Clock) & SDA (Serial Data) which is also known as Inter-Integrated Circuit (I2C) or Tow-Wire Interface (TWI) synchronous serial communication. The data/bin into EEPROM is already flashed/uploaded with the help of other microcontroller/ FPGA/CPLD or hardware programmer.

A part from VGA monitor, for simple user interaction few LEDs and buttons are used. The LEDs are used for various indication such as hardware is running,

With the help of internal VGA synchronised counters and 18-bit colour channel the driver can generate various test patterns, images, text, and various graphics. The complete VGA driver implementation is based on VHDL (Very High-Speed Integrated Circuit – Hardware Description Language). For VHDL, RTL, synthesis, debugging, and programming a Qurtus-II software IDE is used.



2.1 VGA CONTROLLER

VGA (video graphics array) is a video display standard. It provides a simple method to connect a system with a monitor for showing information or images. As a standard display interface, VGA has been widely used. There is more and more need in displaying the result of the process in real time as the fast development of embedded system, especially the development of high speed image processing . Apart from that, display will be replacing paper for future. Words of wisdom; seeing is believing and picture telling thousand words, display can give correct information about something. Display is used when people present something. Pictures or texts at display catch more attention than verbal

data transfer is in progress, etc. The buttons are used to control various parameters of VGA such as brightness, colour shift, system ON/OFF, change data, etc. This LEDs and buttons use few of the IOs of FPGA.

For FPGA pin planning, configurations, synthesis, analysis, and hardware description a Quartus-II 13.0 Web Edition software tool is used. For complete hardware description a VHDL (Very High-Speed Integrated Circuit Hardware Description Language) is used. It also uses one of the internal PLL (Phase Lock Loop) to increase the clock from 50MHz (on-board osc. chip) up-to 400MHz (internal signals).

Objective

1) Objective of this project is to build a FPGA based VGA monitor driver in order to study the working principle, behaviour, and timing pattern of VGA signals.

2) In order to store data such as small size image data, text, etc. a 32KB EEPROM 24LC256 is interfaced to FPGA which reads information from this EEPROM and convert it into VGA signal which then drives the monitor and shows the data in form of image or text.

Methodology :

FPGA based VGA signal generator is a hardware VGA driver based on Field Programmable Gate Array (FPGA). This driver is implemented on Altera's Cyclone-ii FPGA (EP2C5T144C8). As shown in circuit diagram, out of 152 I/Os only 20 I/Os are used to generate 18-bit RGB VGA signal. This driver generates a VGA signal of industrial standard voice??

when people are doing presentation. When people do that kind of presentation, there must be some device involved in control the display.

A part from VGA monitor, for simple user interaction few LEDs and buttons are used The LEDs are used for various indication such as hardware is running, data

transfer is in progress, etc. The buttons are used to control various parameters of VGA

such as brightness, colour shift, system ON/OFF, change data, etc. This LEDs and buttons use few of the IOs of FPGA.

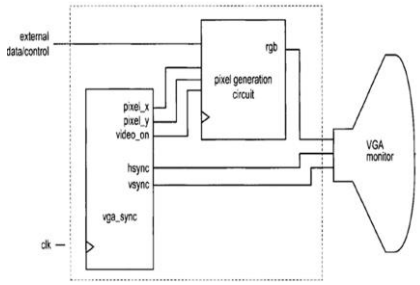


Fig.2 **INTERFACING VGA DISPLAY WITH FPGA**

Literature survey

[1] *" Design and Implementation of VGA controller on FPGA"* – **Radi H.R, M.N Shaha**- Oct 2012

[2*] " Design of VGA monitor controller using Altera FPGA base system*" -**M. Bharti, A.Yognath** – Mar 2014

[3] *" Image acquisition and VGA display system based on FPGA"* – **Zhu, Yi – Dan and Yi-Bing Fang**- 2011

resolution of 640x480 at 60Hz frame rate. The EP2C5T144C8 Cyclone-ii FPGA based board used in this project consists of on-board flash memory to hold PLB (Programmable Logic Block) configurations, SM (Switch Matrix) configurations, and LUTs (Look-Up Tables). It also consists of on-board 3.3v voltage regulator, and crystal oscillator chip which generates 50MHz stable frequency which is feed into Pin_17 of FPGA. As per the VGA industrial standard resolution of 640x480 (@60Hz) the pixel clock frequency is 25.175MHz which is approximately half of on-board oscillator's output clock frequency. To convert this 50MHz clock at Pin_17 of FPGA into 25MHz internal clock an inverted input D-flipflop (or T-flipflop) RTL is described in VHDL to divide this clock by 2 (i.e., 50MHz/2 = 25MHz).

Reference

[1] Kalomiros J. A., Lygouras J., Design and evaluation of a hardware/software FPGA-based system for fast image processing, Microprocessors and Microsystems, Elsevier, pp. 95– pp. 106, doi:10.1016/j.micpro.2007.09.001.

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