International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 09 Issue: 01 | Jan - 2025 SJIF Rating: 8.448 ISSN: 2582-3930

Si-ring quantum-well GAA nanowire FET for 5nm CMOS integration

Gurijala Adi Ram Charan
Electronics and Communication Engineering Institute of Aeronautical Engineering Hyderabad,Telangana,India
adiramcharang@gmail.com

Pawar Amber Singh
Electronics and Communication Engineering Institute of Aeronautical Engineering
Hyderabad,Telangana,India
ambersinghpawar13@gmail.com

Janampally Rahul
Electronics and Communication Engineering Institute of Aeronautical Engineering Hyderabad,Telangana,India
janampallyrahul007@gmail.com

Mr. B Naresh,Assistant Professor *Electronics and Communication Engineering Institute of Aeronautical Engineering*
Hyderabad,Telangana,India
b.naresh@iare.ac.in

***Abstract*—Short-channel effects are a series of phenomena that take place when the channel length of the MOSFET becomes approximately equal to the space charge regions of source and drain junctions with the substrate. They lead to a series of issues including polysilicon gate depletion effect, threshold voltage rolloff, drain- induced barrier lowering (DIBL), velocity saturation, reverse leakage current rise, mobility reduction, hot carrier effects, and similar other annoyances in 5nm scale of transistor. So, to overcome the short- channel effects, gate leakage, and increased variability various methods have been proposed in order to improve the performance of these devices, including the use of materials with high carrier mobility such as germanium or III–V materials, multi gate transistors, tunneling FET (TFET) structures, and structure quantum wells, any of which can significantly reduce SCE (short channel effect).In this paper Si-ring GAA NW FET has proposed due to it has lower static leakage current and a smaller subthreshold slope than conventional MOSFET and GAA, and a good level of electrostatic control is created in the channel due to the channel being surrounded by the cylindrical gate. The performance of the device and its electrical characteristics have been determined using sentaurus TCAD.**

***Index Terms*—tunneling FET,drain-induced barrier lowering (DIBL), quantum wells,**

I. INTRODUCTION

Recently, to develop advanced CMOS technology beyond the 5nm node, GAA NWs or stack NWs MOSFETs have at- tracted increasing interest because of their exceptional channel control ability and their excellent process compatibility with the existing high-k/metal gate (HKMG) FinFET technology in mass production [1]. Scaling FinFETs beyond 7 nm node results in exacerbated SCEs, motivating a move from a tri- gate architecture to a gate-all-around architecture. Among the gateall- around architectures explored by the semiconductor industry, while the nanowires provided best electrostatic con- trol, wider nanosheets are the ones that provide higher" on" current and improved electrostatic control over FinFETs [2].

Quantum well structures have been extensively investigated due to their ability to confine charge carriers in two di-mensions, enhancing quantum effects such as quantization of

energy levels. Silicon (Si) has been a preferred material for many electronic and optoelectronic applications because of its well-understood properties, abundance, and compatibility with existing semiconductor manufacturing processes. However, the ongoing miniaturization of semiconductor devices has driven the exploration of Si-based quantum wells (QWs) at the nanoscale to achieve enhanced quantum confinement and quantum transport phenomena.

Among the different geometries, ring-shaped quantum wells (Si ring QWs) are emerging as a promising configuration for nanoelectronics, especially at scales as small as 5nm. At these dimensions, quantum confinement in all three dimensions be- comes significant, altering the electronic and optical properties of the material. Si ring QWs offer unique features such as the ability to modulate carrier mobility, tunable energy band structures, and potential application in quantum computing and optoelectronic devices.

In a 5nm scale Si ring QW, quantum effects become prominent due to the strong confinement of carriers, which can lead to phenomena like Aharonov-Bohm oscillations and enhanced Coulomb interactions between confined electrons. These quantum effects provide a foundation for future appli- cations in nanoelectronics, where energy efficiency, switching speeds, and device density are paramount concerns.

One key challenge in fabricating Si ring QWs at this scale is maintaining structural integrity while preserving high-quality interfaces. Advanced fabrication techniques, such as atomic layer deposition (ALD) and molecular beam epitaxy (MBE), are employed to create these structures with atomic precision. In addition, the use of novel dielectric materials in conjunction with Si QWs can significantly enhance the performance of nanoscale devices.

Recent studies have demonstrated that Si ring QWs show promise in various applications, including low-power transistors, photodetectors, and even quantum bits (qubits) for quantum computation [3][4]. The ability to tailor quantum confinement effects through geometric and material optimization offers exciting opportunities for innovation at the 5nm scale.

II. MODELS AND METHOD

A. Si-ring QW 5 nm GAA model

Modeling Si-ring quantum wells (QWs) at the 5nm scale involves simulating both the electronic and structural properties to understand the quantum confinement and transport behavior.

FEM is employed to solve the Schrödinger and Poisson equations in nanostructures, including Si-ring QWs. This method provides spatially resolved solutions and is particularly effective for modeling the potential and electric fields within the quantum well. FEM can also simulate strain effects and surface roughness, which become crucial at the 5nm scale, affecting carrier mobility and quantum confinement [5].

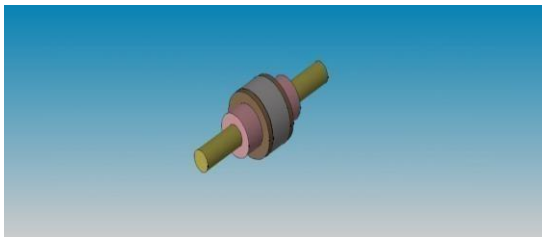

Fig.1. 3D model of Si-ring QW GAA FET

In conventional classical models like the drift-diffusion model, carriers (electrons and holes) are treated as point particles, and their behavior is governed by the classical laws of motion under the influence of electric and magnetic fields. However, as the dimensions of devices shrink to the nanometer scale (e.g., 5nm), quantum mechanical effects—such as the wave nature of carriers and confinement—become important. The DGM introduces a correction to account for these effects by incorporating a quantum potential that is derived from the gradients of the electron density. These

potential mimics the quantum confinement effects by penalizing regions where the electron density changes rapidly, such as at interfaces or in confined regions like quantum wells [6][7].

They were models for 5 nm scale transistor and most of the transistor are FINFET but they failed to solve the short channel effect, polysilicon gate depletion effect, threshold voltage rolloff, drain-induced barrier lowering (DIBL), velocity saturation, reverse leakage current rise, mobility reduction, hot carrier effects. So, to address such problem the GAA FET are popular solution to be used in many studies to solve short-channel effects and other annoyances and many researchers around the world were used many materials to solve the issue of the short-channel effect.

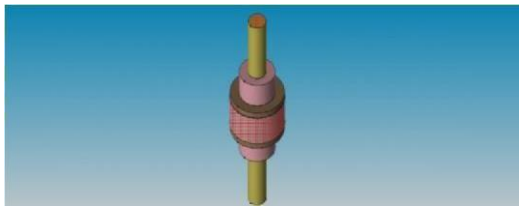

Fig.2. meshing of si-ring QW GAA FET

From the fig.1 and fig.2 we can see the model for 5nm siring quantum well Gate All Around where we have source and the material for the source is Germanium and drain made of Germanium lastly channel is also made of Germanium. Though the material is same for drain, source and channel. The doping concentration and type of doping is different for source/drain and channel. Along with there is silicon material is surrounded some part of channel. Silicon rings are used in 5nm scale transistors primarily because they offer excellent control over electron mobility and minimize leakage currents, critical for improving the performance of transistors at such a small scale. The silicon material provides a stable platform with high carrier mobility, allowing for the efficient transport of electrons even as the transistor dimensions shrink to the nanometer scale. Additionally, silicon's well-known properties, such as its compatibility with existing fabrication technologies and its ability to form stable oxides (like silicon dioxide), make it ideal for reliable transistor manufacturing.

At the 5nm scale, the use of a silicon ring structure helps in reducing short-channel effects, which are a major issue in transistors of such small dimensions. These effects lead to reduced gate control over the channel, resulting in increased leakage currents and power dissipation. Silicon rings allow for improved electrostatic control by surrounding the channel region more effectively, thereby enhancing gate performance and reducing these undesirable effects.

Moreover, silicon's band structure can be engineered to provide optimal on/off switching characteristics, further boosting the overall performance of transistors at such small dimensions. Silicon's mature technology and its ability to support high-yield manufacturing at nanoscales ensure its continued use in 5nm transistor development [9][10].

The above the silicon ring the HfO2 dielectric material is used as dielectric material.

Hafnium dioxide (HfO_2) is widely used as a dielectric material in modern transistors, particularly in metaloxidesemiconductor field-effect transistors (MOSFETs), due to its high dielectric constant ($\kappa \sim 20$-25), excellent thermal stability, and compatibility with silicon-based processes.

As device dimensions have scaled down into the nanometer regime, traditional silicon dioxide (SiO_2) gate dielectrics have become too thin to effectively prevent leakage currents, resulting in increased power consumption and reduced device reliability.

HfO_2, with its higher dielectric constant, allows for a thicker insulating layer while maintaining the same capacitance, thus reducing leakage current and power consumption without sacrificing transistor performance. Additionally, HfO_2 is stable at the high temperatures used in semiconductor fabrication, making it suitable for integration in advanced CMOS technology nodes [8]. So, it is used for 5nm scale transistor

TABLE 1

S.no	ıe of doping profile	Amount of concentration
1	S/D doping (arsenic for nFET and boron for pFET)	1×10^{20} (cm-3)
2	Channel doping (boron for nFET and arsenic for pFET)	1×10^{15} (cm-3)

Arsenic (As) and boron (B) are used as dopants in germanium (Ge) for 5nm scale transistors due to their ability to modify the electrical properties of the semiconductor to create n-type and ptype regions, which are essential for transistor operation. Arsenic, being a group V element, introduces additional electrons into the conduction band of germanium, thus making it an n-type dopant. This results in an increase in the number of free electrons that act as majority charge carriers, enhancing conductivity. On the other hand, boron, a group III element, creates "holes" or vacancies in the valence band by accepting electrons, making it a p-type dopant. This increases hole mobility, which is critical for the p-type region of the transistor. The combination of these dopants in germanium allows for the creation of highly conductive n-type and p-type regions in a single semiconductor substrate. At the 5nm scale, the choice of germanium as a base material is significant due to its higher electron and hole mobility compared to silicon, which is crucial for maintaining high-speed transistor performance at reduced dimensions. The precise control of doping levels and junctions with arsenic and boron is essential for minimizing leakage currents, ensuring reliable switching, and enhancing the overall performance of transistors at such a small scale [11].

Cobalt (Co) is used as a gate material for 5nm scale transistors due to its desirable electrical and magnetic properties, as well as its compatibility with advanced manufacturing techniques. At this scale, conventional materials like silicon face significant challenges due to quantum mechanical effects such as tunneling and increased resistance. Cobalt, being a metal with excellent conductivity, reduces gate resistance, improving the overall speed and performance of the transistor. Additionally, cobalt forms stable metal-semiconductor interfaces, which helps in minimizing electron scattering and leakage currents, both critical issues at nanoscales. So, the ability to create lowresistance contacts with silicon and other semiconductors also makes it a strong candidate for ensuring that electrical connections remain reliable as device dimensions shrink. Furthermore, cobalt's integration into metal gate stacks allows for the use of new high- k dielectric materials, which are essential for controlling leakage current and improving capacitance [12][13].

III RESULTS

Figure 3 shows that object is shown from a perspective view that reveals a cylindrical structure with several distinct

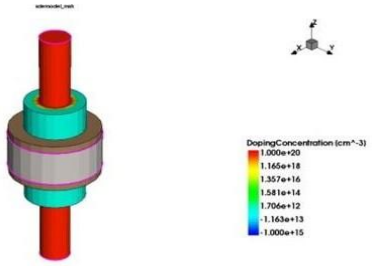

Fig.3. 3 D Doping Concentration

regions, each characterized by a different color. The color map on the right side indicates doping concentrations ranging from (1.0×10^{20} cm^{-3}) (red) to (-1.000×10^{15} cm^{-3}) (dark blue). The cylindrical structure is composed of concentric layers of varying doping concentrations. The outermost layer is in the brown color range, corresponding to a moderate doping concentration, while the inner layers exhibit higher concentrations, particularly towards the center, where the red region suggests a highly doped core.

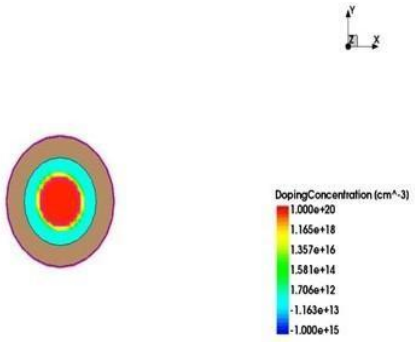

Fig.4. Doping Concentration

Figure. 4 shows a cross-sectional view of the same cylindrical structure, looking directly down the Z-axis. This view clearly reveals the layered nature of the doping profile, with the same color scheme showing how doping concentration changes as you move radially outward from the center of the cylinder. At the center, the highly doped red core is surrounded by layers of progressively lower doping concentrations as indicated by the transition from red to yellow, then green, cyan, and brown. This cross-sectional view suggests that the central region, likely the active region of the device, is heavily doped, while the outer layers, which could act as insulation or passivation, have lower doping levels.

The transitions between colors are smooth, suggesting that the doping process or a graded junction. The innermost red region is the most highly doped and could represent the part of the device where high conductivity or carrier injection is required. The high doping concentration at the center might suggest a need for high conductivity or fast carrier transport in that region, while the lower doped outer regions could be intended to control leakage currents, improve thermal stability, or provide mechanical stability.

The gradient in doping concentration could also indicate a desire to control the electric field distribution within the device. For example, in high-power devices, a graded doping profile helps to spread the electric field more evenly across the structure, reducing the risk of breakdown in any one region. the two images depict a 3D cylindrical structure with a

complex doping profile, where doping concentration is highest at the center and decreases towards the outer layers. The device is likely a semiconductor component with a specific doping profile designed to optimize its electronic properties, such as conductivity, electric field distribution, and carrier mobility. The graded doping profile and concentric layer design suggest that the structure could be used in advanced electronic or optoelectronic devices such as power transistors, photovoltaic cells, or nanoscale semiconductor components. The careful control of doping concentrations in different regions is crucial for achieving the desired performance and reliability of the device.

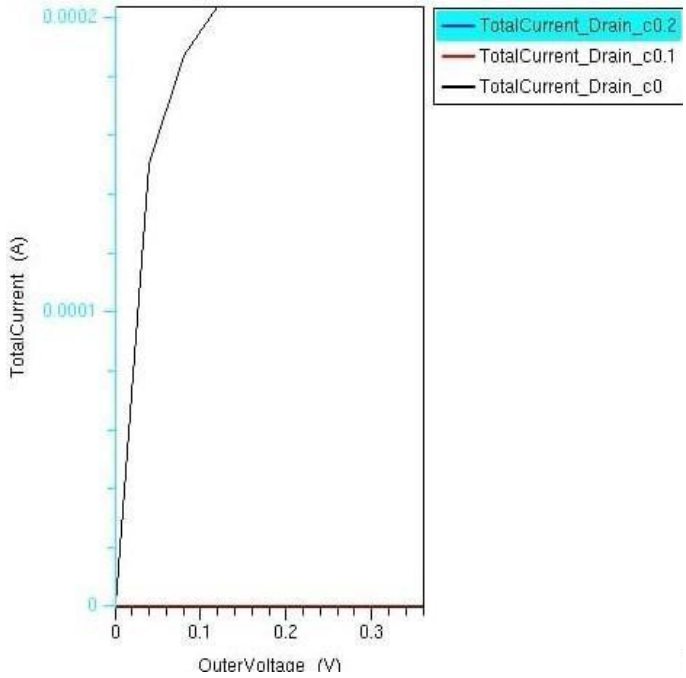

Fig.5. Id-Vd characteristics

The plot presented here shows the **Drain Current (ID)** as a function of **Drain Voltage (VD)**, commonly referred to as an ID
-VD characteristic curve, for a FET (Field-Effect Transistor). The x-axis represents the drain voltage (OuterVoltage) in volts (V), while the y-axis represents the drain current (TotalCurrent) in amperes (A). The plot contains three distinct curves labeled TotalCurrent_Drain_c0, TotalCurrent_Drain_c0.1, and TotalCurrent_Drain_c0.2, which may correspond to different experimental conditions or device configurations, likely involving variations in gate voltage.

In this graph, the current initially rises steeply as the drain voltage increases, which is characteristic of the linear (ohmic) region where the current increases linearly with voltage. However, as the voltage continues to rise, each curve begins to level off, indicating a transition towards a saturation region where further increases in drain voltage result in minimal changes in current. This behavior is a typical FET response, where at low drain voltages, the device operates in a region where the channel resistance determines the current. At higher voltages, the current reaches a quasi-saturation level as the channel is pinched off near the drain end.

The three curves exhibit different magnitudes of saturation current, with TotalCurrent_Drain_c0.2 (cyan) achieving the highest current, followed by TotalCurrent_Drain_c0.1 (red) and then TotalCurrent_Drain_c0 (black). This suggests that as we move from c0 to c0.2, there is an increase in either gate voltage or another parameter enhancing the channel conductivity, resulting in higher drain current. The differences in these curves indicate how sensitive the drain current is to gate control or other parameters in this device structure.

TABLE 2

Curve label	Color	Max Drain Current (A)	Behaviour Summary
TotalCurrent_Drain_c0	Black	~10^{-5}	High initial rise and saturation
TotalCurrent_Drain_c0.1	Red	~10-10	Moderate rise, stabilizes at lower current
TotalCurrent_Drain_c0.2	Cyan	~10-20	Minimal current, no significant increase

IV CONCLUSION

In summary, this plot demonstrates the typical output characteristics of a FET, showing both the linear and saturation regions, with variations in drain current magnitude across the curves, likely due to different gate biases or material properties. The distinct curves provide insights into how parameter adjustments can modulate the current, which is crucial for optimizing the device's performance for various applications.

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