International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 07 Issue: 12 | December - 2023 SJIF Rating: 8.176 ISSN: 2582-3930

Simplified Bilayer TFETS with Oxide and Group-IV Semiconductor For P-Channel Operation

Dandagala Sukanya[1] Padala Kavya[2] Dr.J.V.Suman[3]
1 UG Student, Dept. of ECE, GMR Institute of Technology, Rajam
2 UG Student, Dept. of ECE, GMR Institute of Technology, Rajam
3 Asst.Prof, Dept. of ECE, GMR Institute of Technology, Rajam
Sukanyadandagala24@gmail.com

Abstract

The paper proposes a p-channel bilayer TFET composed of an n-type oxide semiconductor (n-OS)/p-type group-IV semiconductor (p-IV) heterostructure, allowing for both n- and p-channel TFET operations under the same device structure. The p-IV side in the heterostructure has a metal-oxide-semiconductor (MOS) gate-stack that modulates the surface potential of the p-IV MOS interface and controls the band-to-band tunneling (BTBT) current during p-TFET operation. Technology computer-aided design (TCAD) simulation is used to predict the p-TFET operation with symmetric electrical characteristics to the n-TFET operation. The p-TFET operation of the n-ZnSnO/p-SiGe bilayer device is experimentally demonstrated on a SiGe-on-insulator substrate, under Si back-gate operation. Both n- and p-TFET operations are observed in an identical device by using the top- and back-gate electrodes.

Keywords: Bilayer, n-TFET, p-TFET, SiGe, SiGe-on-insulator (SiGeOI), ZnSnO

1.Introduction

The paper proposes a p-channel bilayer TFET composed of an n-type oxide semiconductor (n-OS)/p-type group-IV semiconductor (p-IV) heterostructure, enabling both n- and p-channel TFET operations under the same device structure. The introduction of a backside gate-stack to the p-IV layer in the n-OSp-IV stacked tunnelling junction allows for p-channel TFET operation by controlling the surface potential of the p-IV channel. The bilayer TFET structure is composed of a heterodyning junction of an n-type oxide semiconductor (n-OS) and a p-type group-IV semiconductor (p-IV) with type-II energy band alignment. The lower conduction band minimum of OS materials compared to group-IV semiconductors enables type-II energy band alignment, increasing the band-to-band tunnelling (BTBT) probability without increasing

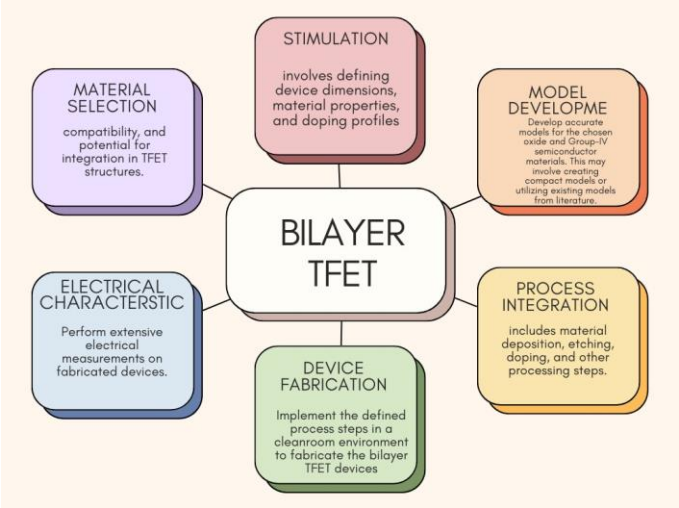
the OFF-state leakage current. The paper experimentally demonstrates both n- and p-TFET operations in a single ZnSnOSiGe bilayer TFET, achieving similar ION values for both n- and p-TFETs.

2.Literature Survey

This paper introduces a groundbreaking concept—a bilayer Tunnel Field-Effect Transistor (TFET) that accommodates both n-channel and p-channel operations within the same device structure. Traditionally, TFETs have been limited to either n-channel or p-channel configurations, but this proposal presents a design that allows for both within a single device.The structure of this TFET comprises two distinct semiconductors: an n-type oxide semiconductor (n-OS) and a p-type group-IV semiconductor (p-IV) arranged in a heterostructure. This heterostructure facilitates tunnelling across the junction between these two layers, taking advantage of their type-II energy band alignment. One significant innovation lies in the introduction of a backside gate-stack specifically applied to the p-IV layer within the n-OS/p-IV stacked tunnelling junction. This gate-stack manipulation enables the control of the surface potential of the p-IV channel, a critical factor in achieving p-channel TFET operation. The experimental validation of this concept is demonstrated through the creation of a ZnSnOSiGe bilayer TFET. This device successfully showcases both n-channel and p-channel TFET operations, yielding similar ION (current-on) values for both modes. This parity in performance between n- and p-TFETs is a remarkable achievement and speaks to the feasibility and effectiveness of this proposed bilayer TFET design. The significance of this innovation extends to its potential applications in ultralow-power circuits on the widely used Si CMOS platform. By enabling complementary TFETs, which can handle both types of charge carriers efficiently, this advancement holds promise for energy-efficient and high-performance circuitry. Overall, this paper presents a novel and versatile approach in semiconductor device design, offering a pathway towards more efficient and adaptable transistor technologies, which are crucial for advancing modern electronics. Certainly! Bilayer TFETs (Tunnel Field Effect Transistors) are a type of transistor design that involves using two different materials in its structure. In this case, the focus is on creating these transistors using oxide materials and semiconductors made from Group-IV elements. The goal here is to make TFETs that work specifically for p-channel operation, which means they're designed to control the flow of positively charged particles (holes) within the transistor. A literature survey on this topic would involve gathering and summarizing various studies, research papers, or articles that discuss and analyse the use of these specific materials (oxides and Group-IV semiconductors) in creating bilayer TFETs that are tailored to work

effectively in allowing the flow of positive charges in transistors. The aim is to understand how these materials can be optimized to improve the performance of p-channel TFETs.

3.Project Design



3.1. Concept of P-Channel Bilayer Structure TFET

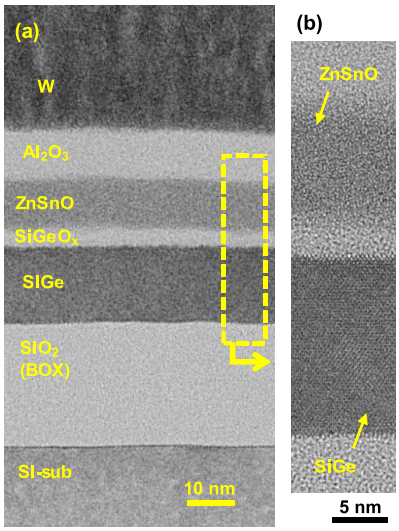
A p-channel bilayer TFET is a proposed device structure that allows for both n-channel and p-channel TFET operations under the same structure. In this structure, an n-type oxide semiconductor (n-OS) and a p-type group-IV semiconductor (p-IV) are combined to form a heterostructure. The p-IV side of the heterostructure has a metal-oxide-semiconductor (MOS) gate-stack that modulates the surface potential and controls the band-to-band tunnelling (BTBT) current during p-TFET operation. By applying a negative gate bias to the gate electrode, the surface potential of the p-IV channel is bent, inducing the overlap of density of states (DOS) between the n-OS source and the p-IV channel, allowing electrons in the p-IV channel to tunnel into the n-OS source, resulting in p-TFET operation. The back-gate configuration is used to simplify the fabrication process and enable the same structure to be utilized for both n- and p-channel bilayer TFETs.

3.2. TCAD Simulation

The proposed p-channel TFET and its electrical characteristics were studied using TCAD simulation with the Sentaurus device simulator. The simulation considered the device structures of both p-channel and n-channel bilayer TFETs.The materials used in the simulation were ZnO for the n-type oxide semiconductor (n-OS) and Ge for the p-type group-IV semiconductor (p-IV). The simulation assumed a uniform impurity concentration of 5 x 10^18 cm^-3 for both the n-ZnO and p-Ge layers. The simulation also considered the

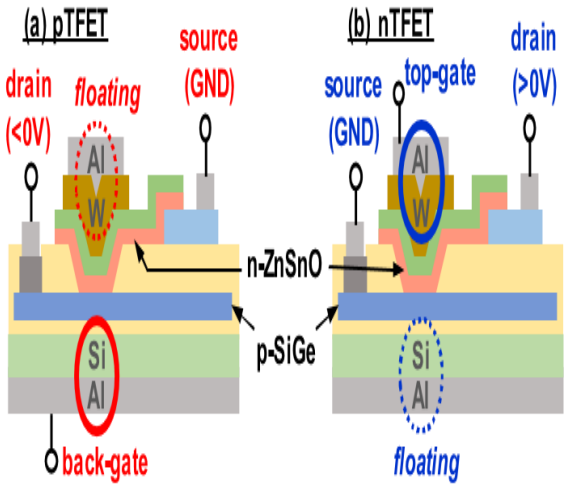
lateral length of the heterotunneling junction (L) to be 100 nm and the equivalent oxide thickness (EOT) of the gate insulator to be 4 nm. The TCAD simulation results showed the energy band diagrams and the I_d-V_g characteristics of both p-TFET and n-TFET operations.

3.3. Device Fabrication



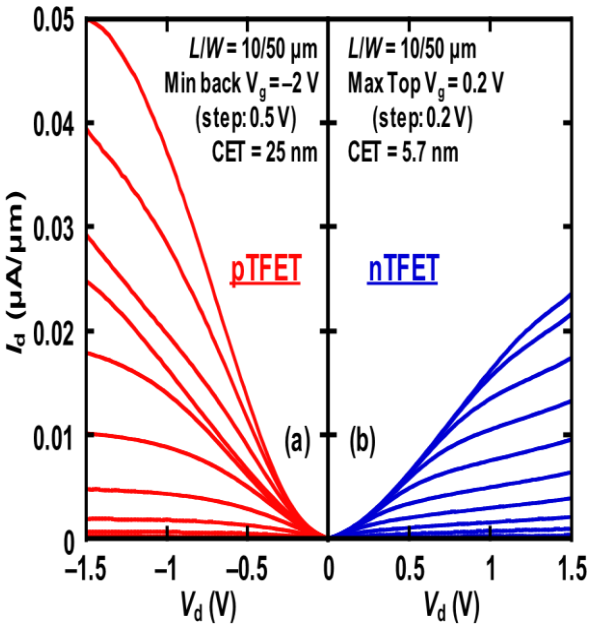
Bilayer TFETs composed of p-type SiGe -OI and n-type ZnSnO layers were fabricated for demonstrating the proposed p-TFET operation .The fabrication process involved several steps, including the isolation of the SiGe-OI layer by plasma etching, deposition of a SiO2 layer, patterning of the tunnelling region, formation of the InSnO buried drain, deposition of the ZnSnO layer using pulsed laser deposition (PLD), formation of a WAl2O3 top gate-stack, and formation of a Ni contact electrode on the SiGe layer. The gate-stack formation process included plasma and thermal treatments to improve the interface quality.

	p-TFET	n-TFET
p-SiGe	Channel	Source
n-ZnSnO	Source	Channel
Top W	(floating)	Gate
Back Al/Si-sub	Gate	(floating)
Ni	Drain M (< 0 V)	Source M (= 0 V)
ITO	Source M (= 0 V)	Drain M (> 0 V)



Cross-sectional transmission electron microscopy (TEM) images confirmed the stacked layers of amorphous ZnSnO and single-crystal SiGe, as well as the interfacial layer between the ZnSnO and SiGe layers. The device fabrication process for the p-channel TFET was similar to that of the n-channel TFET, which had already been demonstrated.

3.4. Electrical Characteristics



The p-TFET operation of the n-ZnSnO/p-SiGe bilayer device has been experimentally demonstrated, showing clear ON-OFF switching. The p-TFET operation is controlled by the back gate, and the electrical characteristics are obtained by changing the applied bias conditions. The p-TFET performance currently has a high subthreshold swing (SS) value of 900 mV/decade, which may be attributed to the interface states at the SiGeBOX interface and/or defects at the tunnelling junction. minimum SS value of the p-TFET is 91 mV/decade, which is higher than that of the n-TFET.The p-TFET exhibits a high OFF current (I_OFF) compared to the n-TFET, resulting in a small I_ON/I_OFF ratio. The symmetric I_ON values of the p-TFET and n-TFET are comparable, as expected from TCAD simulation.

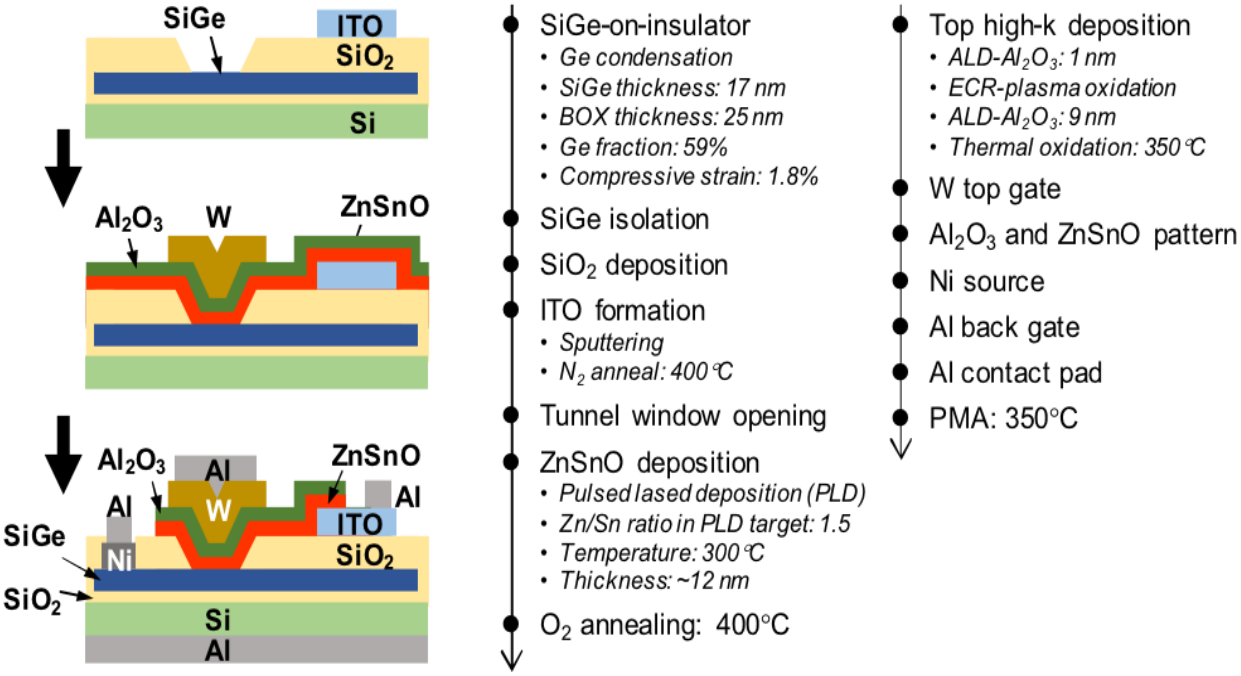
4. Future Perspective of Bilayer TFET Structure and Circuit Integration

The double-gate bilayer TFET structure with both top and back-gate electrodes has potential advantages, such as the adjustment of the threshold voltage and effective control of the surface potential of the channel. The double-gate structure allows for the effective decrease of supply voltage and dynamic control of the threshold voltage, leading to a reduction in power consumption of TFET circuits. By applying a positive bias to the sub gate, the conduction band minimum of the n-OS source layer can be shifted towards the

lower energy direction, resulting in a decrease in V_OFF from the p-channel TFET. However, very high positive bias on the sub gate can cause an increase in the average SS value over a certain V_g swing. The double-gate structure enables the realization of single-gate n- or p-channel TFETs when one of the two gate electrodes is electrically floating.

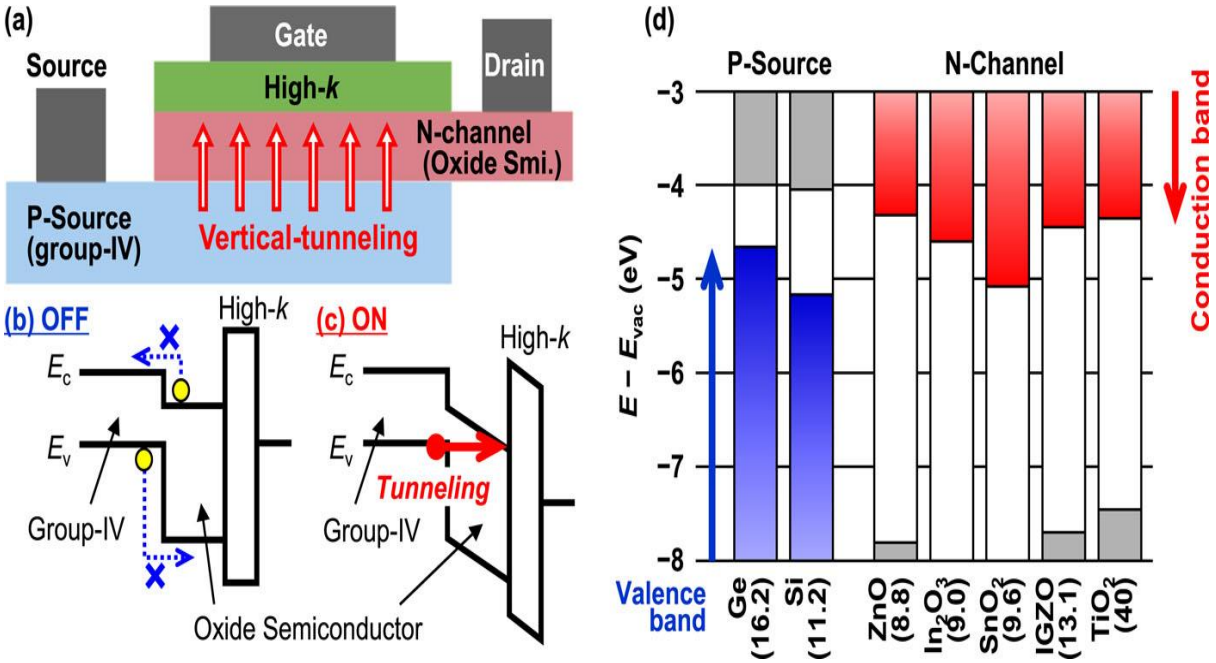
5. Practical Implementation

The proposed bilayer TFET structure presents a breakthrough by facilitating both n- and p-channel TFET operations within a single design. TCAD simulations showcase symmetric electrical characteristics for both n- and p-TFETs, validating their viability and balanced performance. Notably, experimental validation of p-TFET operation has been successfully achieved in a ZnSnOSiGe TFET, affirming the practical feasibility of the concept.



This innovative bilayer TFET design holds promise for complementary TFET operations, allowing both types of transistors to operate within the same structure. Such versatility streamlines semiconductor manufacturing processes and circuit design complexities by enabling complementary TFETs through a unified bilayer architecture. The ability to harness both n- and p-channel TFET functionalities within a single structure signifies a substantial advancement in semiconductor technology, offering potential benefits in power efficiency, circuit compactness, and performance optimization.Further exploration and refinement of this bilayer TFET architecture hold significant potential for advancing semiconductor device technology, potentially revolutionizing how complementary TFETs are integrated into practical circuit designs, leading to more efficient and versatile electronic systems.

5.1. Oxide Layer



Typically, an oxide layer such as silicon dioxide (SiO2) acts as one of the components in the bilayer structure. Oxides are chosen for their insulating properties and compatibility with semiconductor materials.

5.2. Group-IV Semiconductors:

These semiconductors, such as silicon (Si) or germanium (Ge), constitute the other layer of the bilayer structure. Group-IV materials are commonly used due to their well-understood properties and compatibility with existing semiconductor technologies.

5.3. Type-II Heterotunneling Junction:

This refers to the junction formed between the oxide and group-IV semiconductor layers. In a Type-II heterojunction, there is a staggered band alignment, allowing for favourable tunnelling characteristics, particularly for p-channel TFET operation. This junction design influences the tunnelling behaviour of charge carriers, crucial for the transistor's functionality.

6. Results

TCAD simulations anticipate balanced electrical traits for p-TFET operation, validating its potential efficacy. Using both top- and back-gate electrodes, the identical device exhibits both n- and p-TFET functionalities. This remarkable achievement highlights the versatility of the structure, showcasing its ability to accommodate both types of operations within a single device configuration. his innovation marks a significant advancement in semiconductor technology, offering a unified bilayer TFET capable of

supporting both n- and p-channel operations in a single device, potentially revolutionizing circuit design and enhancing electronic system efficiency.

7.Conclusion

Both n- and p-TFET operations are experimentally verified within a single device, a significant milestone showcasing their versatility. Attaining similar ION values for p-TFETs as in n-TFETs underscores the structure's efficiency in supporting both types of operations.

This breakthrough suggests a path towards complementary TFETs, offering immense potential for streamlined semiconductor technology and circuit design by harnessing both polarities within a unified bilayer struct.

8. Future Scope

The proposed p-channel bilayer TFET structure and operation scheme show potential for future low-power complementary circuit applications on the Si CMOS platform .The bilayer TFET structure composed of an n-type oxide semiconductor (n-OS) and a p-type group-IV semiconductor (p-IV) with type-II energy band alignment offers opportunities for improving the electrical performance of TFETs .Further research can focus on optimizing the design and fabrication processes of the bilayer TFETs to enhance their performance, such as increasing the ON-state current (ION) and the ON-OFF current ratio (ION/IOFF)

9. References

[1] D. Sarkar et al., “A sub thermionic tunnel field-effect transistor with an atomically thin channel,” Nature, vol. 526, no. 7571, pp. 91–95, Sep. 2015, Doi: 10.1038/nature15387.

[2] J. L. Padilla, C. Alper, F. Gámiz, and A. M. Ionescu, “Assessment of field-induced quantum confinement in heterogate germanium electron– hole bilayer tunnel field-effect transistor,” Appl. Phys. Lett., vol. 105, no. 8, Aug. 2014, Art. no. 082108, Doi: 10.1063/1.4894088.

[3] J. L. Padilla et al., “Gate leakage tunneling impact on the InAs/GaSb heterojunction electron–hole bilayer tunneling field-effect transistor,” IEEE Trans. Electron Devices, vol. 65, no. 10, pp. 4679–4686, Oct. 2018, Doi: 10.1109/TED.2018.2866123.

[4] U. E. Avci et al., "Energy efficiency comparison of nanowire heterojunction TFET and Si MOSFET at Lg=13 nm, including P-TFET and variation considerations," in IEDM Tech. Dig., Dec. 2013, pp. 830–833, Doi: 10.1109/IEDM.2013.6724744.

[5] G. Zhou et al., "InGaAs/InP tunnel FETs with a subthreshold swing of 93 mV/dec and ION/IOFF ratio near 106," IEEE Electron Dev. Lett., vol. 33, no. 6, pp. 782–784, Jun. 2012, Doi: 10.1109/LED.2012.2189546. [8] X. Zhao, A. Vardi, and J. A. del Alamo, "InGaAs/InAs heterojunction vertical nanowire tunnel FETs fabricated by a top-down approach," in IEDM Tech. Dig., Dec. 2014, pp. 590–593, Doi: 10.1109/ IEDM.2014.7047108.