International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 09 Issue: 06 | June - 2025 SJIF Rating: 8.586 ISSN: 2582-3930

Simulation And Analysis of Inverting and Non-Inverting Mixed-Logic 2x4 Decoders Using 32NM Finfet Technology

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ABSTRACT

This Project introduces the need for higher performance applications with low power consumption as we see there is lots of difficulty in using low power devices for a higher rank application like microprocessor, DSP, SRAM. As we know the Decoder plays an important role in memory design & logical circuit design. In this Project, we have been comparing the parameter Power delay product, Energy delay product, Power consumption, and Delay on 12T, 14T decoder base on MOS, FinFET, and FinFET using CMOS as proposed in 32nm technology. So the final proposed circuit is obtained by application of FinFET, to vary threshold from the ground path of the final 12T. Where we get significant improvement in proposed work.

KEYWORDS: High Delay, High Performance, 45nm Technology, FinFET 32nm Technology low power.

INTRODCUTION

In VLSI technology, as we know that it contains thousands of transistors in a single chip called Integrated circuits (IC) with an increase in transistor densities by the law of Moore's, also increasing the power consumption with higher clock frequency. Now the trade occurs, where we try to make efficient logic circuits to optimize the key factors like Power loss, leakage current, voltage source, etc through which we can make the device more efficient with low power consumption. VLSI occupies a comparatively a low area. The size of the circuits is lessened. Discrete components use a lot of power. The authenticity in using VLSI in circuits is extremely high. The operating speed of components powerfully increasing. The inclusive cost of the device is now reduced. The employ of VLSI in Digital Signal Processing Commercial Electronics, Automobiles, medicine. CMOS devices have two basic elements static power utilization is low high noise immunity.[7] CMOS production does not waste much heat as other logic, like NMOS type logic or TTL which have a current level state, when not in changing state. That feature allows to CMOS merge a high substance of logic functions on a chip. So CMOS is the most broadly used technology to be in the appliance in VLSI chip design. Storage register combinational logic and the associated interconnection are very easy to design and implement in both NMOS and CMOS Poly-silicon resistance is the most common gate electrode and interlayer connect material in use today in the manufacture of VLSI MOS devices. Poly-silicon

has many desirable properties including good etch ability, good oxidation characteristics, mechanical stability at high-temperature excellent step coverage, and adhesion. It's one major drawback is its relatively high resistance.

II.LITERATURE SURVEY

There are certain developments in SOI MOSFET with single gate, double gate, triple gate as well as gate all around structures. The bulk Si MOSFET has been the main device forming the backbone of the development of ultra-high density ICs. In order to reduce parasitic capacitances Silicon-on-insulator (SOI) technology used. The double-gate (top and bottom gate) silicon-on-insulator (SOI) MOSFET and the gate-all-around (GAA) device are the most suitable device structures for suppressing short-channel effects such as drain-induced barrier lowering (DIBL) and sub threshold slope degradation. A rigorous numerical model is developed for threshold voltage (Vth) that includes a dependence on the back gate bias .

It was observed that the DG transistor shows the best SCE control and performance. Some of the performance outcomes are given below: DG transistors exhibit the best electrical results in terms of SCEs and saturation Currents for both nMOS and pMOS transistors. DG devices exhibit a low symmetrical threshold voltage V_{th} adjusted to 0.45 V. Conversely, the GP architecture shows a very high threshold voltage due to the influence of the grounded back gate.

III.EXISTING METHOD

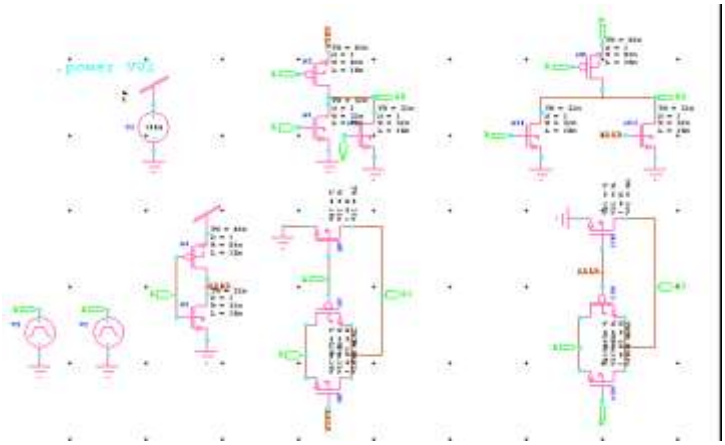


Fig .1. Schematic of 14 Transistor 2x4 Decoder using CMOS method.

In existing method a 2x4 decoder designed with 14T MOS and 15T By using TSpice simulation software, we include model file 45 nm technology, where all supply voltage are simulated at 1.8V and ground to 0V. In circuit topology we defined input voltage and output voltage on the basis of 2x4 decoder. In 15T CMOS added a new transistor in ground path in replacement of ground 0, so all main circuit are changes to ground 0 to new transistor and give a new a signal also. we give a pulse in between new signal and new transistor which activate the sleep mode by this changes with respect to ground are all changed in the ground. then analysis transient of circuit. we measure circuit analysis by using transient analysis (measure value as a function of time t=1n to t=500n) then measure average power and delay by measure command (used to measure rise and fall time delay) voltage V(2) to voltage V(31). For getting the

various parameter like PDP, EDP can be calculated by simple formulation which is describe next. As we know that PDP is the Power delay product which is the combination of calculated power & estimated delay. And another factor is the EDP stand for Energy power delay which is the combination of PDP & delay. So these factor are very useful in comparing the losses or improvement in design by using different mode of operation or technology.

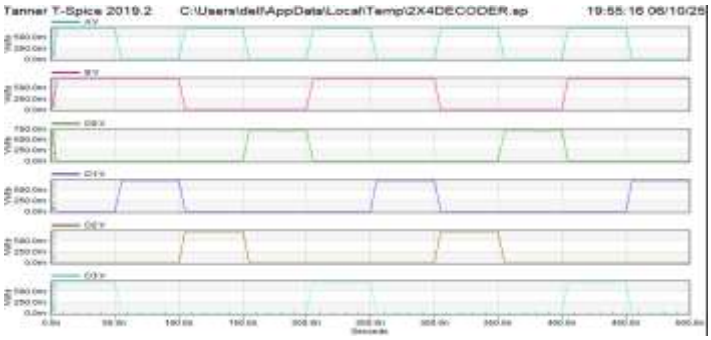


Fig.2.Schematic of 2x4 Decoder using 15 Transistor

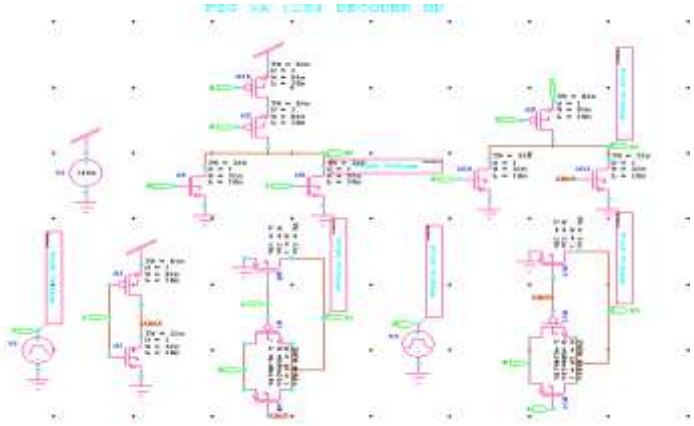


Fig.3.Simulation of 2x4 decoder using 15 Transistor CMOS methodology.

For schematic designing, TSpice tool is used for designing the circuit. 2x4 decoder based on CMOS 45 nm using 2x4 decoder is realize by the schematics of 2x4 decoder using 15T.

The 2x4 low power fourteen transistor decoder architecture have its limitations in terms of latency, which is caused by using input signal A in complement form while transmitting signals for D0 and I3 outputs. To complement input A signal, an inverter is utilized, which adds delay in that line. Despite this, static CMOS can correctly produce D0 and I3 outputs [5]. Fig 1. LP non-inverting decoder using fourteen. Schematic of High Power 2x4 decoder in figure 3 shown. using fifteen transistor. D0 to D3 output may be designed neither using a CMOS NOR gate. So, the number of transistors in both non-inverting and inverting decoder is now increased by one hence called fifteen transistor topologies. Hence by using 14 and 15 transistors the area occupied in silicon becomes more and delay occurred in producing the 2x4 decoder is more and power consumption also becomes more. So to counter above problems we promised a suitable solution with scaling of transistor technology.

PROPOSED METHOD

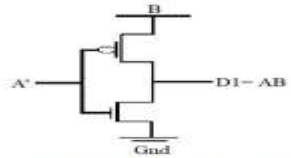
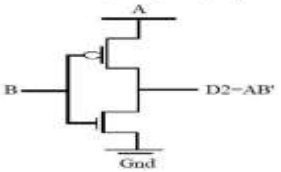


Figure 1. First Term (D1=AB) using Proposed Design



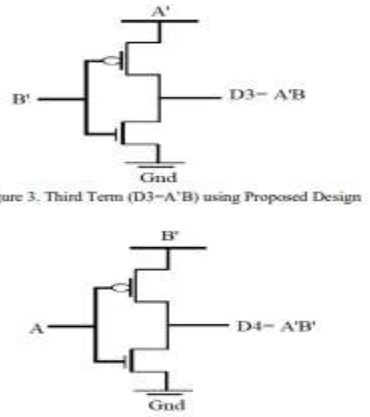


Figure 3. Third Term (D3=A'B) using Proposed Design

Fig.4.Proposed 2x4 Decoder with 12 transistors With LP Mode

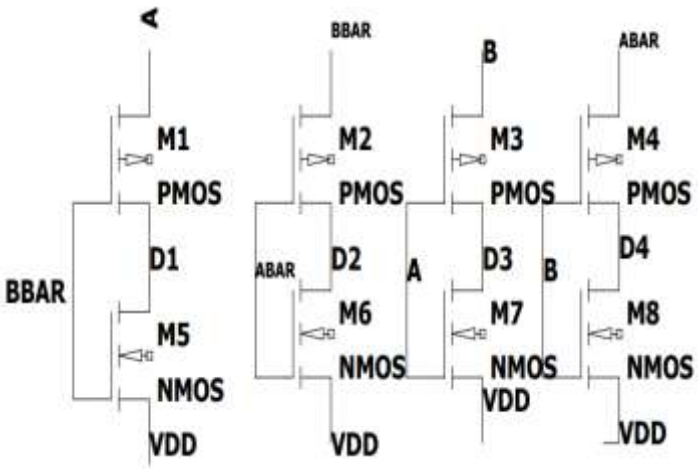


Fig.5 .Proposed 2x4 Decoder with 12 transistors With LP Inversion Mode

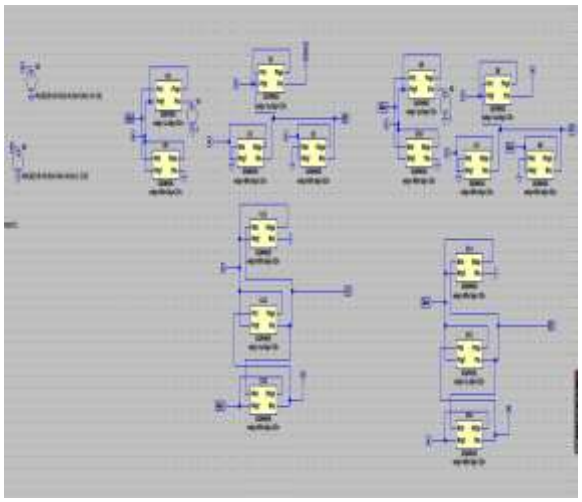


Fig.6. Simulation of 2x4 Decoder using 12 T Transistor using FinFET methodology

Diminishing chip area is additionally truly impressive factor, creators need to recall when suggesting any novel design.

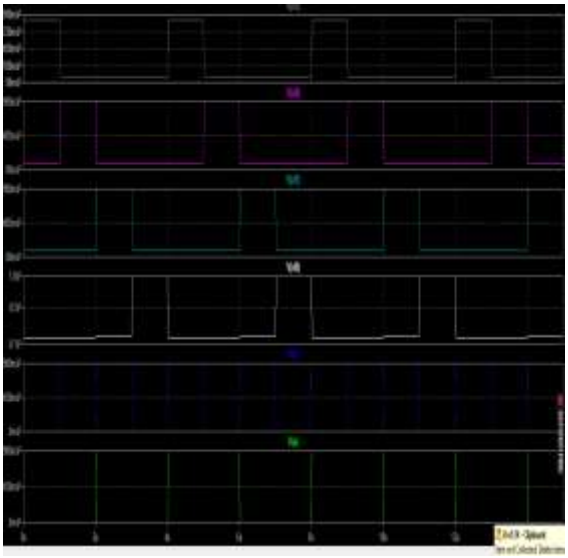


Fig.7.Simulation of 2x4 Decoder using 12 T Transistor using FinFET methodology

Decoder is used for conversion of binary inputs to associated output bits in a pattern. A novel 2x4 decoder with only 12 Transistor is proposed with area optimization in power project. CMOS logic is additionally used for execution of 2x4 decoders. Delay and power is used for evaluation between the novel design and CMOS logic. The novel design of 2x4 decoders is less optimized for power in contrast to CMOS logic design at a typical value of VDD.

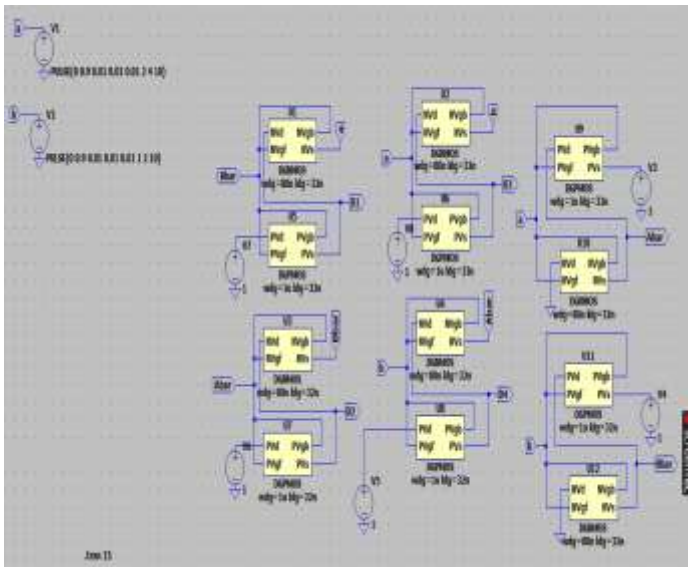


Fig .8. simulation of 2x4 Decoder using 12 T Inversion Transistor using FinFET methodology.

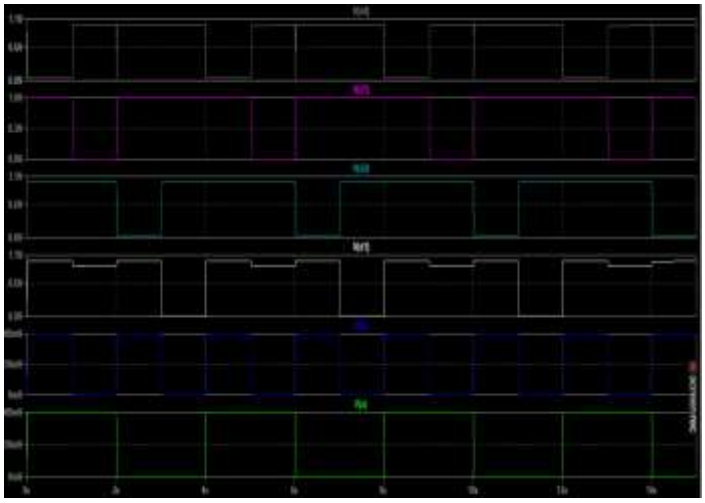


Fig.9.Fig simulation of 2x4 Decoder using 12 T Inversion Transistor using FinFET methodology.

COMPARISON TABLE

s.no	No of Transistors	Static Power	Dynamic power	Average power	delay
1	14T	35.1428 Nw	11.3788 Nw	2.8405 Nw	170.03
2	15T	36.0649 Nw	11.9334 Nw	3.0749 Nw	166.47
3	12T	12.85f	1.08f	6.96f W	0.003 s
4	12TI	30pW	15.90pw	10Pw	0.001 s

LAYOUT FOR 2x4 DECODER

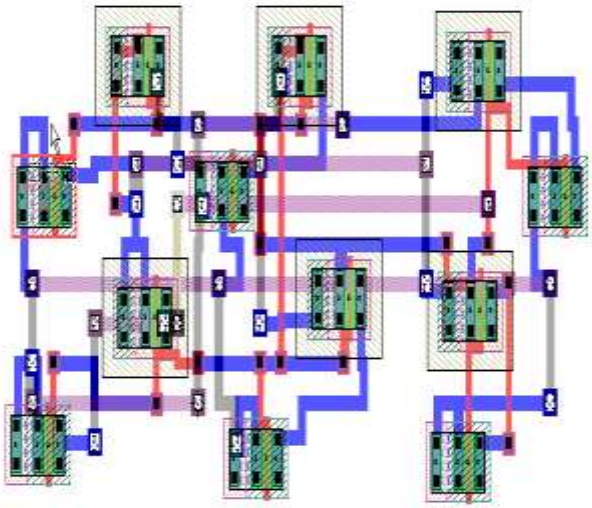


Fig.10. Layout of 2x4 Decoder using 12 T Transistor using Tanner

The CMOS design layouts are based on following components Substrates or Wells : These wells are p type for NMOS devices and n type for PMOS devices. Diffusion regions: At these regions the transistors are formed and also called as active layer. These are defined by n+ for NMOS and p+ for PMOS transistors The layout design rules provide a set of guidelines for constructing the various masks needed in the fabrication of integrated circuits. Design rules are consisting of the minimum width and minimum spacing requirements between objects on the different layers. The most important parameter used in design rules is the minimum line width. This parameter indicates the mask dimensions of the semiconductor material layers. Layout design rules are used to translate a circuit concept into an actual

geometry in silicon. The design rules is the media between circuit engineer and the IC fabrication engineer. The Circuit designers requires smaller designs with high performance and high circuit density whereas the IC fabrication engineer requires high yield process. Minimum line width (MLW) is the minimum MASK dimension that can be safely transferred to the semiconductor material. For the minimum dimension design rules differ from company to company and from process to process.

CONCLUSION

We got results from the simulation platform. where we find that power consumption is reduced by using FinFET as compare to MOSFET, which makes it a promising substitute for MOSFET beyond 32nm technology, due to short channel effects. We can compare the high speed and low PDP, and Low EDP by the value that improvement in power, Low variation in delay, respectively improvement in PDP and EDP. So, by the controlling of leakage current in ground path terminal, our performance is better high.

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