

Simulation of an approximate Discrete Cosine Transform architecture using Verilog

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ABSTRACT-This paper presents the simulation and implementation of an approximate Discrete Cosine Transform (DCT) architecture using Verilog for image compression applications. DCT, a key component in standards such as JPEG, transforms spatial data into frequency components to reduce redundancy. To address the high hardware complexity of conventional designs, the proposed architecture replaces multipliers with adders, subtractors, shift operations, and a clock gating technique, significantly reducing area and power consumption. The algorithm is initially validated in MATLAB R2020a and subsequently implemented on an FPGA using Xilinx Vivado targeting an Artix-7 XC7VX330T device. Experimental results demonstrate that the design achieves lower hardware complexity, improved processing efficiency, and reduced power usage, making it well-suited for real-time image compression systems.

Key Words: Approximate DCT, Image Compression, Verilog, FPGA, Xilinx Vivado, Low Power Design, Hardware Optimization, Clock Gating, Shift-and-Add, Real-Time Processing

1. INTRODUCTION

The rapid growth of digital multimedia devices has increased the demand for efficient image and video compression techniques to reduce storage and bandwidth requirements. The Discrete Cosine Transform (DCT) is widely used in standards such as JPEG and MPEG due to its ability to convert spatial data into frequency components and achieve high energy compaction. However, conventional DCT implementations require complex multipliers, leading to higher area and power consumption. To overcome this, simplified DCT architectures using adders, subtractors, shift operations, and clock gating are adopted. In this work, a multiplier-free DCT design using only adders and subtractors is proposed to reduce hardware complexity and improve processing speed, making it suitable for real-time applications.

2. LITERATURE SURVEY

Numerous research efforts have been dedicated to improving the performance and efficiency of Discrete Cosine Transform (DCT) architectures for image and video compression applications. Shabani et al. (2021) proposed an area- and power-efficient variable-sized DCT architecture for HEVC using a muxed-MCM approach to reduce hardware complexity. Mukherjee and Mukhopadhyay (2020) introduced a hardware-efficient 2D DCT/IDCT design using Taylor-series expansion to simplify trigonometric computations. Mert et al. (2017) developed a high-performance 2D transform architecture utilizing parallelism and pipelining techniques. Singhadia et al. (2020) presented a compact and efficient DCT/IDCT architecture for portable HEVC devices. Imen et al. (2021) focused on hardware acceleration of DCT-II for the VVC standard to enhance compression performance. Chatterjee and Sarawadkar (2018) proposed an optimized HEVC core transform using real-valued DCT coefficients. Xing et al. (2018) developed an energy-efficient approximate DCT for wireless medical applications. In addition, Chen et al. (2022) explored low-power approximate DCT designs for real-time systems. Kumar and Rao (2021) proposed a multiplier-less DCT architecture using shift-and-add operations to reduce hardware cost. Zhang et al. (2020) focused on FPGA-based optimized DCT implementations for high-speed processing. Lee et al. (2019) introduced a pipelined DCT architecture to improve throughput. Patel and Mehta (2022) designed a reconfigurable DCT structure for adaptive multimedia applications. Singh et al. (2021) proposed a low-latency DCT architecture for real-time video encoding. Wang et al. (2020) developed a high-efficiency DCT design with reduced memory usage. Additionally, several studies emphasize approximate and hardware-friendly DCT techniques to achieve a balance between performance, power consumption, and implementation cost, highlighting the continuous advancements in efficient DCT architectures for modern multimedia systems.

3. EXISTING METHODOLOGY

The block diagram illustrates the process of image compression and reconstruction using the Discrete Cosine Transform (DCT), as commonly employed in JPEG systems. The input image is divided into 8×8 blocks to reduce computational complexity, and each block is transformed from the spatial domain to the frequency domain using DCT, where most of the image energy is concentrated in low-frequency components. These coefficients are then compressed through quantization by reducing less significant high-frequency components, thereby minimizing data size. For reconstruction, the compressed data undergoes dequantization followed by Inverse DCT (IDCT) to convert it back into spatial domain pixel values. Finally, all blocks are combined to form the reconstructed image, which, despite slight quality loss due to quantization, achieves efficient compression with acceptable visual quality, making the architecture suitable for modern multimedia applications.

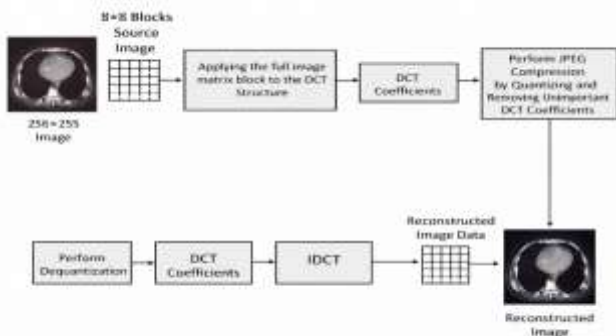


Figure 1 : DCT Architecture Block Diagram

LIMITATIONS: High hardware resource usage, increased design complexity, higher power consumption, approximation errors, pipeline latency, limited flexibility, area overhead, and scaling and normalization issues.

4. PROPOSED METHODOLOGY

The diagram illustrates a low-power image processing architecture based on the Discrete Cosine Transform (DCT). The system begins with an input image that undergoes a pre-processing stage to prepare the data for transformation. The processed data is then fed into DCT computation blocks consisting of multiple DCT units, enabling parallel processing and improved computational efficiency. To reduce power consumption, clock gating is applied to selectively disable inactive components, thereby minimizing switching activity and dynamic power usage. The transformed coefficients are

then passed through a post-processing stage for proper arrangement and formatting, and finally converted into the output image. This architecture effectively achieves efficient image compression with reduced power consumption, making it suitable for portable and embedded multimedia applications.

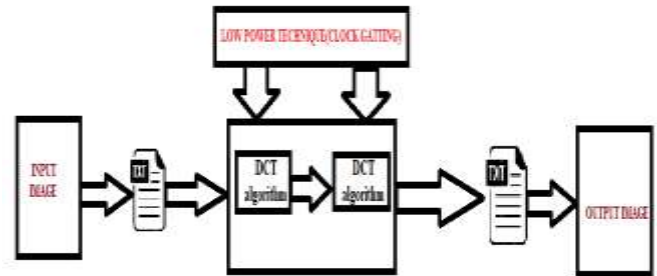


Figure 2: Proposed Block Diagram

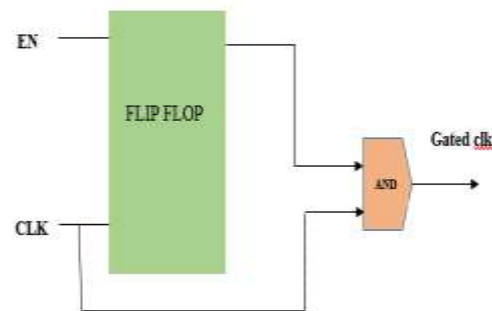


Figure 3: Proposed Flip-Flop based Clock Gating

The diagram presents a basic clock gating technique used to reduce power consumption in digital circuits by controlling the distribution of the clock signal. An enable signal (EN) is first synchronized with the clock (CLK) using a flip-flop to ensure glitch-free operation and stable signal transitions. The synchronized enable signal is then applied to an AND gate along with the clock signal to generate a gated clock output. When the enable signal is high, the clock is allowed to pass through, enabling normal circuit operation, whereas when the enable signal is low, the clock is blocked, effectively disabling inactive portions of the circuit. This approach significantly reduces unnecessary switching activity and dynamic power consumption, making it highly effective for low-power design in large-scale integrated systems.

5. RESULTS & DISCUSSION

METHODS	AREA(lut's)		POWER(W)		DELAY(ns)	
	Existing	Proposed	Existing	Proposed	Existing	Proposed
DCT	6590	6590	86.136	12.325	19.626	19.626
IDCT	6985	6986	96.296	5.405	18.978	18.978

Table 1: Comparison table for Existing and Proposed method

The table presents a comparative evaluation of the existing and proposed architectures for both Discrete Cosine Transform (DCT) and Inverse Discrete Cosine Transform (IDCT) based on key performance metrics, including area, power consumption, and delay. In terms of area, the DCT implementation shows no variation, with both existing and proposed methods utilizing 6590 LUTs, while the IDCT exhibits a negligible increase from 6985 LUTs to 6986 LUTs, indicating that the proposed design introduces minimal hardware overhead. With respect to power consumption, the proposed method achieves a significant reduction, decreasing from 86.136 W to 12.325 W for DCT and from 96.296 W to 5.405 W for IDCT, thereby demonstrating its effectiveness in low-power design, which is essential for modern VLSI systems and portable applications. Regarding delay, both DCT and IDCT maintain identical values in the existing and proposed methods, with DCT at 19.626 ns and IDCT at 18.978 ns, confirming that the power optimization does not introduce any additional latency. Overall, the proposed architecture offers substantial improvements in power efficiency while preserving comparable area and delay, making it a highly efficient solution for optimized DCT and IDCT implementations.

6. CONCLUSION

This work presents the design and implementation of an approximate Discrete Cosine Transform (DCT) architecture aimed at reducing hardware complexity for image compression applications. By replacing conventional multipliers with simpler operations such as adders, subtractors, shift operations, and incorporating clock gating, the proposed design significantly minimizes area and power consumption while maintaining efficient

performance. The functionality of the DCT algorithm was validated through MATLAB simulation, where the reconstructed images closely matched the original inputs, confirming effective compression capability. Furthermore, the hardware implementation using Verilog HDL and Xilinx Vivado demonstrated correct functionality, satisfactory timing performance, and efficient resource utilization. Overall, the proposed architecture achieves a balanced trade-off between complexity, power, and performance, making it a suitable and efficient solution for real-time image and video processing applications in modern digital systems.

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