International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 10 Issue: 03 | March - 2026 SJIF Rating: 8.659 ISSN: 2582-3930

Simulation of Dual Gate TFET Using Silvaco TCAD

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Abstract – The project aims to investigate the fundamental operating principles and performance characteristics of TFETs, which are promising candidates for low-power electronics due to their potential for a sub-60 mV/decade subthreshold swing. A Intrinsic channel silicon DG-TFET with a p-in structure was simulated. The report details the device structure, simulation methodology, and physical models employed. Key results, including the Id-Vg and Id-Vd characteristics, energy band diagrams, and internal physical properties, are analyzed. The simulation confirms the TFET's operation via band-to-band tunneling (BTBT), demonstrating steep-slope switching behavior. However, it also highlights the challenge of ambipolar conduction, a characteristic issue in TFET design.

Key Words: BTBT, TFET, Subthreshold swing, DG-TFET, Short channel effects, TCAD Simulation,

1.INTRODUCTION

As conventional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) approach their physical scaling limits, their power consumption has become a major bottleneck. The subthreshold swing (SS) of a MOSFET is fundamentally limited to 60 mV/decade at room temperature, which restricts the reduction of the threshold voltage and leads to significant leakage currents.

The continuous scaling of conventional MOSFETs faces severe limitations due to short-channel effects and increasing power dissipation. To overcome these challenges, advanced device architectures such as Tunnel Field-Effect Transistors (TFETs) have been widely investigated. TFETs operate based on band-to-band tunneling instead of thermionic emission, enabling subthreshold swings below the conventional 60 mV/dec limit at room temperature. This characteristic makes TFETs highly attractive for low-power and ultra-low-voltage applications.

A Dual Gate TFET (DG-TFET) structure further enhances device performance by improving electrostatic control over the channel region. The presence of two gates strengthens the electric field at the tunneling junction, leading to higher ON-current and improved switching behavior. Dual-gate configurations also help suppress short-channel effects and reduce leakage current.

The Tunneling Field-Effect Transistor (TFET) is an alternative device architecture that overcomes this limitation. Instead of relying on thermionic emission over a potential barrier, the TFET operates based on the quantum mechanical principle of band-to-band tunneling (BTBT). By modulating the tunneling barrier width with the gate voltage, a TFET can achieve a subthreshold swing below 60 mV/decade, enabling ultra-low power operation.

The objective of this project is to use the Silvaco TCAD framework to:

1. Construct a Double-Gate (DG) Intrinsic channel TFET structure.
2. Simulate its electrical characteristics (Id-Vg, Id-Vd).
3. Analyze the internal device physics, including energy bands and tunneling rates, to understand its operation.

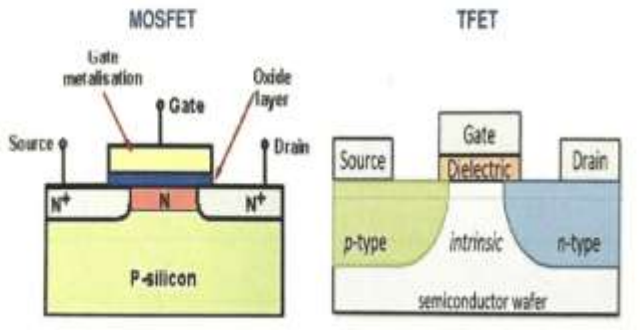


Fig:structure difference in MOSFET and TFET.

2. Device Structure and Simulation Code and Methodology

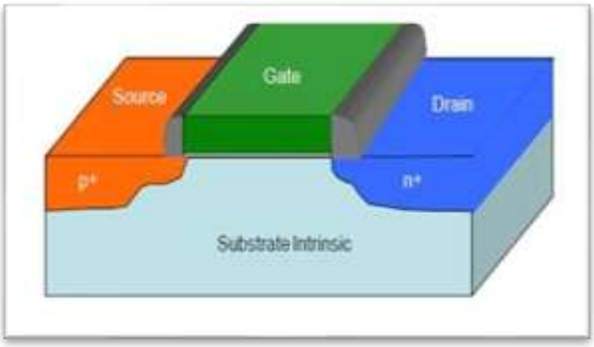


Fig: Device structure of an N-TFET

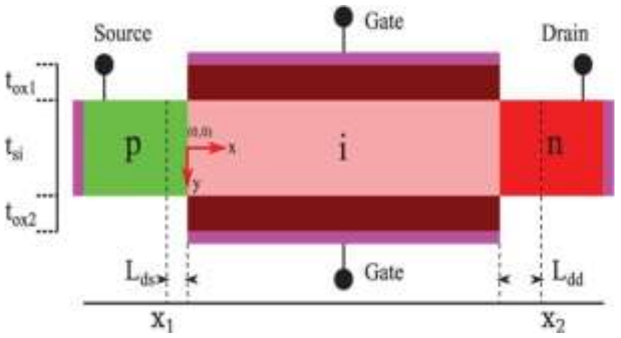


Fig: The basic structure of Double Gate TFET

While Tunneling Field-Effect Transistors (TFETs) excel in low-power applications, their inherent drawbacks, such as low ON current and ambipolar behavior, hinder further scaling efficiency. To overcome these limitations, a promising alternative emerges in the form of Double-Gate TFETs (DG-TFETs), incorporating an additional gate to enhance current flow. The foundational configuration of a DG-TFET is depicted in Fig. 5. DG-TFETs exhibit improved Band-to-Band tunneling characteristics, leading to increased ambipolar current, as illustrated in Fig. 6 and Fig. 7. Projections suggest that a double-gate TFET with a high I_{on}/I_{off} ratio can achieve a sub-threshold slope of less than 60mV/decade.

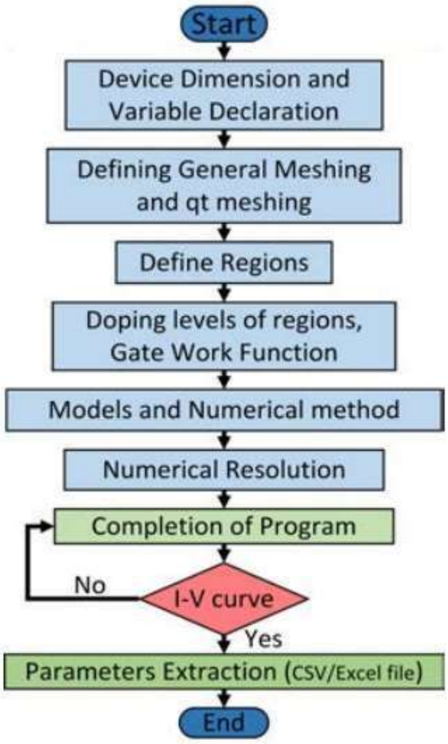


Fig:simulation process of the TCAD

The simulation of engineered devices is conducted using a 2D device simulator TCAD tool. To accurately capture the internal functioning of the devices, a nonlocal band-toband (B2B) tunneling model is employed. This model incorporates quantum tunneling phenomena at the SCIn (source/channel interface) and DCIn (channel/drain interface) by delineating a quantum tunneling region. This ensures precise simulation of the tunneling process of charge carriers at both interfaces.

Proposed system:

In this design, a symmetrical dual-gate configuration is implemented to achieve superior electrostatic control over the channel region and to reduce short channel effects. A high-k gate dielectric material is proposed instead of conventional SiO_2 to improve gate capacitance and minimize leakage current. Gate work function engineering is applied to precisely control the threshold voltage. To enhance the tunneling probability and increase the ON current, source pocket engineering is introduced near the source-channel junction, thereby reducing the tunneling barrier width. The source region is heavily doped to promote strong band-to-band tunneling, while the drain doping is optimized to suppress ambipolar conduction. A lightly doped or intrinsic channel is used to reduce OFF current. Advanced physical models such as non-local band-to-band tunneling (BTBT), Shockley-Read-Hall recombination, bandgap narrowing, and field-dependent mobility models are enabled to ensure accurate simulation of carrier transport Fine meshing is applied near the tunneling junction to improve electric field accuracy and convergence stability. The transfer characteristics (ID–VG) and output characteristics (ID–VD) are extracted to evaluate device performance, and parameters such as subthreshold slope, ION, IOFF, ION/IOFF ratio, and threshold voltage are calculated. Energy band diagrams and electric field distributions are analyzed at different bias conditions to study tunneling behavior. The proposed design targets a steep subthreshold slope below 60 mV/dec, higher ON current, reduced leakage current, minimized ambipolar behavior, and improved switching efficiency. By optimizing structural parameters such as oxide thickness, channel length, and gate material, the proposed DG-TFET demonstrates superior current drive capability, reduced power consumption, and enhanced suitability for low-power nano electronic applications compared to the existing system.

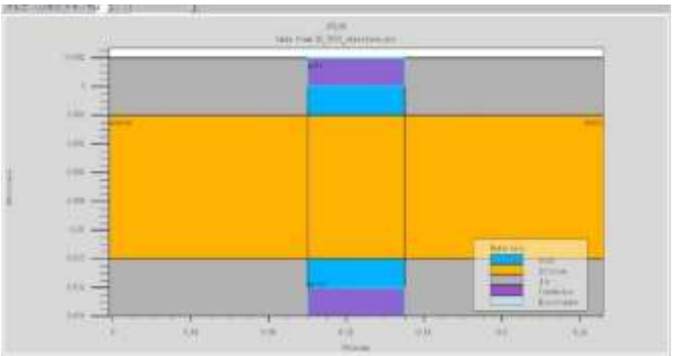


Fig : MOSFET Structure

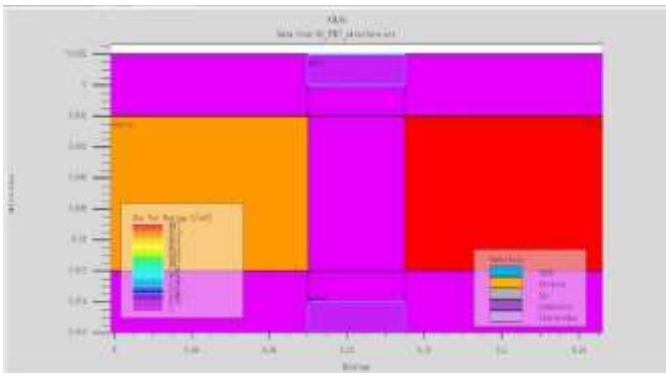
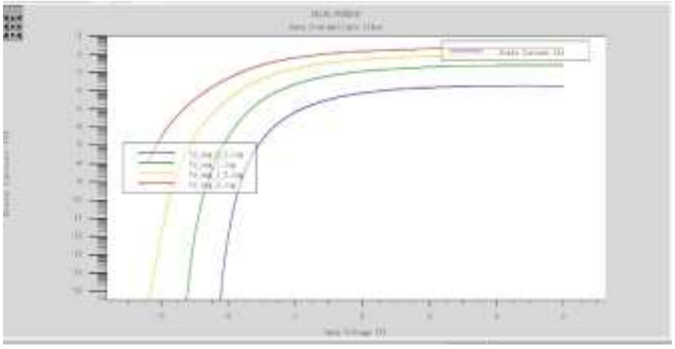


Fig: DG-FET Structure

Results:



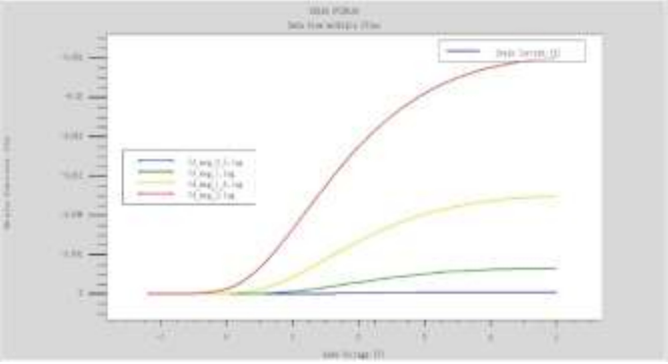
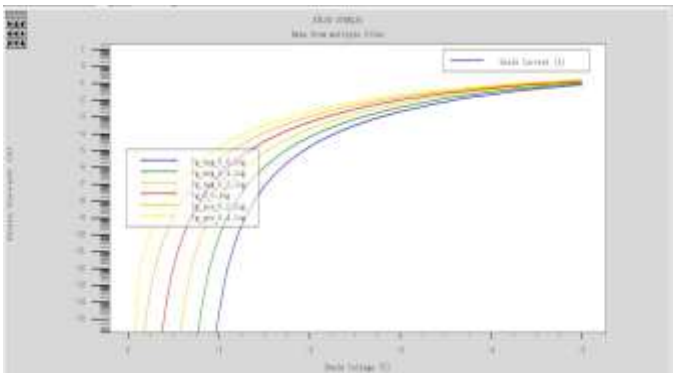


Fig: Drain current v/s Gate voltage



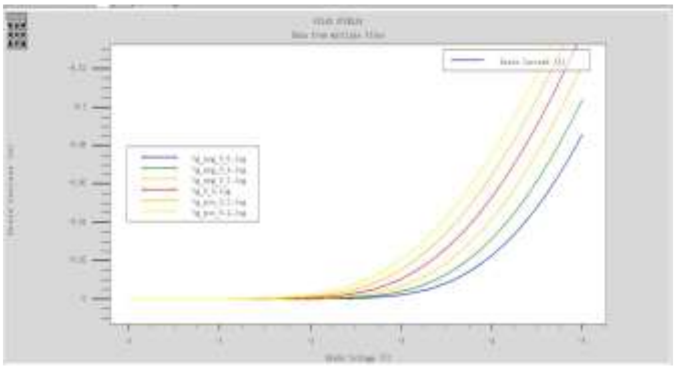


Fig: Output characteristics (Id-Vd)

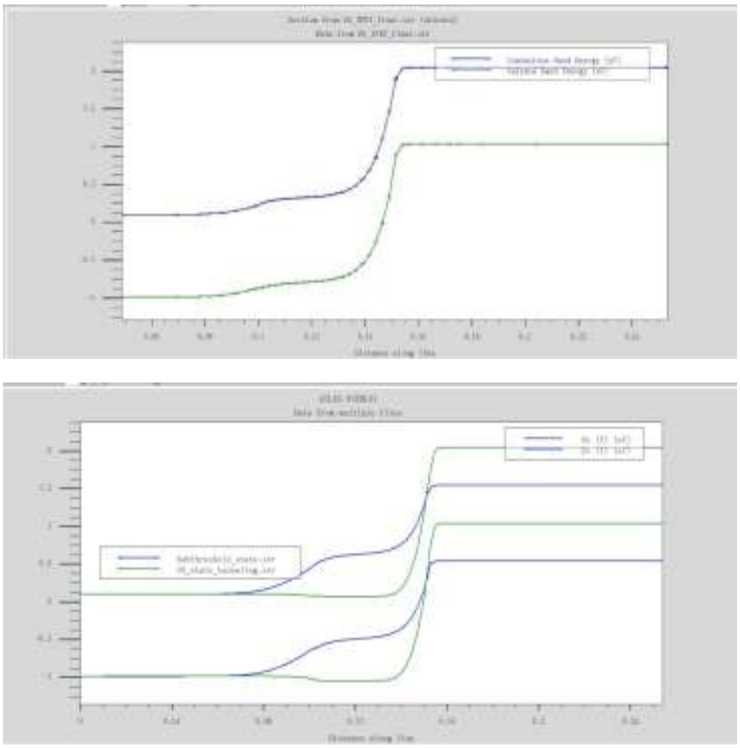


Fig: Energy Band Diagram

4.CONCLUSIONS

The dual-gate configuration provided improved electrostatic control over the channel, resulting in enhanced band-to-band tunneling efficiency. Compared to conventional MOSFET structures, the DG-TFET exhibited a significantly steeper subthreshold slope, enabling operation below the thermionic limit of 60 mV/decade. The device showed reduced off-state leakage current due to better gate control and optimized source-channel junction design.

The energy band diagrams obtained from the simulation confirmed effective tunneling at lower gate voltages. Drain current characteristics (Id–Vg and Id–Vd) indicated improved switching behavior and higher on-current with appropriate doping optimization. The dual-gate structure also minimized short-channel effects, enhancing scalability for nanoscale dimensions. Electric field distribution analysis revealed strong tunneling near the source region, validating the device design strategy.

Parameter optimization in Silvaco TCAD further improved the Ion/Ioff ratio, making the DG-TFET suitable for ultra-low-power circuit applications. Overall, the simulation results confirm that the DG-TFET structure offers superior performance, reduced power consumption, and better control compared to single-gate TFET designs, making it a promising candidate for future low-voltage semiconductor technologies

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