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Single-Switch DC-DC Converter Topology for High Voltage Gain

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Abstract— **This paper proposes a novel high voltage gain DC-DC converter topology designed for renewable energy applications. The converter utilizes a coupled inductor with its primary winding connected to the input, which ensures continuous input current a desirable feature for renewable energy sources (RES). The proposed topology operates using a single power switch, and a clamping circuit is employed to reduce the voltage stress across this switch. As a result, conduction losses in the main switch are minimized. Furthermore, the clamping circuit effectively recycles the energy stored in the leakage inductance of the coupled inductor by charging a capacitor placed across the switch. This energy recycling improves overall efficiency. The converter is designed with fewer components, and the voltage stress across the power switch and diodes is significantly reduced. Consequently, low-voltage-rated components can be selected, leading to cost reduction and enhanced efficiency. Additionally, by altering the connected inductor's turns ratio, the voltage gain can be raised. Both simulation and experimental prototype results show how effective the suggested converter is.**

Keywords: DC-DC converter, passive clamping, reverse recovery, two-winding coupled-inductor, leakage inductance low voltage stress.

1.INTRODUCTION

Nowadays, DC-DC converters are being utilized more and more in a variety of sectors and applications, such as electric trains, uninterruptible power sources, electric vehicle charging stations, and renewable energy systems [1]. Alternative energy sources such as solar panels and fuel cells typically generate low DC output voltages. To make these voltages suitable for practical use, high voltage gain DC-DC converters are necessary. The conventional converter faces several limitations especially when high voltage gain is required to 8-10 times. To increase output voltage, a higher duty cycle is needed, which also results cycle also results in greater voltage stress on the switching devices and semiconductor devices like diodes, capacitor etc. When required the components with higher voltage ratings and contributing to increasing energy losses and overall cost. As a result of the aforementioned impacts, the conventional converter's overall efficiency has significantly decreased. Therefore, large voltage gain cannot be achieved with ordinary converters. Numerous research studies have

examined various DC-DC converter configurations intended to produce high voltage gain in the literature. These include techniques such as switched inductors, switched capacitor, cascaded stages and voltages multiplier cells [2]-[7]. Although the aforementioned converter topologies are capable of achieving substantial voltage gains, semiconductor components are subjected to increasing voltage stress [6], [8]. In [9], the output diode's reverse recovery performance was subpar despite the large voltage gain.

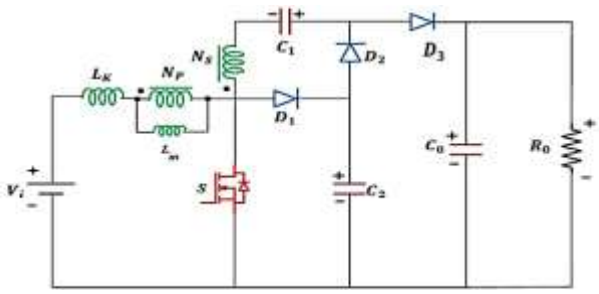

Fig. 1. The proposed converter

In order to solve the above problems, coupled inductor -based configuration have been proposed in the literature. In this topology minimize the number of components and reduce voltage stress on switching devices and semiconductor devices [10]. In coupled inductor converters, the impact of leakage energy becomes more significant as the turns ratio and switching frequency. Several studies have explored methods to mitigate the leakage energy in coupled inductor converters by RCD snubber circuits. According to the RCD snubber circuit approach, the snubber resistance dissipates the leakage energy [11]. Active and passive clamp circuits are further techniques [10]. In order to accomplish the recycling process, the active clamp circuit requires an additional switch and capacitor; however, this design does not use an active clamp circuit due to switching losses and the need for an additional switch [12]. In addition to reducing input current ripple, a passive clamp circuit recycles the energy from leakage inductance to the load without switching losses [13-16].

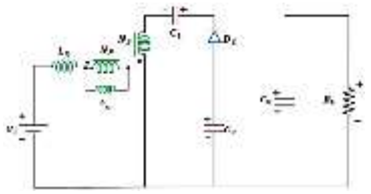

Fig. 2. Mode 1

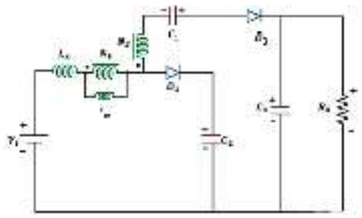

Fig. 3. Mode 2

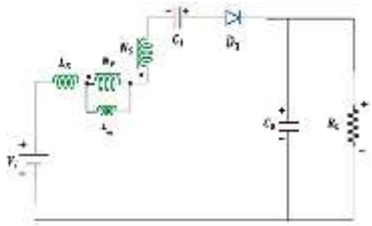

Fig. 4. Mode 3

2.Derivation of Proposed Topology

The suggested converter is displayed in Fig. (1). It has a voltage multiplier and a boost stage. One active switch is used for the whole operation of the voltage multiplier and boost stage. The capacitor C_2 receives the magnetizing and leakage energy of the coupled inductor during the boost stage. The multiplier helps to raise the converter's voltage gain. An additional benefit is that the energy held in capacitor C_2 due to boost stage operation can be returned to the load via the voltage multiplier's capacitor C_1. A connected inductor's duty cycle or turns ratio can be increased slightly to provide a comparatively greater shift in voltage gain. In the suggested topology with a single switch connection, the voltage stress is medium. The input side and the output side are not the same. This improves the switch's ability to withstand both voltage and current stress. In order to achieve a high coupling coefficient, the coupled inductor was built using a bi-filar winding procedure without air in the core. As a result, it is evident that primary leakage inductance has no effect on switching transients. Additionally, compared to traditional converters, the suggested converter provides low voltage stress across the switches; as a result, the primary switch's low on-state resistance can be used to reduce switch losses. Through simulation, experimental research, and a thorough comparison with the current solution, the suggested concept is validated.

3.Operating Principle of the Proposed Converter:

This section describes the steady-state operation of the proposed DC-DC converter and identifies its various modes of operation. The converter comprises a power switch (S), capacitors (C_1, C_2, C_0), diodes (D_1, D_2, D_3), a coupled inductor (Lm), and a load resistor (R_0). Although the

internal resistances of these components are considered in loss calculations, they are neglected in the idealized analysis presented here.

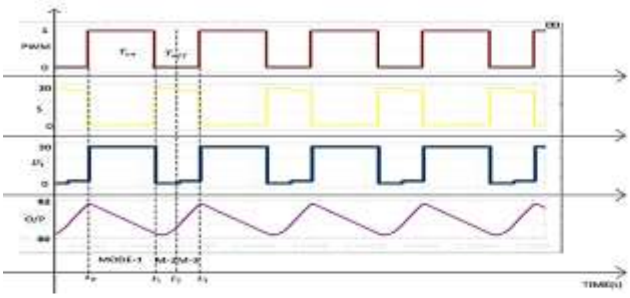

Fig. 5. Voltage waveforms of the proposed Converter where PWM, Switch (S), Diode (D_1), Output (V_0)

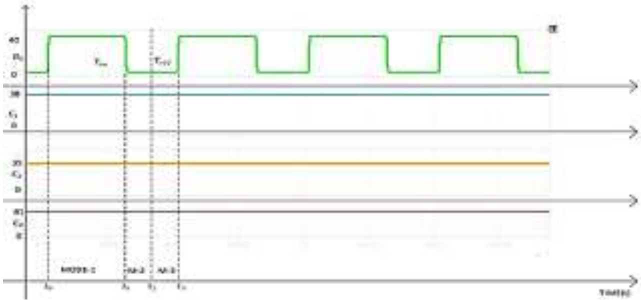

Fig. 6. Voltage waveforms of the proposed Converter where Diode (D_3), Capacitor (C_1), Capacitor (C_2), Capacitor (C_0)

In this topology, the inductor Lm represents the magnetizing inductance, which is associated with the mutual magnetic flux linking the primary and secondary windings. The leakage inductance (L_k) accounts for the flux that does not link both windings and is distributed between the primary and secondary sides of the coupled inductor. For analytical simplicity, the leakage inductances from both sides are assumed to be equal and are referred to the primary side. However, the same analysis approach remains valid even if the leakage inductances differ.

The proposed converter introduces a modified topology that utilizes a single active switch, coupled inductors, clamping diodes, and voltage-lift capacitors to address the limitations of conventional high-gain converters. This design achieves a high voltage conversion ratio even at moderate duty cycles and significantly reduces voltage stress across the power switch. As a result, the converter not only enhances efficiency but also allows for the use of low-voltage-rated components, leading to a more compact and cost-effective solution.

Circuit Description

- Coupled Inductor: Replaces the conventional inductor to boost voltage gain using the turns ratio.
- Single MOSFET Switch: Reduces control complexity and cost.
- Clamping Diode and Capacitor: Used to recycle leakage energy and clamp switch voltage.
- Output Diode and Filter Capacitor: Ensure rectification and voltage smoothing.

There are two modes of operation:

Mode-1 [t_0-t_1]: This mode is a transient state where the switch on and diode D_2 is forward biased. This is shown in the fig. (2) Diodes D_1 and D_3 are reverse biased. The source voltage V_i charge L_k and L_m of the coupled inductor through the switch. Due to this the leakage current in the coupled inductor increase. The energy stored in the capacitor C_2 is transferred to capacitor C_1. Output capacitor C_0 supplies the load current.

$$V_{lm} = V_{in}$$
$$V_S = K\,V_{lm} = K\,V_{in}$$
$$V_{C1} = V_{C2} + K\,V_{in}$$

Mode-2 [t_1-t_2]: In this mode, the power switch is turned off and diodes (D_1 and D_3) are forward biased while the other diode(D_2) is reversed biased the leakage and magnetizing energy through diode D_1 and it charges the capacitor C_2. [This mode ends when the diode D_1 current have reached zero. As shown in fig. (3) The capacitor C_1 gets charged by the energy storage in the coupled inductor and input voltage V_{in}. The capacitor C_2 receives the leakage energy V_{in} diode D_1. The output capacitor C_0 gets charged V_{in} diode D_3 using the stored energy of capacitor C_1 and coupled inductor.

$$V_{switch} = V_{C2} = \frac{V_{in}}{1-D}$$
$$V_{C1} = V_{in} + \frac{V_{in}}{1-D}$$
$$V_{lm} = V_{in} - V_{C2}$$
$$V_{D1} = V_{C2} - V_{in}$$
$$V_{D3} = V_{C0} - V_{C2}$$

Mode-2 [t_2-t_3]: This mode is initiated when the diode current I_{D1} have reached zero the magnetizing energy of the coupled inductor and the stored energy of capacitor C_1 are discharged to the load. As shown in fig. (4)

$$V_{D2} = V_{C1} - K\,V_{in}$$
$$V_0 = 4V_{in} + \frac{V_{in}}{1-D}$$

Where the coefficient of coupled inductor

$$K = \frac{L_m}{L_m + L_K}$$

The converter voltage gain is

$$L_m = \frac{5-4D}{1-D}$$

The volt-sec balancing law is applied to the coupled inductor and current ripple given as

$$\Delta\, I_{lm} = \frac{D\,V_{in}}{f\,L_m 1-D}$$

The required value of the capacitor Co and C1 given as

$$C_0 = \frac{D\,I_0}{f\,\Delta\,V_0}$$
$$C_1 = \frac{D\,I_0(2+K)}{f\,\Delta\,V_{C1}}$$

4.(a) Efficiency Analys:

At a rated power of 13W, the theoretical analysis indicates that diode losses are the most significant, contributing up to 1W. The forward voltage drops for the diodes are considered as 0.3V for D_1 and D_2, and 0.43V for D_3. Additionally, the magnetic losses in the system are approximately 0.12W, with the core of the coupled inductor (EE35/29/12) constructed using FP40 (N67) material. The switching losses are estimated at around 0.28W, while capacitor losses amount to roughly 0.11W. Overall, the proposed power converter achieves an efficiency of around 96% at full load.

4.(b) Leakage Energy Analysis

The suggested topology has the benefit of recycling leakage energy, as illustrated in Fig. 1, which considerably lowers the voltage stress on the switch. This improvement is seen in Fig. 2, where the efficient use of the otherwise wasted leakage energy results in a noticeably decreased voltage stress. On the other hand, Fig. 1's redesigned converter architecture, which connects diode D_2's anode, does not offer a way to recycle leakage energy. Consequently, as shown in Fig. 3, this setup experiences continuous switching voltage transients. It can be concluded that the suggested topology successfully reduces switching voltage stress by permitting leakage energy recycling, as confirmed by the observation of a voltage spike of about 30V during the switch turn-off period, which further confirms the lack of energy recovery in this instance.

5. Comparison with Conventional Topologies

A comparison was made between the proposed converter and conventional high-gain topologies such as the quadratic boost and the interleaved boost. The proposed topology offered competitive voltage gain with reduced component count and control complexity.

Topology	Voltage Gain	Component Count	Control Complexity	Efficiency (%)
Conventional Boost	4–5×	Low	Low	80–85
Quadratic Boost	7–9×	Medium	Medium	85–90
Proposed Topology	7×	Low	Low	93-96

6.Experimental Verification:

A hardware prototype of the proposed converter was developed in the laboratory, as illustrated in Fig. (7). This topology consist of PWM circuit and power circuit. This converter is designed to step up an input voltage of 12V (Vi) to an output voltage of 82V (Vo), with a power rating of 13W. It operates at a switching frequency of 100 kHz. The component specifications include capacitors C1 and C2 each rated at 47 µF, and C0 rated at 100 µF. The coupled inductor consists of a leakage inductance (Lk) of 6 µH and a magnetizing inductance (Lm) of 200 µH.

The chosen semiconductor devices include VT3045C diodes for D1 and D2, an NTST40120CTG diode for D3, and an FDPF085N10A MOSFET used as the main switch (S). The inductor values were selected to maintain a current ripple of approximately 3% of the average inductor current, while the capacitors were chosen to ensure a voltage ripple of around 2% of the rated capacitor voltage.

Voltage waveforms for the load (Vo) and the switch (Vs) are depicted in the corresponding figure, showing that Vs is approximately 15% of Vo when operating at a duty cycle of 0.64. Additional waveforms such as diode reverse voltages, capacitor voltages, and currents through the coupled inductor are also provided. These measurements closely align with the predicted theoretical values, validating the converter's design.

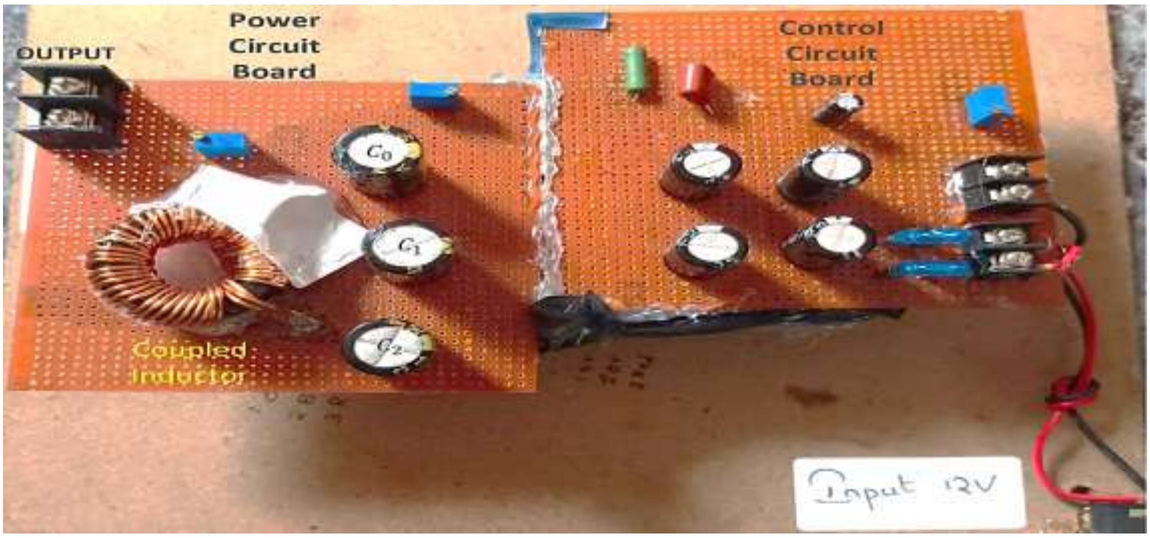

Fig. 7. hardware setup

Input Output

Fig. 8. Results

The experimental results indicate that, for a constant power output, the converter's efficiency improves as the input voltage increases. The maximum efficiency recorded is around 95% when the input voltage is raised to 15V. It's also evident that recycling the leakage energy significantly enhances efficiency compared to a system without energy recovery. At the rated output power of 13W, the converter achieves an experimental efficiency of approximately 96% with leakage energy recovery, whereas it drops to about 90.2% without it.

It was also observed that as output power increases, the overall efficiency tends to decrease. This drop is more pronounced if the leakage energy is not effectively recycled, highlighting the importance of energy recovery mechanisms at higher power levels. Lastly, the dynamic response of the converter is found to be robust under both load increase and decrease scenarios, showing good performance during step load changes.

7.RESULT AND DISCUSSION

To evaluate the performance of the proposed single-switch DC-DC converter topology, both simulation and hardware prototype tests were conducted. The design targets applications that require a high step-up voltage gain while maintaining efficiency and simplicity in control. Voltage Gain: The converter was designed to step up an input voltage of **12 V** to a target output voltage of **82 V**, achieving a gain of **7×**. The measured gain closely matched the theoretical predictions, validating the analytical model. The high voltage gain was made possible by integrating coupled inductors and a voltage multiplier network, which reduced the stress on the switch and passive components.

8.CONCLUSION

Using a boost stage with a linked inductor and a passive voltage multiplier, a high voltage gain DC-DC converter with a single switch and continuous input current is demonstrated. minimal-resistance MOSFETs can be used for increased efficiency since this arrangement maintains minimal voltage stress across the power switch and diodes while achieving a significant voltage gain of up to seven times the input. Performance is enhanced by the voltage multiplier's recycling of the associated inductor's leakage energy. Through design processes, efficiency estimates, and steady-state modeling, the converter is thoroughly examined.When compared to current topologies under the same power and voltage parameters, comparative assessments reveal that it provides greater voltage gain, lower switch and diode voltage stresses, and less input current ripple. The success of the converter is confirmed by both simulation and hardware findings, underscoring the advantages of leakage energy recovery and its influence on overall performance and efficiency.

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