International Research Journal of Engineering and Management Studies (IRJEMS)
Volume: 03 Issue: 05 | May -2019 ISSN: 2395-0126

Speed Control of BLDC Motor using PWM Technique

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Abstract— Efficiency and Reliability are the key features for the development of advanced motor drives. Residential and commercial appliances such as refrigerators and air conditioning systems use conventional motor drive technology. A brushless DC (BLDC) motor drive is characterized by higher efficiency, lower maintenance, and higher cost. Therefore, it is necessary to have a low-cost but effective BLDC motor controller. PWM has been widely used in power converter control. PWM control is the most power full technique that offer a simple method for controlling of analog system with processors digital output. PWM frequency depends on the target FPGA device speed and duty cycle resolution requirement. In this paper, BLDC motor drive controlled using FPGA controller.

Keywords - Brushless DC (BLDC) motor drives, converters, field-programmable gate arrays (FPGAs), inverters, pulse width modulation (PWM).

I.INTRODUCTION

An electrical motor is defined as a mechanical transducer that converts electrical energy into mechanical energy. Electric motors are an integral part of industrial plants. Residential and commercial applications mostly use conventional motor drive technologies. Electric motors are responsible for consuming more than half of all the electrical energy used in the world. In every industry there are processes that require adjustment for normal speed. Such adjustments are usually accomplished with variable speed drive and it consists of electrical motor, power converter and controller. Typically, machines found in all appliances are single-phase induction motors or brushed dc machines which are characterized by low efficiency and high maintenance, respectively [1]. Single-phase induction motors are less efficient because of

The ohmic loss in the rotor and due to the phase angle displacement between the stator current and back electromotive force (EMF). But the above losses are less in BLDC motor due to the absence of brushes and mechanical commutation. Different methods are available for speed control of BLDC motor, like DC link variable voltage, PWM technique, etc.

In this paper, PWM technique has been employed. Nowadays different PWM techniques are available, like Sinusoidal, multiple sinusoidal, 60 degree modulation etc. Here, sinusoidal PWM technique is used for controlling the speed of BLDC motor, because it is easy and less time consuming. This paper introduce speed control of BLDC motor has been achieved through variation of duty cycle. Simulation result is verified with FPGA (Field Programming Gate Array) based hardware.

II.BLDC MOTOR: AN INTRODUCTION

BLDC motor is a brushless motor. The name itself implies that there are no brushes and commutator. In BLDC Motor the commutation is performed with the help of electronic circuit, which reduces the mechanic losses and improves the efficiency. Replacing the inefficient motors with more efficient BLDC motors will result in substantial energy savings. A BLDC has several advantages over other machine types. Most notably they require lower maintenance due to the elimination of the mechanical commutator. It also has high power density. Compared to induction machines, BLDC motors have lower inertia, allowing for faster dynamic response to reference commands.

The major disadvantage with permanent-magnet motors is their higher cost and relatively greater degree of complexity introduced by the power electronic converter used to drive them. The speed of the motor is directly proportional to the applied voltage. By varying the average voltage across the windings, the speed can be altered. This is achieved by altering the duty cycle of the base PWM signal.

The use of PWM in power electronics to control high energy with maximum efficiency & power saving is not new but, interesting is to generate PWM signals using HDL and implementing it in FPGA. FPGAs are increasingly being used in motor control applications due to their robustness and customizability.

Microcontrollers have typically been used to implement motor controls, with computation algorithms executed by software. Some of the challenges in this implementation are response time, a fixed number of PWM channels, limited communication interfaces and pre-determined analog triggering.

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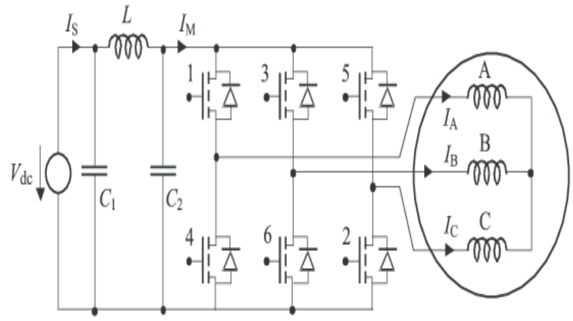
III. FIELD-PROGRAMMABLE GATE ARRAY

The Field Programmable Gate Array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing hence "field programming". The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application specific (ASIC).The generic architecture of an SRAMbased FPGA as shown in Fig.1



IV. DRIVE STRATEGY

BLDC motor have two types of driving strategies namely, uni-polar and bipolar drives. A three-phase (brushless) motor is driven by a three-phase bridge circuit, comprising of IGBTs as shown in Fig 2. The efficiency, which is the ratio of the mechanical output power to the electrical input power, is the highest, since in this drive an alternating current flows through each winding as an ac motor. This drive is often referred to as bipolar drive. Here, 'bipolar' means that a winding is alternatively energized in the south and north poles. The bipolar driving strategy includes sensor based and sensor-less techniques. Position encoders and back EMFs are used in sensor-less techniques. Whereas, hall sensors, and optical sensors are used in sensor based techniques.The EMF can have a trapezoidal or sinusoidal waveform.

In this paper we consider that the rotor information is being collected using hall sensors. The Hall position sensors are placed 120 degree apart and they sense the actual rotor position.

V_a, V_b, V_c are the phase voltage

$I_a, I_b,$ are the phase current

E_a, E_b, E_c are the back EMFs

The back EMFs can be expressed as,

$E_a = K_e\omega_m F(\theta_e)$ ……………………………..(4)

$E_b = K_e\omega_m F(\theta_e - \frac{2\pi}{3})$ ………………………..(5)

$E_c = K_e\omega_m F(\theta_e + \frac{2\pi}{3})$…………………………………… (6)

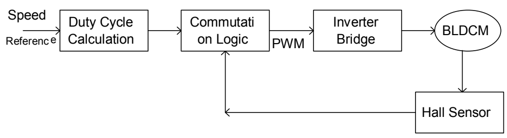
Where,

ω_m is Angular speed of rotor.

θ_m is Mechanical angle of rotor.

θ_e is Electrical angle of rotor.

$F(\theta_e)$ is Back –EMF reference function of rotor position.



V. SIMULATION RESULTS & EXPERIMENT VERIFICATION

Speed control of BLDC motor using variation of duty cycle, is shown in fig 6. Average output voltage is controlled through duty cycle of PWM. The relationship between average output voltage, duty cycle and input voltage is,

$V_{avg} = D\, V_{input}$………………………………. (7)

Where,

D = Duty cycle

V_{avg} = Average output voltage

V_{input}= Input DC voltage

Table-I Experiment Parameters

Terminal voltage	Volts DC	310
Rated current	Amps	4.52
No of Poles		4
Rated torque	N*m	2.2

VI. CONTROL STRATEGY

PWM technique is one of the most popular speed control techniques for BLDC motor. In this technique a high frequency chopper signal with specific duty cycle is multiplied by switching signals of VSI. Therefore it is possible to adjust output voltage of inverter by controlling duty cycle of switching pulses of inverter. The disadvantages of analog methods are that they are prone to noise and they change with voltage and temperature change. Also they suffer changes due to component variation.They are less flexible as compared to digital methods. PWM signals are generated from the Spartan-3A processor by writing VHDL program to control the inverter switches. The principle of generating PWM waveform is shown in Fig 5. Counter is used to generate triangular wave. The value of compare register is compared with triangular wave. If the value of compare register is less than the value of triangular wave, then PWM is ‘1’, else PWM is ‘0’.

Rotor inertia	Kg*m	1.4-1.8
IPM Module	PEC16D5M01	
SPARTAN 3A KIT	FPGA	
Voltage Constant	Volts	5
Torque Constant	N*m	0.49
Auto Transformer Current Rating	Amps	4

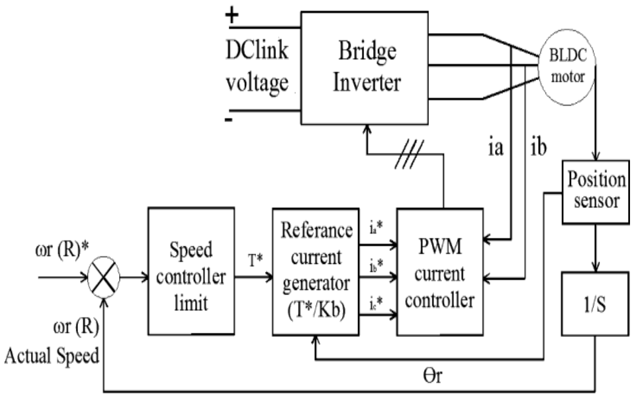
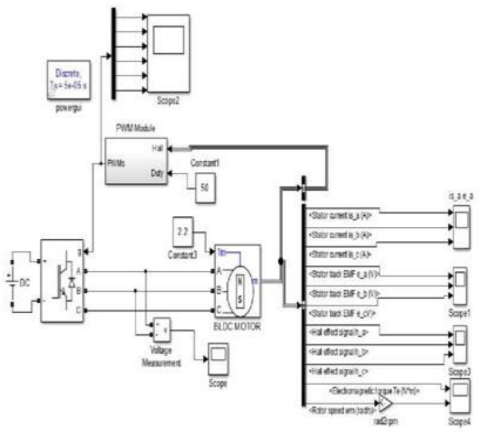


Fig. 7 and 8 show stator current and back EMF of BLDC motor respectively. Three phase stator currents (I_a, I_b, I_c) and back EMFs (E_a, E_b, E_c) are 120□ phase shifted with respect to each other. Back EMF is constant for each 60 degree interval. In Fig. 7 and Fig. 8, the stator current is 5. torque; the speed is 1950 rpm. 8A and the back EMF is and the back EMF is 49V. Fig. 9 shows the rotor speed of BLDC motor at a rated



49V. Fig. 9 shows the rotor speed of BLDC motor at a rated torque; the speed is 1950 rpm

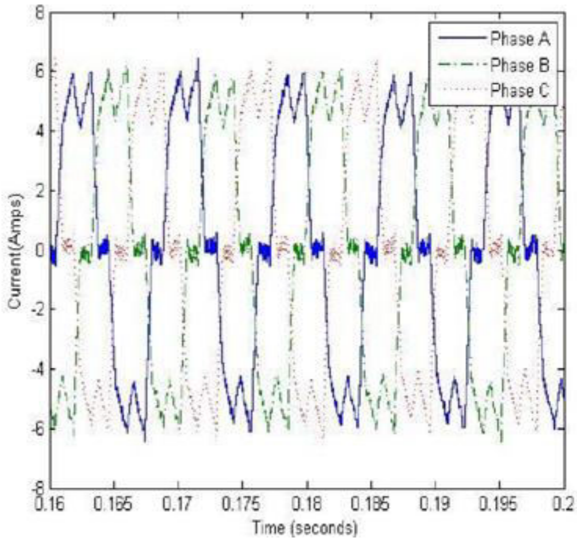


Fig. 7

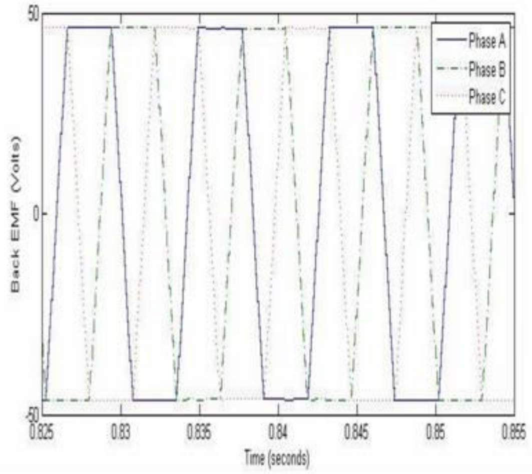


Fig. 11 Pictorial view of experiment setup of BLDC motor

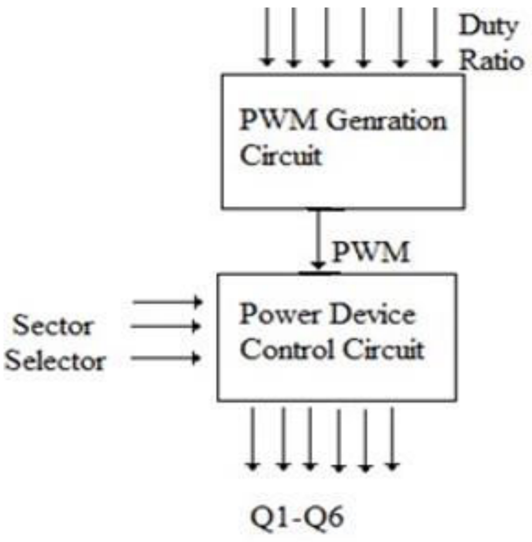
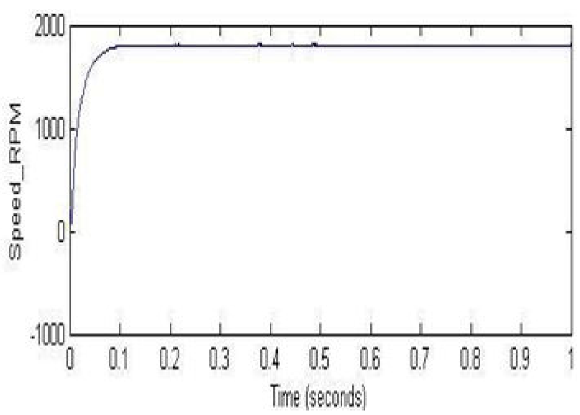
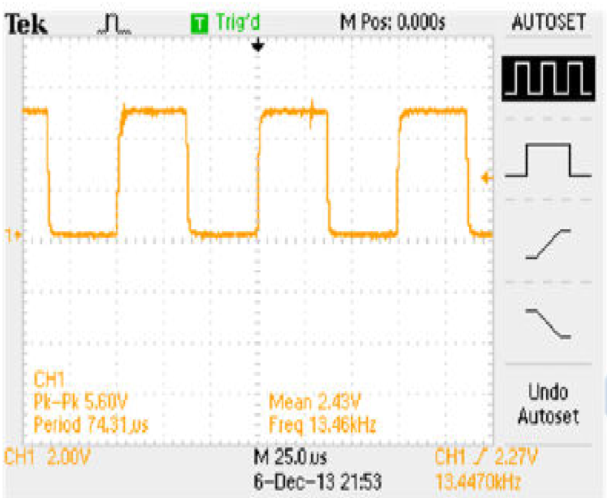
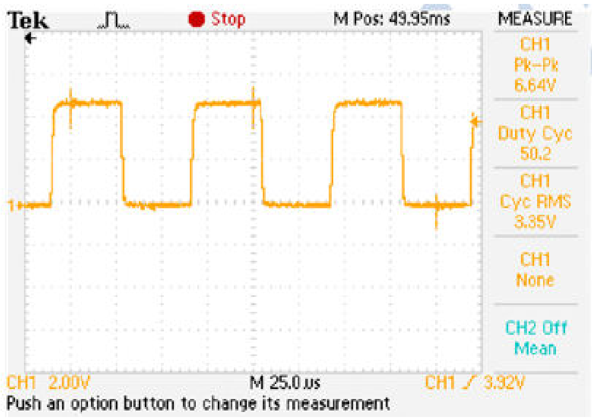


Fig.10 Block digram of FPGA implemation

Fig. 8 Back EMF of BLDC motor







VII. CONCLUSION

A fuzzy logic controller (F) has been employed for the speed control of PMBLDC motor drive and analysis of results of the performance of a fuzzy controller is presented. The modelings and simulation of the complete drive system is described in this thesis. Effectiveness of the model is established by performance prediction over a wide range of operating conditions. A performance comparison between the fuzzy logic controller and the conventional PI controller has been carried out by simulation runs confirming the validity and superiority of the fuzzy logic controller for implementing the fuzzy logic controller to be adjusted such that manual tuning time of the classical controller is significantly reduced. The performance of the PMBLDCM drive with reference to PI controller, FLC controller and experimental verified with conventional PI controller using DSP processor. Fuzzy logic speed controller improved the performance of PMBLDC Drive of the fuzzy logic speed controller.

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