International Journal of Scientific Research in Engineering and Management (IJSREM)
Volume: 06 Issue: 12 | December - 2022 Impact Factor: 7.185 ISSN: 2582-3930

Subthreshold Leakage Current Reduction Technique in Large Scale Integration with SRAM

Prof. Dipangi Nayak[1], Prof. Suresh S. Gawande[2]

[1]Professor, Department of Electronics and Communication Engineering, BERI, Bhopal, India

[2]Professor, Department of Electronics and Communication Engineering, BERI, Bhopal, India

Email- *dipanginayak@gmail.com*

Abstract - Static power dissipation is due to leakage current when the transistor is normally off. The two main sources of power dissipation in CMOS circuits are static and dynamic power dissipation. By scaling down the feature size the dynamic power dissipation has no effect but the static power dissipation has become equal or more than that of Dynamic power dissipation. So, in recent CMOS technologies static power dissipation i.e. power dissipation due to leakage current has become a challenging area for VLSI chip designers. Leakage current occurs in both active and standby modes. Gate leakage, subthreshold leakage cannot be solved by MOS structures nor by introducing new material. One of the feasible solutions is by combinational use of Low-*Vt* transistors for its high-speed capability and High-*Vt* transistors for very small leakage current. Multi-Threshold CMOS(MTCMOS) and Variable-Threshold CMOS (VTCMOS) are biasing techniques that uses combinations of different threshold voltage and are suitable for SRAM design.

Keywords: leakage power, CMOS, VTCMOS, *Feature size, Subthreshold,*

1.INTRODUCTION

Power dissipation is regarded as top-priority issue. Highly desirable aspect of VLSI circuits is the low power consumption of the circuit with high performance as it directly relates to reliability, heat removal packaging and cost. Dynamic power consumption of the circuit is reduced as a result of scaling Vdd but its performance is degraded.[1] This performance degradation can be partially compensated by lowering threshold voltage but at the cost of increased leakage power. Leakage current is because of sub threshold leakage, reverse bias p-n junction leakage, gate oxide tunneling leakage, gate induced drain leakage and punch through current.[2] The leakage current is mainly due to the result of reverse biased PN junction leakage and subthreshold leakage. Sub threshold leakage

is due to current flows between drain and source of a MOSFET in weak inversion region. (2)

$$I_{sub} = I_{so} \exp (V_{gs} - V_{th} / V_{th})(1-\exp(-V_{ds} / V_T)) \quad (1)$$

$$I_{so} = \mu 0\, C_{ox}\, W_{eff}/L_{eff} V^2 e^{1.8} \quad (2)$$

The level of integration of random-access memory cells (RAM) too, has reached the gigabit

size with deep submicron technology.[3] Complexity of the system has also pushed up the energy consumption, power requirements and power dissipation. Power and energy dissipation are the key importance to high performance circuit. The subthreshold leakage current reduction by application of two most popular leakage current reduction techniques, MTCMOS and VTCMOS, on SRAM. A 256-bits SRAM circuits was designed and simulated with 0.18µm TSMC process and typical power supply of 1.8v.

2.EFFECTS ON LEAKAGE CURRENT

Subthreshold leakage current occurs in both active and standby periods. Standby leakage current depends when circuits are in idle mode where no circuit activity takes place. When performance is not required, switched off the leakage current. Fig 1(a). shows change in bulk or substrate source voltage (V_{bs}) will vary the threshold voltage device. This is not possible all time to shut of the leakage current completely during this time. Threshold voltage is increased with the substrate voltage. In this picture standby mode is not visible with this plot. These characteristics shows with logarithmic scale plotting the drain source current (I_{ds}). Fig. 1(b)

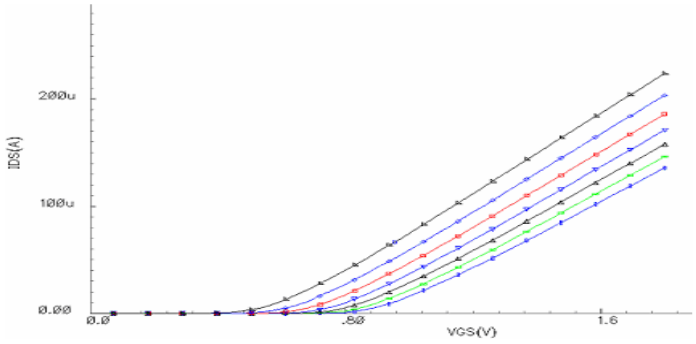

Fig.1(a) effects on substrate voltage variation to threshold voltage (V_t)

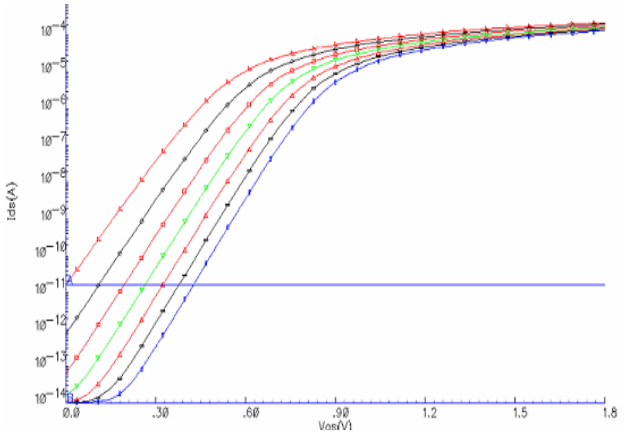

Fig. 1(b) shows Log(i_{ds}), leakage current plot

Whenever the threshold voltage increased, leakage current will be reducing from 10 (pa) to 10 (fa). Figure shows parametric sweeping of 300mv steps on V_{bs} will vary the

leakage current by the 10s of pa, which is 1000 times, under 27^0c of room temperature.

3.LEAKAGE CURRENT REDUCTION TECHNIQUES

There are lots of techniques are involved to reduce the leakage current. A great number of circuit topologies have been introduced to lower the subthreshold current such as, switched source impedance circuit, switched power supply with level holder, and multiple threshold level. [4,5] The *Vt* variations is particularly useful in SRAM architecture assuming the control circuitry knows when particular memory cells are not required, in other words when it can be switched down to sleep mode.[6] A higher *Vt* - MOS transistor is used during sleep period to prevent the leakage current from a particular node to channel through ground line.

For sub-threshold leakage power reduction, the following are the techniques:

a. SLEEPY KEEPER:

Sleepy keeper is an excellent alternative to sleepy stack since three transistors in sleepy stack are replaced with one transistor in sleepy keeper. Advantage of this sleepy keeper technique is that it reduces the subthreshold leakage current and also retains the present state of the circuit in sleep mode. In Sleepy Keeper additional NMOS is placed in parallel to pull-up sleep transistor which connects VDD to pull-up Network and an additional PMOS is placed in parallel to Pull-down sleep transistor which connects Pull-down Network to the Ground.[7] Dual Threshold Voltages can also be applied to reduce sub-threshold leakage Current.[8]

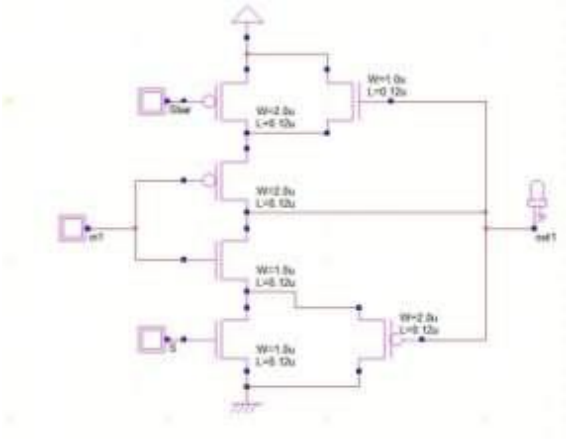

Fig2. Sleepy keeper

b. SLEEPY STACK TECHNIQUE:

Other technique to reduce leakage current is by stacking of the transistor. Stacking of the transistor is done by dividing pull up and pull-down networks into half size where this doesn't affect W/L ratio of given circuit. This technique divides existing transistors circuit into two half-length transistors and sleep transistor is added in parallel to the divided circuit.[9] There are two modes of operation: active mode and sleep mode. During the sleep mode, sleep transistors are turned off. The function of sleep transistor in this circuit is same as in sleep transistor technique. In active mode, sleep transistors are turned on. The stacked transistor suppresses leakage current while saving state. The sleep transistor and the stacked transistor in each network are made parallel. In this technique, the width of the sleep transistors is reduced. Additional tradeoffs between delay, power and area occur by changing the width of the sleep transistors.[8]

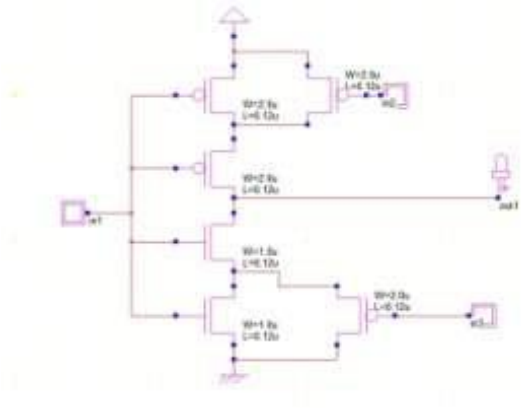

Fig.3. Sleepy Stack Technique

c. VARIABLE-THRESHOLD CMOS(VTCMOS):

The reduction can be achieved by directly manipulating the threshold level in the core logic.[10] In this technique during standby mode, threshold voltage (Vth) is raised by making substrate voltage either higher than supply voltage (for PMOS) or lower than ground (for NMOS). During active mode, a slight forward substrate bias can be used to increase circuit speed. In this technique, an additional power supply is required by the circuit which may be a drawback for commercial designs. The ideal way for determining appropriate threshold level is to have two different levels of threshold, one for standby and another for active. VTCMOS uses different principle with dynamic- *Vdd* scaling. Dynamic- *Vdd* scaling is where the power supply of the core logic is actively scaled according to input and clock requirement and is effective in reducing *Pdynamic*.

d.MULTI-THRESHOLDCMOS (MTCMOS):

MTCMOS or Multi-Threshold CMOS is a circuit technique that uses two different combinations of transistors type. Low- *Vt* transistors for the high-speed core logic and High- *Vt* transistors as power switch to reduce leakage current wasted in the circuit. MTCMOS has been a popular technique because of simplicity of the design. Ideally the larger the threshold level the lower the leakage current.

MTCMOS is a technique to design CMOS circuit using low, normal and high voltage transistors. Using this technique, selective scaling of threshold voltage is done along with supply voltage so as to increase the circuit speed without increasing the subthreshold leakage currents. Therefore, this technique provides high speed as well as low power operation using both high threshold and low threshold transistors.[7] The propagation delay time in the critical path can be reduced by low threshold voltage transistors and the power consumption in the shortest path is reduced by high threshold voltage transistors. There are two modes of operation: active mode and sleep mode. Sleep transistors in MTCMOS circuits are controlled by a “sleep” signal that is used for the active/standby mode control. Usually in standby state there is much leakage current and this leakage current can be reduced by using high threshold transistors (sleep transistors). Both PMOS and NMOS transistors can be used as sleep transistors but by employing NMOS transistor as sleep transistor, the performance of the circuit is enhanced. [11,12]

Standby leakage power is reduced using this technique but the area and delay of the circuit are increased because of the insertion of large MOSFETs.[13] To reduce the area,

one transistor can be used for each group of gates rather than each logic gate.

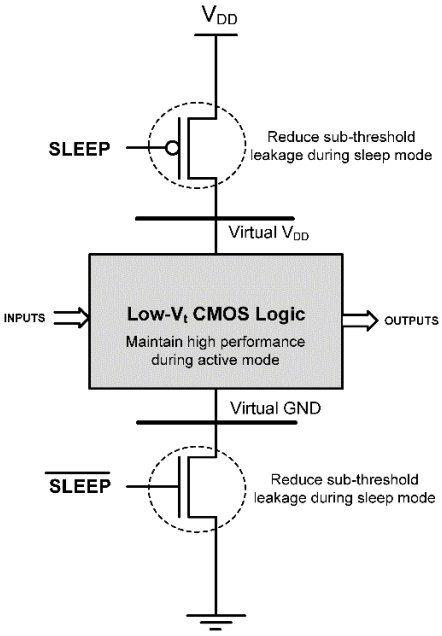

Fig.4.MTCMOS circuit architecture

4.RESULTS ANALYSIS

The active power dissipations measurement was done by writing different data to two different addresses and a read cycle to the first address. In observation, the reading cycle consumes more power as at this time, the sense amplifiers are activated, which dissipate around 20% of total power dissipation.

Simulation readings have also been performed to the bit lines capacitance load effect on read and write propagation delay. Write time is faster compares to read time for a smaller number of rows, as illustrated. However, the read time is larger than write time for larger number of rows, where larger number of rows is typical for present SRAM size.

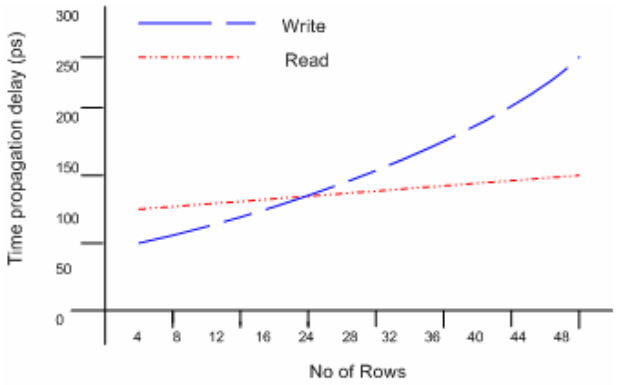

Fig.5. Time propagation delay of different number of memory cells rows

Technique parameter	Sleepy stack	Sleepy keeper	Sleep Transistor
Power	6.014	5.514	2.747
Delay	9	41.5	4.5
Current	0.130	0.100	.096
Area	50.22	50.22	33.06
Performance	Good	Poor	Poor

Table1: Comparison of Leakage Reduction Technique

Technique	Power Saving	Delay	Area
VTCMOS	50%	25%	1%
MTCMOS	10%	4.6-8.4%	2%
DTCMOS	98%	44%	0%

Table 2: Percentage of Power Saving, Delay and Area for a S27(ISCAS89 Benchmark) Circuit

5.CONCLUSION

In low power VLSI design, leakage power reduction plays a prominent role. As the scaling of technology and in the pursuit of improving the performance of the system, leakage power has increased to a greater extent. As threshold voltage reduces with technology scaling results in increasing of static leakage current. A large circuit such as memory circuits will suffer from leakage current and memory designers need to reduce leakage current to reduce overall power consumption. The advantage of leakage current reduction techniques such as MTCMOS and VTCMOS proves to reduce the static leakage current, but with a slight trade off in circuit delay. Various sub-threshold leakage current reduction techniques have been discussed in this paper and one can opt for a technique depending on the requirement. All the above-mentioned techniques are applicable at circuit level. For more power saving than existing circuit level techniques, leakage reduction techniques can be applied at gate level and block level in the future.

ACKNOWLEDGEMENT

I would like to convey my heartfelt gratitude to Prof. Suresh S. Gawande as a professor from Bhabha engineering college of research and institute, Bhopal, India for his tremendous support and assistance in the completion of my project and special thanks to my family, husband and friends who supports me to do this work.

REFERENCES

[1] Dhananjay E. Upasani, Sandip B. Shrote, and Pallavi S. Deshpande, Standby Leakage Reduction in Nanoscale CMOS VLSI Circuits, *International Journal of Computer Applications, 7(5),* 2010, 1-4

[2] Roy K. ,Mukhopadhyay S.,and Mahmoodi-Meimand H., Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits, *Proceedings of the IEEE, 91(2),* 2003, 305-327

[3] J. Poullon ," An Embeded SRAM for CMOS ASIC's," University of North Carolina,

[4] N. Shibata, H. Morimura, M. Harada, "1-V 100MHz Embedded SRAM Techniques for Battery Operated MTCMOS, SIMOX ASICS," *IEEE Journ. Solid State Circuits,* Vol. 35, No. 10, pp. 1396-1407, 2000.

[5] K. Agowa, H. Hera, T. Takayanagi, T. Kurada, "A Bitline Leakage Compensation Scheme for Low Voltage SRAMS," *IEEE Journ. Solid State Circuits,* Vol. 36, No. 5, pp. 726-734, 2001

[6] D. Fitrio, A. Stojcevski, J. Singh, "Leakage Current Reduction Techniques for Subthreshold Circuit in a Simulation Environment," *Int. Conference on Modeling & Simulation (ICMS),* 2004

[7] Vandana B, M.Siva Kumar, Theoretical Study of MOSFET Multi Threshold Voltage over Single Threshold

Voltage, *International Journal of Engineering Science and Innovative Technology (IJESIT), 2(2)*, 2013, 352-363

[8] Chowdhury, A.J. Rizwan, M.S. ; Nibir, S.J. ; Siddique, M.R.A., A New Leakage Reduction Method for Ultra Low Power VLSI Design for Portable Devices, *IEEE International Conference on Power, Control and Embedded Systems (ICPCES)*,pp. 1-4, December 2012, Allahabad, India

[9] Ajay Kumar Dadoria, and KavitaKhare, A Novel Approach for Leakage Power Reduction Techniques in 65nm Technologies *International Journal of VLSI design & Communication Systems (VLSICS), 5(3)*, 2014, 1-11

[10] T. Kobayashi, T. Sakurai, "Self Adjusting Threshold Voltage Scheme (SATS) for Low Voltage High Speed Operation," *Cust. Integrated Circuit Conference*,pp. 271-274, 1994

[11] K.Sailaja, V. Leela Rani, and Sk.MahammadAkram Analysis of Leakage Power Reduction Techniques for Low Power VLSI Design, *International Journal of Computer Applications, 82(18)*, 2013, 20-23

[12] Abdollahi, A. , Fallah, F.; Pedram, M., Leakage Current Reduction in CMOS VLSI Circuits by Input VectorControl, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *12(2*), 2004, 140-154

[13] Patikineti Sreenivasulu, Srinivasa Rao, and Vinaya Babu, Ultra-Low Power Designing for CMOS Sequential Circuits, *Int. J. Communications, Network and System Sciences*, 2015,

BIOGRAPHY

Dipangi Nayak is post graduated in VLSI Design from RGPV University Bhopal, India. she is awarded with Young India Scientist Congress in the year 2015 and 2017. She is currently working as a prof. in engineering college in electronics department. She is completed her project speech recognition using MFCC and retina scanning in 2015 and international paper has been published.